Add a below restriction to above mentioned applicable products.

**RA2A1 Group**

**14.2.5 Restriction on Exclusive Access**

The main bus does not support exclusive transfers and there is no global monitor in the MCU.

The main bus always deasserts the HEXOKAY signal (a signal in the AHB-Lite protocol) to the CPU.

This means that a store exclusive instruction such as STREX instruction always gets a failed status.

When an exclusive write operation is performed by the CPU, the main bus always writes the data successfully.

**RA2L1/RA2E1/RA2E2 Group**

**13.2.5 Restriction on Exclusive Access**

The main bus does not support exclusive transfers and there is no global monitor in the MCU.

The main bus always deasserts the HEXOKAY signal (a signal in the AHB-Lite protocol) to the CPU.

This means that a store exclusive instruction such as STREX instruction always gets a failed status.

When an exclusive write operation is performed by the CPU, the main bus always writes the data successfully.