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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A326A/E	Rev.	1.00
Title	About the specification change of TPU and port 1		Information Category	Technical Notification		
Applicable Product	H8/38086R Group H8/38076R Group	Lot No. All	Reference Document	H8/38086R Group Hardware manual (REJ09B0182-0200 Rev.2.00) H8/38076R Group Hardware manual (REJ09B0093-0300 Rev.3.00)		

The specification of TPU and the port of the H8/38086R group and the H8/38076R group will be changed, Please refer to the following for details of the hardware manual.

Before change

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		Pin No.					
Type	**Symbol**	**FP-80A, TFP-80C**	**TLP-85V**	**Pad No.*1**	**Pad No.*2**	**I/O**	**Functions**
16-bit timer pulse unit (TPU)	TIOCA1	80	A3	81	80	I/O	Pins for the TGR1A input capture input or output compare output, or PWM output.
	TIOCB1	1	B1	1	1	I/O	Pins for the TGR1B input capture input or output compare output, or PWM output.
	TIOCA2	2	C1	2	2	I/O	Pins for the TGR2A input capture input or output compare output, or PWM output.
	TIOCB2	3	B2	3	3	I/O	Pins for the TGR2B input capture input or output compare output, or PWM output.
	TCLKA	80	A3	81	80	Input	External clock input pins.
	TCLKB	1	B1	1	1	Input	
	TCLKC	2	C1	2	2	Input	

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12.1 Features

The following operations can be set for each channel:

Waveform output at compare match

Input capture function

Counter clear operation

Multiple timer counters (TCNT) can be written to simultaneously

Simultaneous clearing by compare match and input capture is possible

Register synchronous input/output is possible by synchronous counter operation

PWM output with any duty level is possible

A maximum 3-phase PWM output is possible in combination with synchronous operation

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Table 12.1 TPU Functions

Item		Channel 1	Channel 2
Compare match output	0 output	O	O
	1 output	O	O
	Toggle output	O	O

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Figure 12.1 Block Diagram of TPU

Input/output pins

Channel 1: TIOCA1

TIOCB1

Channel 2: TIOCA2

TIOCB2

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Table 12.2 Pin Configuration

Channel	Symbol	I/O	Function
Common	TCLKA	Input	External clock A input pin
	TCLKB	Input	External clock B input pin
	TCLKC	Input	External clock C input pin
1	TIOCA1	I/O	TGRA_1 input capture input/output compare output/PWM output pin
	TIOCB1	I/O	TGRB_1 input capture input/output compare output/PWM output pin
2	TIOCA2	I/O	TGRA_2 input capture input/output compare output/PWM output pin
	TIOCB2	I/O	TGRB_2 input capture input/output compare output/PWM output pin

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Table 12.7 TIOR_1(Channel 1)

				Description	
Bit 7 IOB3	Bit 6 IOB2	Bit 5 IOB1	Bit 4 IOB0	TGRB_1 Function	TIOCB1 Pin Function
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCB1 pin Input capture at rising edge
			1		Capture input source is TIOCB1 pin Input capture at falling edge
		1	X		Capture input source is TIOCB1 pin Input capture at both edges
	1	X	X		Setting prohibited

[Legend]

X: Don’t care

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Table 12.8 TIOR_2(Channel 2)

				Description	
Bit 7 IOB3	Bit 6 IOB2	Bit 5 IOB1	Bit 4 IOB0	TGRB_2 Function	TIOCB2 Pin Function
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	X	0	0	Input capture register	Capture input source is TIOCB2 pin Input capture at rising edge
			1		Capture input source is TIOCB2 pin Input capture at falling edge
		1	X		Capture input source is TIOCB2 pin Input capture at both edges

[Legend]

X: Don't care

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(b) Examples of Waveform Output Operation

Figure 12.10 shows an example of 0 output/1 output.

In this example, TCNT has been designated as a free-running counter, and settings have been made such that 1 is output by compare match A, and 0 is output by compare match B. When the set level and the pin level match, the pin level does not change.

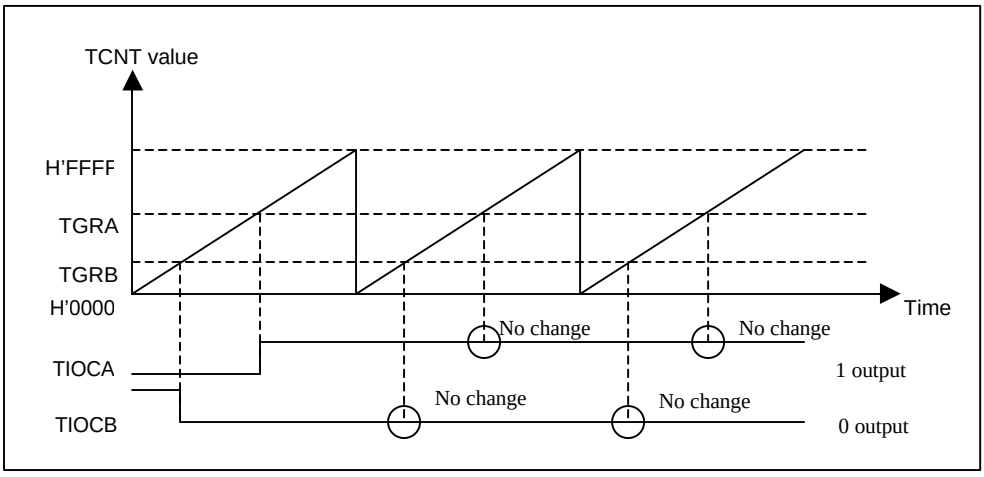

Figure12.10 Example of 0 Output/1 Output Operation

Figure 12.11 shows an example of toggle output.

In this example, TCNT has been designated as a periodic counter (with counter clearing on compare match B), and settings have been made such that the output is toggled by both compare match A and compare match B.

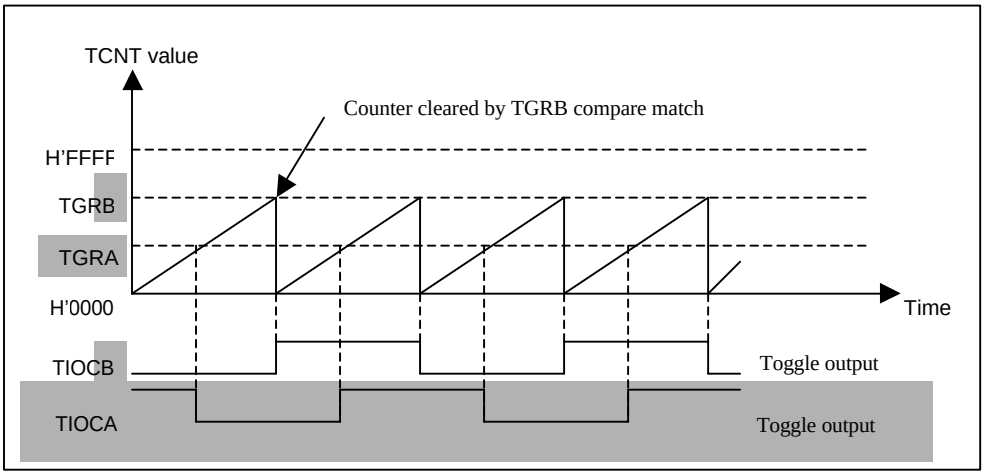

Figure 12.11 Example of Toggle Output Operation

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Table 12.12 PWM Output Registers and Output Pins

Channel	Registers	Output Pins: PWM Mode 1	Output Pins: PWM Mode 2*
1	TGRA_1	TIOCA1	TIOCA1
	TGRB_1		TIOCB1
2	TGRA_2	TIOCA2	TIOCA2
	TGRB_2		TIOCB2

Note:* In PWM mode 2, PWM output is not possible for TGR in which the period is set.

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Figure 12.20 shows an example of PWM mode 2 operation. In this example, synchronous operation is designated for channels 1 and 2, TGRB_1 compare match is set as the TCNT clearing source, and 0 is set for the initial output value and 1 for the output value of the other TGR registers (TGRA_1, TGRB_1, and TGRA_2), outputting a 3-phase PWM waveform.

In this case, the value set in TGRB_1 is used as the cycle, and the values set in the other TGRs are used as the duty levels.

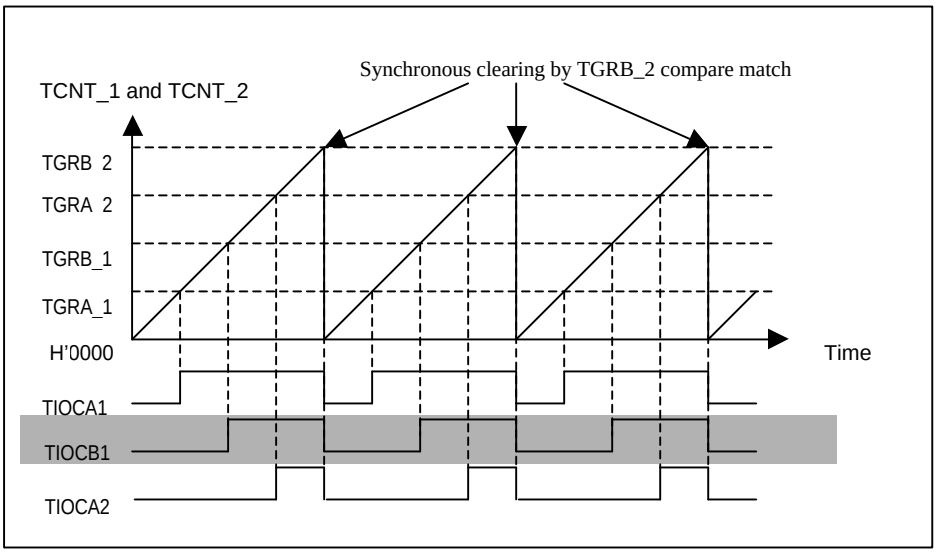

Figure 12.20 Example of PWM Mode Operation (2)

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· P15/TIOCB2 pin

The pin function is switched as shown below according to the combination of the TPU channel 2 setting by the MD1 and MD0 bits in TMDR_2, IOB3 to IOB0 bits in TIOR_2, and CCLR1 and CCLR0 bits in TCR_2, and the PCR15 bit in PCR1.

TPU Channel 2 Setting	Next table (1)	Next table (2)	
PCR15	-	0	1
Pin Function	TIOCB2 output pin	P15 input pin	P15 output pin
		TIOCB2 input pin *	

Note: * When the MD1 and MD0 bits are set to B'00 and the IOB3 bit to 1, the pin function becomes the TIOCB2 input pin.

TPU Channel 2 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD1, MD0	B'00		B'10	B'11		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	-	B'xx00	Other than B'xx00	
CCLR1, CCLR0	-	-	-	-	B'10	B'10
Output Function	-	Output compare output	-	-	PWM mode 2 output	-

[Legend] x: Don't care.

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P13/TIOCB1/TCLKB pin

The pin function is switched as shown below according to the combination of the TPU channel 1 setting by the MD1 and MD0 bits in TMDR_1, IOB3 to IOB0 bits in TIOR_1, and CCLR1 and CCLR0 bits in TCR_1, the TPSC2 to TPSC0 bits in TCR_1 and TCR_2, and the PCR13 bit in PCR1.

TPU Channel 1 Setting	Next table (1)	Next table (2)	
PCR13	-	0	1
Pin Function	TIOCB1 output pin	P13 input pin	P13 output pin
		TIOCB1 input pin *1	
	TCLKB input pin *2		

Notes: 1. When the MD1 and MD0 bits are set to B'00 and the IOB3 bit to 1,the pin function becomes the TIOCB1 input pin.

2.When the TPSC2 to TPSC0 bits in TCR_1 or TCR_2 are set to B'101, the pin function becomes the TCLKB input pin.

TPU Channel 1 Setting	(2)	(1)	(2)	(2)	(1)	(2)
MD1, MD0	B'00		B'10	B'11		
IOB3 to IOB0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	-	B'xx00	Other than B'xx00	
CCLR1, CCLR0	-	-	-	-	Other than B'10	B'10
Output Function	-	Output compare output	-	-	PWM mode 2 output	-

[Legend] x: Don't care.

After change

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Type	Symbol	Pin No. FP-80A, TFP-80C	Pin No. TLP-85V	Pad No.*1	Pad No.*2	I/O	Functions
16-bit timer pulse unit (TPU)	TIOCA1	80	A3	81	80	I/O	Pins for the TGR1A input capture input or output compare output, or PWM output.
	TIOCB1	1	B1	1	1	I	Pins for the TGR1B input capture input
	TIOCA2	2	C1	2	2	I/O	Pins for the TGR2A input capture input or output compare output, or PWM output.
	TIOCB2	3	B2	3	3	I	Pins for the TGR2B input capture input.
	TCLKA	80	A3	81	80	Input	External clock input pins.
	TCLKB	1	B1	1	1	Input	
	TCLKC	2	C1	2	2	Input	

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12.1 Features

The following operations can be set for each channel:

- Waveform output at compare match
- Input capture function
- Counter clear operation
- Multiple timer counters (TCNT) can be written to simultaneously
- Simultaneous clearing by compare match and input capture is possible
- Register synchronous input/output is possible by synchronous counter operation
- PWM output with any duty level is possible
- A maximum 2-phase PWM output is possible in combination with synchronous operation

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Table 12.1 TPU Functions

Item			Channel 1	Channel 2
Compare match output	0 output	TIOCA	O	-
		TIOCB		
	1 output	TIOCA	O	-
		TIOCB		
	Toggle output	TIOCA	O	-
		TIOCB		

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Figure 12.1 Block Diagram of TPU

Input/output pins

Channel 1: TIOCA1

Channel 2: TIOCA2

Input pins

Channel 1:TIOCB1

Channel 2:TIOCB2

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Table 12.2 Pin Configuration

Channel	Symbol	I/O	Function
Common	TCLKA	Input	External clock A input pin
	TCLKB	Input	External clock B input pin
	TCLKC	Input	External clock C input pin
1	TIOCA1	I/O	TGRA_1 input capture input/output compare output/PWM output pin
	TIOCB1	I	TGRB_1 input capture pin
2	TIOCA2	I/O	TGRA_2 input capture input/output compare output/PWM output pin
	TIOCB2	I	TGRB_2 input capture pin

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Table 12.7 TIOR_1(Channel 1)

				Description	
Bit 7 IOB3	Bit 6 IOB2	Bit 5 IOB1	Bit 4 IOB0	TGRB_1 Function	TIOCB1 Pin Function
0	0	0	0	Output compare register	Output disabled
			1		Setting prohibited
		1	0		
			1		
	1	0	0		
			1		
		1	0		
			1		
1	0	0	0	Input capture register	Capture input source is TIOCB1 pin Input capture at rising edge
			1		Capture input source is TIOCB1 pin Input capture at falling edge
		1	X		Capture input source is TIOCB1 pin Input capture at both edges
	1	X	X		Setting prohibited

[Legend]

X: Don’t care

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Table 12.8 TIOR_2(Channel 2)

				Description	
Bit 7 IOB3	Bit 6 IOB2	Bit 5 IOB1	Bit 4 IOB0	TGRB_2 Function	TIOCB2 Pin Function
0	0	0	0	Output compare register	Output disabled
			1		Setting prohibited
		1	0		
			1		
	1	0	0		
			1		
		1	0		
			1		
1	0	0	0	Input capture register	Capture input source is TIOCB2 pin Input capture at rising edge
			1		Capture input source is TIOCB2 pin Input capture at falling edge
		1	X		Capture input source is TIOCB2 pin Input capture at both edges
	1	X	X		Setting prohibited

[Legend]

X: Don’t care

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(b) Examples of Waveform Output Operation

Figure 12.10 shows an example of 0 output/1 output

In this example, TCNT has been designated as a free-running counter, and setting the 1 is output by compare match A. When the set level and the pin level match, the pin level does not change.

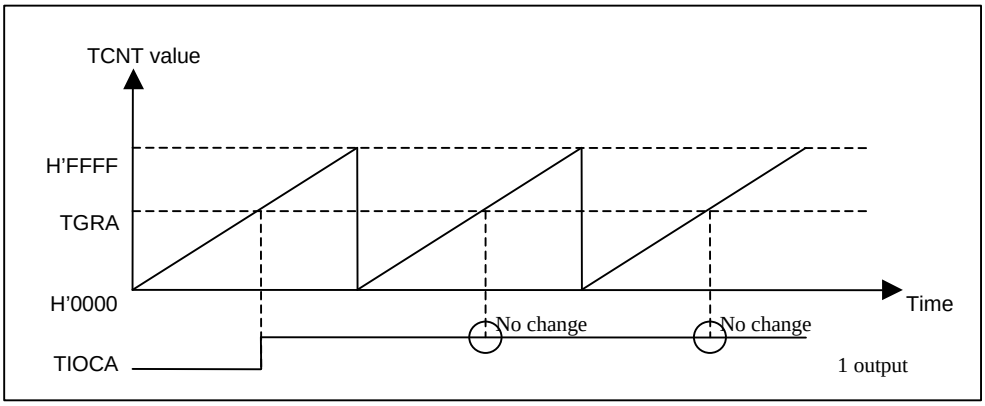

Figure12.10 Example of 1 Output Operation

Figure 12.11 shows an example of toggle output.

In this example, TCNT has been designated as a periodic counter (with counter clearing on compare match B), and settings have been made such that the output is toggled by both compare match A and compare match B.

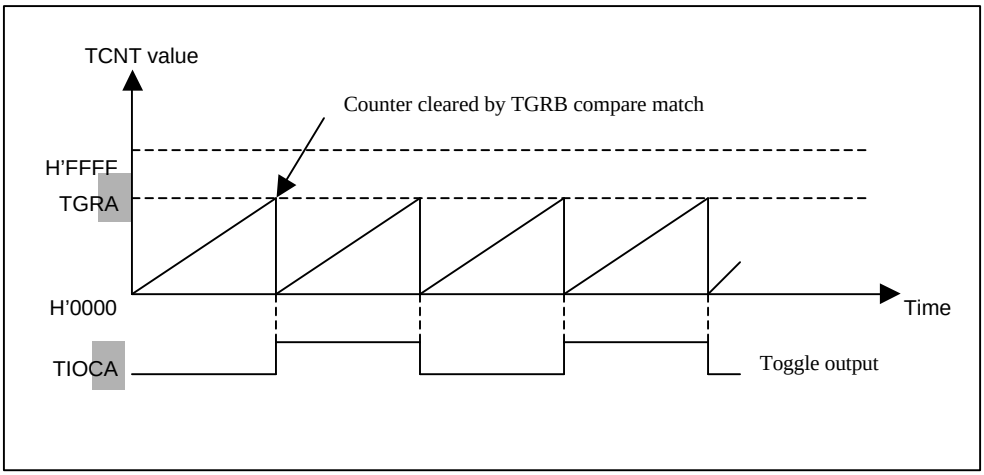

Figure 12.11 Example of Toggle Output Operation

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Table 12.12 PWM Output Registers and Output Pins

		Output Pins	
Channel	Registers	PWM Mode 1	PWM Mode 2
1	TGRA_1	TIOCA1	TIOCA1
	TGRB_1		-
2	TGRA_2	TIOCA2	TIOCA2
	TGRB_2		-

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Figure 12.20 shows an example of PWM mode2 operation. In this example, synchronous operation is designated for channels 1 and 2, TGRB_2 compare match is set as the TCNT clearing source, and 0 is set for the initial output value and 1 for the output value of the other TGR registers (TGRA_1, and TGRA_2), outputting a 2-phase PWM waveform.
In this case, the value set in TGRB_2 is used as the cycle, and the values set in the other TGRs are used as the duty levels.

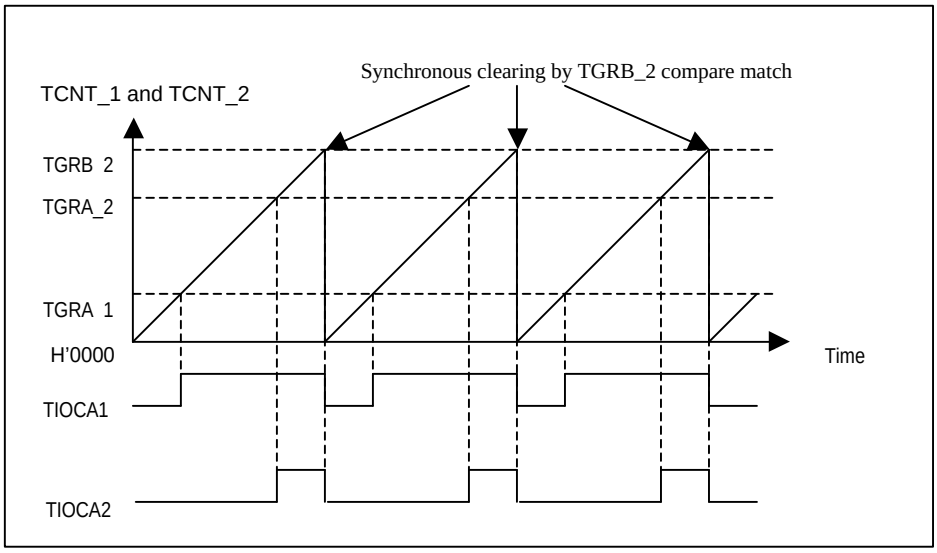

Figure 12.20 Example of PWM Mode Operation (2)

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· P15/TIOCB2 pin

The pin function is switched as shown below according to the combination of the TPU channel 2 setting by the MD1 and MD0 bits in TMDR_2, IOB3 to IOB0 bits in TIOR_2, and CCLR1 and CCLR0 bits in TCR_2, and the PCR15 bit in PCR1.

TPU Channel 2 Setting	Next table (1)	Next table (2)		Next table (3)	
PCR15	-	0	1	0	1
Pin Function	-	P15 input pin	P15 output pin	P15 input pin	P15 output pin
				TIOCB2 input pin	

TPU Channel 2 Setting	(2)	(3)	(1)	
MD1, MD0	B'00			B'10, B'01, B'11
IOB3 to IOB0	B'0000	B'1xxx	B'0001 to B'0111	B'xxxx
CCLR1, CCLR0	B'xx			
Output Function	-		Setting prohibited	

[Legend] x: Don't care.

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· P13/TIOCB1/TCLKB pin

The pin function is switched as shown below according to the combination of the TPU channel 1 setting by the MD1 and MD0 bits in TMDR_1, IOB3 to IOB0 bits in TIOR_1, and CCLR1 and CCLR0 bits in TCR_1, the TPSC2 to TPSC0 bits in TCR_1 and TCR_2, and the PCR13 bit in PCR1.

TPU Channel 1 Setting	Next table (1)	Next table (2)		Next table (3)	
PCR13	-	0	1	0	1
Pin Function	-	P13 input pin	P13 output pin	P13 input pin	P13 output pin
				TIOCB1 input pin	
		TCLKB input pin *1			

TPU Channel 1 Setting	(2)	(3)	(1)	
MD1, MD0	B'00			B'10, B'01, B'11
IOB3 to IOB0	B'0000	B'1xxx	B'0001 to B'0111	B'xxxx
CCLR1, CCLR0	B'xx			
Output Function	-	Setting prohibited		

[Legend] x: Don't care.