To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-H8*-A333B/E	Rev.	2.00
Title	About the SCI3 specification change.		Information Category	Technical Notification		
Applicable Product	Please see following description.	Lot No. All	Reference Document	Please see following description.		

The target product that the following show deletes the multiprocessor communication function of SCI3 from the specification.

< Target product manual>

H8/38086R Group Hardware Manual (REJ09B0182-0200)

H8/38076R Group Hardware Manual (REJ09B0093-0300)

H8/38024,H8/38024S,H8/38024R,H8/38124 Group Hardware Manual (REJ09B0042-0700)

H8/3887 Series Hardware Manual (ADE-602-151A)

H8/3867 Series Hardware Manual (ADE-602-142B)

H8/3847R Group H8/3847S Group H8/38347 Group H8/38447 Group Hardware Manual (REJ09B0145-0500)

H8/3827R Group H8/3827S Group H8/38327 Group H8/38427 Group Hardware Manual (REJ09B0144-0500)

H8/3802,H8/38004,H8/38002S,H8/38104 Group Hardware Manual (REJ09B0024-0600)

H8/38602R Group Hardware Manual (REJ09B0152-0200)

The explanation and the communication format etc. of SCI3 register are shown in the following and other multiprocessor communication functions are deleted from the specification.

Change point from Rev.1:

Bit 2(MPIE) of cereal control register (SCR)

Rev.1: When this bit is one, the format of 5 bits communication becomes possible.
In the case of writing 1 to this bit, bit5 (PE) should be written with 1 all at once.
Please write 1 to the bit 3 of Serial control register (SCR) before writing 1 in this bit

Rev.2: It's a reserved bit.
When this bit is one, the format of 5 bits communication becomes possible.
In the case of writing 1 to this bit, bit5 (PE) should be written with 1 all at once.

Bit 3(MPIE) of cereal control register (SCR)

Rev.1: Bit3 is reserved, this can only be written with 1.

Rev.2: It's a reserved bit.

[Before change]

Serial mode register (SMR)

Bit	7	6	5	4	3	2	1	0
	COM	CHR	PE	PM	STOP	MP	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 2 : Multiprocessor Mode (MP)

When this bit is set to 1, the multiprocessor communication function is enabled. The PE bit and PM bit settings are invalid. In clocked synchronous mode, this bit should be cleared to 0.

[after change]

Serial mode register (SMR)

Bit	7	6	5	4	3	2	1	0
	COM	CHR	PE	PM	STOP	MP	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 2 : 5 bit communication (MP)

When this bit is one, the format of 5 bits communication becomes possible.

In the case of writing 1 to this bit, bit5 (PE) should be written with 1 all at once.

[Before change]

Serial mode register (SMR)

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 3 : Multiprocessor Interrupt Enable (MPIE)

When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and OER status flags in SSR is prohibited. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed.

[after change]

Serial mode register (SMR)

Bit	7	6	5	4	3	2	1	0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 3 : Reserved bit

It's a reserved bit.

[Before change]

Serial Status Register (SSR)

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	OER	FER	PER	TEND	MPBR	MPBT
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Bit 1 : Multiprocessor Bit Receive (MPBR)

MPBR stores the multiprocessor bit in the receive character data. When the RE bit in SCR is cleared to 0, its previous state is retained.

Bit 0 : Multiprocessor Bit Transfer (MPBT)

MPBT stores the multiprocessor bit to be added to the transmit character data.

[after change]

Serial Status Register (SSR)

Bit	7	6	5	4	3	2	1	0
	TDRE	RDRF	OER	FER	PER	TEND	MPBR	MPBT
Initial value	1	0	0	0	0	1	-	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Bit 1 : Reserve bit

It's a reserved read-only bit.

Bit 0 : Reserve bit

The write value should always be 0.

[Before change]

Data Transfer Formats (Asynchronous Mode)

SMR				Serial Data Transfer Format and Frame Length											
CHR	PE	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	0	S	8-bit data								STOP		
0	0	0	1	S	8-bit data								STOP	STOP	
0	0	1	0	S	8-bit data								MPB	STOP	
0	0	1	1	S	8-bit data								MPB	STOP	STOP
0	1	0	0	S	8-bit data								P	STOP	
0	1	0	1	S	8-bit data								P	STOP	STOP
0	1	1	0	S	5-bit data					STOP					
0	1	1	1	S	5-bit data					STOP	STOP				
1	0	0	0	S	7-bit data							STOP			
1	0	0	1	S	7-bit data							STOP	STOP		
1	0	1	0	S	7-bit data							MPB	STOP		
1	0	1	1	S	7-bit data							MPB	STOP	STOP	
1	1	0	0	S	7-bit data							P	STOP		
1	1	0	1	S	7-bit data							P	STOP	STOP	
1	1	1	0	S	5-bit data					P	STOP				
1	1	1	1	S	5-bit data					P	STOP	STOP			

[after change]

Data Transfer Formats (Asynchronous Mode)

SMR				Serial Data Transfer Format and Frame Length											
CHR	PE	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	0	S	8-bit data								STOP		
0	0	0	1	S	8-bit data								STOP	STOP	
0	0	1	0	Setting prohibited											
0	0	1	1	Setting prohibited											
0	1	0	0	S	8-bit data								P	STOP	
0	1	0	1	S	8-bit data								P	STOP	STOP
0	1	1	0	S	5-bit data					STOP					
0	1	1	1	S	5-bit data					STOP	STOP				
1	0	0	0	S	7-bit data							STOP			
1	0	0	1	S	7-bit data							STOP	STOP		
1	0	1	0	Setting prohibited											
1	0	1	1	Setting prohibited											
1	1	0	0	S	7-bit data							P	STOP		
1	1	0	1	S	7-bit data							P	STOP	STOP	
1	1	1	0	S	5-bit data					P	STOP				
1	1	1	1	S	5-bit data					P	STOP	STOP			

[Before change]

SMR Settings and Corresponding Data Transfer Formats

SMR									
Bit 7 COM	Bit 6 CHR	Bit 2 MP	Bit 5 PE	Bit 3 STOP	Mode	Data Length	Multiprocessor Bit	Parity Bit	Stop Bit Length
0	0	0	0	0	Asynchronous mode	8-bit data	No	No	1 bit
				1					2 bits
			1	0				Yes	1 bit
				1					2 bits
	1		0	0		7-bit data		No	1 bit
				1					2 bits
			1	0				Yes	1 bit
				1					2 bits
	0	1	0	0		8-bit data	Yes	No	1bit
				1					2 bits
			1	0		5-bit data	No		1bit
				1					2 bits
	1		0	0		7-bit data	Yes		1bit
				1					2 bits
			1	0		5-bit data	No	Yes	1bit
				1					2 bits
1	*	0	*	*	Clocked synchronous mode	8-bit data	No	No	No

[Legend] *: Don't care

[After change]

SMR Settings and Corresponding Data Transfer Formats

SMR									
Bit 7 COM	Bit 6 CHR	Bit 2 MP	Bit 5 PE	Bit 3 STOP	Mode	Data Length	Multiprocessor Bit	Parity Bit	Stop Bit Length
0	0	0	0	0	Asynchronous mode	8-bit data	No	No	1 bit
				1					2 bits
			1	0				Yes	1 bit
				1					2 bits
	1		0	0		7-bit data		No	1 bit
				1					2 bits
			1	0				Yes	1 bit
				1					2 bits
	0	1	0	0	Setting prohibited				
				1					
			1	0		5-bit data	No		1bit
				1					2 bits
	1		0	0	Setting prohibited				
				1					
			1	0		5-bit data	No	Yes	1bit
				1					2 bits
1	*	0	*	*	Clocked synchronous mode	8-bit data	No	No	No

[Legend] *: Don't care