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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A815A/E	Rev.	1.00
Title	About change of SH7730 AC bus timing spec.		Information Category	Technical Notification		
Applicable Product	SH7730 Group	Lot No. From September, 2011	Reference Document	SH7730 Hardware Manual Rev3.00 (REJ09B0359-0300)		

AC bus timing spec of SH7730 Group is changed. Please refer to change part as shown in the following.

Before change

Table 33.9 Bus Timing

Conditions: Clock Modes 0/3, $V_{CC}Q$ = 3.0 to 3.6 V, V_{CC} = 1.1 to 1.3 V, T_a = -20 to 75°C

Item	Symbol	Min.	Max.	Unit	Figure
Address delay time 1	t_{AD1}	1	13	ns	33.8 to 33.38
Address delay time 2	t_{AD2}	$1/2t_{cyc}$	$1/2t_{cyc}$ + 13	ns	33.15
Address setup time	t_{AS}	0	-	ns	33.8 to 33.15
Address hold time	t_{AH}	0	-	ns	33.8, 33.9
$\overline{BS}$ delay time	t_{BSD}	-	13	ns	33.8 to 33.34
$\overline{CS}$ delay time 1	t_{CSD1}	1	13	ns	33.8 to 33.38
Read/write delay time 1	t_{RWD1}	1	13	ns	33.8 to 33.38
Read strobe delay time	t_{RSD}	$1/2t_{cyc}$	$1/2t_{cyc}$ + 13	ns	33.8 to 33.15, 33.35, 33.36
Read data setup time 1	t_{RDS1}	$1/2t_{cyc}$ + 10	-	ns	33.8 to 33.14, 33.33 to 33.38
Read data setup time 2	t_{RDS2}	7	-	ns	33.16 to 33.19, 33.24 to 33.26, 33.33, 33.34
Read data setup time3	t_{RDS3}	$1/2t_{cyc}$ + 10	-	ns	33.15
Read data hold time 1	t_{RDH1}	0	-	ns	33.8 to 33.14, 33.33 to 33.38
Read data hold time 2	t_{RDH2}	2	-	ns	33.16 to 33.19, 33.24 to 33.26, 33.33, 33.34
Read data hold time3	t_{RDH3}	0	-	ns	33.15
Write enable delay time 1	t_{WED1}	$1/2t_{cyc}$	$1/2t_{cyc}$ + 13	ns	33.8 to 33.13, 33.37, 33.38
Write enable delay time 2	t_{WED2}	-	13	ns	33.14
Write data delay time 1	t_{WDD1}	-	13	ns	33.8 to 33.14, 33.35 to 33.38
Write data delay time 2	t_{WDD2}	-	13	ns	33.20 to 33.23, 33.27 to 33.29, 33.33, 33.34

Item	Symbol	Min.	Max.	Unit	Figure
Write data hold time 1	t_{WDH1}	1	-	ns	33.8 to 33.14, 33.33 to 33.38
Write data hold time 2	t_{WDH2}	1	-	ns	33.20 to 33.23, 33.27 to 33.29, 33.33, 33.34
Write data hold time4	t_{WDH4}	0	-	ns	33.8
Write data hold time5	t_{WDH5}	1	-	ns	33.35 to 33.38
$\overline{WAIT}$ setup time 1	t_{WTS1}	$1/2t_{cyc}$ + 7	-	ns	33.8 to 33.15, 33.36, 33.38
$\overline{WAIT}$ hold time 1	t_{WTH1}	$1/2t_{cyc}$ + 2	-	ns	33.8 to 33.15, 33.36, 33.38
$\overline{RAS}$ delay time 1	t_{RASD1}	1	13	ns	33.16 to 33.34
$\overline{CAS}$ delay time 1	t_{CASD1}	1	13	ns	33.16 to 33.34
DQM delay time 1	t_{DQMD1}	1	13	ns	33.16 to 33.34
CKE delay time 1	t_{CKED1}	1	13	ns	33.31 to 33.34
DACK delay time	t_{DACD}	-	13	ns	33.8 to 33.33
$\overline{ICIORD}$ delay time	t_{ICRSD}	-	$1/2t_{cyc}$ + 13	ns	33.37, 33.38
$\overline{ICIOWR}$ delay time	t_{ICWSD}	-	$1/2t_{cyc}$ + 13	ns	33.37, 33.38
$\overline{IOIS16}$ setup time	t_{IO16S}	$1/2t_{cyc}$ + 6	-	ns	33.38
$\overline{IOIS16}$ hold time	t_{IO16H}	$1/2t_{cyc}$ + 4	-	ns	33.38
$\overline{REFOUT}$, $\overline{IRQOUT}$ delay time	t_{REFOD}	-	$1/2t_{cyc}$ + 13	ns	33.39

After change

Table 33.9 Bus Timing

Conditions: Clock Modes 0/3, $V_{CC}Q$ = 3.0 to 3.6 V, V_{CC} = 1.1 to 1.3 V, T_a = -20 to 75°C

Item	Symbol	Min.	Max.	Unit	Figure
Address delay time 1	t_{AD1}	1	10	ns	33.8 to 33.38
Address delay time 2	t_{AD2}	$1/2t_{cyc}$	$1/2t_{cyc}$ + 10	ns	33.15
Address setup time	t_{AS}	0	-	ns	33.8 to 33.15
Address hold time	t_{AH}	0	-	ns	33.8, 33.9
$\overline{BS}$ delay time	t_{BSD}	-	10	ns	33.8 to 33.34
$\overline{CS}$ delay time 1	t_{CSD1}	1	10	ns	33.8 to 33.38
Read/write delay time 1	t_{RWD1}	1	10	ns	33.8 to 33.38
Read strobe delay time	t_{RSD}	$1/2t_{cyc}$	$1/2t_{cyc}$ + 10	ns	33.8 to 33.15, 33.35, 33.36
Read data setup time 1	t_{RDS1}	$1/2t_{cyc}$ + 7	-	ns	33.8 to 33.14, 33.33 to 33.38
Read data setup time 2	t_{RDS2}	7	-	ns	33.16 to 33.19, 33.24 to 33.26, 33.33, 33.34
Read data setup time3	t_{RDS3}	$1/2t_{cyc}$ + 7	-	ns	33.15
Read data hold time 1	t_{RDH1}	0	-	ns	33.8 to 33.14, 33.33 to 33.38
Read data hold time 2	t_{RDH2}	2	-	ns	33.16 to 33.19, 33.24 to 33.26, 33.33, 33.34
Read data hold time3	t_{RDH3}	0	-	ns	33.15

Write enable delay time 1	t_{WED1}	$1/2t_{cyc}$	$1/2t_{cyc}$ + 10	ns	33.8 to 33.13, 33.37, 33.38
Write enable delay time 2	t_{WED2}	-	10	ns	33.14
Write data delay time 1	t_{WDD1}	-	10	ns	33.8 to 33.14, 33.35 to 33.38
Write data delay time 2	t_{WDD2}	-	10	ns	33.20 to 33.23, 33.27 to 33.29, 33.33, 33.34

Item	Symbol	Min.	Max.	Unit	Figure
Write data hold time 1	t_{WDH1}	1	-	ns	33.8 to 33.14, 33.33 to 33.38
Write data hold time 2	t_{WDH2}	1	-	ns	33.20 to 33.23, 33.27 to 33.29, 33.33, 33.34
Write data hold time4	t_{WDH4}	0	-	ns	33.8
Write data hold time5	t_{WDH5}	1	-	ns	33.35 to 33.38
$\overline{WAIT}$ setup time 1	t_{WTS1}	$1/2t_{cyc}$ + 7	-	ns	33.8 to 33.15, 33.36, 33.38
$\overline{WAIT}$ hold time 1	t_{WTH1}	$1/2t_{cyc}$ + 2	-	ns	33.8 to 33.15, 33.36, 33.38
$\overline{RAS}$ delay time 1	t_{RASD1}	1	10	ns	33.16 to 33.34
$\overline{CAS}$ delay time 1	t_{CASD1}	1	10	ns	33.16 to 33.34
DQM delay time 1	t_{DQMD1}	1	10	ns	33.16 to 33.34
CKE delay time 1	t_{CKED1}	1	10	ns	33.31 to 33.34
DACK delay time	t_{DACD}	-	13	ns	33.8 to 33.33
$\overline{ICIORD}$ delay time	t_{ICRSD}	-	$1/2t_{cyc}$ + 10	ns	33.37, 33.38
$\overline{ICIOWR}$ delay time	t_{ICWSD}	-	$1/2t_{cyc}$ + 10	ns	33.37, 33.38
$\overline{IOIS16}$ setup time	t_{IO16S}	$1/2t_{cyc}$ + 6	-	ns	33.38
$\overline{IOIS16}$ hold time	t_{IO16H}	$1/2t_{cyc}$ + 4	-	ns	33.38
$\overline{REFOUT}$, $\overline{IRQOUT}$ delay time	t_{REFOD}	-	$1/2t_{cyc}$ + 10	ns	33.39