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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-78K-A007A/E	Rev.	1.00
Title	78K0R/Kx3 Restriction of P50 and P51 input access		Information Category	Technical Notification		
Applicable Product	78K0R/Kx3 Expanded-specification products (see 1.1 Target products list.)	Lot No. All lots	Reference Document	User's manuals of target products U17894EJ9V0UD00 Rev.9.00 U18432EJ5V0UD00 Rev.5.00 U18417EJ4V0UD00 Rev.4.00		

A restriction of P50 and P51 input access when the external bus interface is in use has been added for target products indicated above.

Restriction reported in this document

Section	Restriction	Target Products	Page Nos. in This Document
1	78K0R/Kx3 Restriction of P50 and P51 input access	Expanded-specification products of the 78K0R/KG3, 78K0R/KH3, and 78K0R/KJ3 (see 1.1 Target products list)	Pages 2 and 4

List of restrictions which have already been reported

Section	Restriction	Target Products	Page Nos. in This Document
2	Restriction on output level when the clock output and buzzer output controller is stopped	See Attachment 1, List of 78K0R/Kx3 Microcontroller Usage Restrictions	Page 5
3	Restriction on simultaneous use of constant-period interrupt and alarm interrupt of real-time counter		Page 6
4	Restriction on year, month, week, day, hour, minute and second count registers after real-time counter operation is stopped		Page 7
5	Restriction on DMA transfer termination		Pages 8 and 9
6	Restriction on holding a DMA transfer pending by using the DWAITn bit of the DMA controller		Page 10

Note Since the errors in the user's manual were all corrected in a previous technical update (ZBG-CC-09-0009), this document only reports the usage restrictions.

Revision history

Revision history of technical updates on restrictions of the 78K0R/Kx3 products

Document Number	Issued Date	Description
ZBG-CC-07-0021	October 1, 2007	First edition
ZBG-CC-08-0009	June 19, 2008	Correction to errors in the maximum value of the supply current (I_{DD2}) under the conditions of f_{IH} = 8 MHz, in HALT mode
ZBG-CC-09-0009	April 23, 2009	• Correction to errors in electrical specifications for 3-wire serial I/O communication • Correction to errors in DMA controller response time • Addition of a restriction on DMA transfer termination • Addition of a restriction on holding a DMA transfer pending by using the DWAITn bit of the DMA controller

Document Number	Issued Date	Description
TN-78K-A007A/E	Jul. 15, 2016	First edition -Section 1 added in the table under “Restriction reported in this document”. -This document is issued as the first edition because numbering management was changed.

Restriction Added in this Document

1. 78K0R/Kx3 Restriction of P50 and P51 input access

1.1 Target products list

Table 1 : Target Products list

Target Product Group	Target Products
78K0R/KG3	UPD78F1162AGC-UEU-AX UPD78F1163AGC-UEU-AX UPD78F1164AGC-UEU-AX UPD78F1165AGC-UEU-AX UPD78F1166AGC-UEU-AX UPD78F1167AGC-UEU-AX UPD78F1168AGC-UEU-AX, UPD78F1162AGC(A)-UEU-AX UPD78F1163AGC(A)-UEU-AX UPD78F1164AGC(A)-UEU-AX UPD78F1165AGC(A)-UEU-AX UPD78F1166AGC(A)-UEU-AX UPD78F1167AGC(A)-UEU-AX UPD78F1168AGC(A)-UEU-AX UPD78F1162AGF-GAS-AX UPD78F1163AGF-GAS-AX UPD78F1164AGF-GAS-AX UPD78F1165AGF-GAS-AX UPD78F1166AGF-GAS-AX UPD78F1167AGF-GAS-AX UPD78F1168AGF-GAS-AX UPD78F1162AGF(A)-GAS-AX UPD78F1163AGF(A)-GAS-AX UPD78F1164AGF(A)-GAS-AX UPD78F1165AGF(A)-GAS-AX UPD78F1166AGF(A)-GAS-AX UPD78F1167AGF(A)-GAS-AX UPD78F1168AGF(A)-GAS-AX
78K0R/KH3	UPD78F1174AGF-GAT-AX UPD78F1175AGF-GAT-AX UPD78F1176AGF-GAT-AX UPD78F1177AGF-GAT-AX UPD78F1178AGF-GAT-AX UPD78F1174AGF(A)-GAT-AX UPD78F1175AGF(A)-GAT-AX UPD78F1176AGF(A)-GAT-AX UPD78F1177AGF(A)-GAT-AX UPD78F1178AGF(A)-GAT-AX
78K0R/KJ3	UPD78F1184AGJ-GAE-AX UPD78F1185AGJ-GAE-AX UPD78F1186AGJ-GAE-AX UPD78F1187AGJ-GAE-AX UPD78F1188AGJ-GAE-AX UPD78F1184AGJ(A)-GAE-AX UPD78F1185AGJ(A)-GAE-AX UPD78F1186AGJ(A)-GAE-AX UPD78F1187AGJ(A)-GAE-AX UPD78F1188AGJ(A)-GAE-AX

Note Above products are blank products. There are Factory Programming Products and Emboss Taping Products as target products besides above products.

1.2 Usage to which this restriction applies

This restriction applies when the external bus interface is in use (bit 7, EXEN, of the MEM register is set to 1) and all of the following settings are made.

(1) Multiplexed bus mode (bit 3 of the MEM register is set to 0 : MM3=0)

(2) 8-bit bus mode (bit 2 of the MEM register is set to 0 : MM2=0)

(3) 256-byte extension mode (bits 1 and 0 of the MEM register are both set to 0 : MM1,MM0 = 0,0)

1.3 Restriction

P50 and P51 cannot be correctly read when the above settings are made (P50 and P51 cannot be used as input port pins).

1.4 Workaround

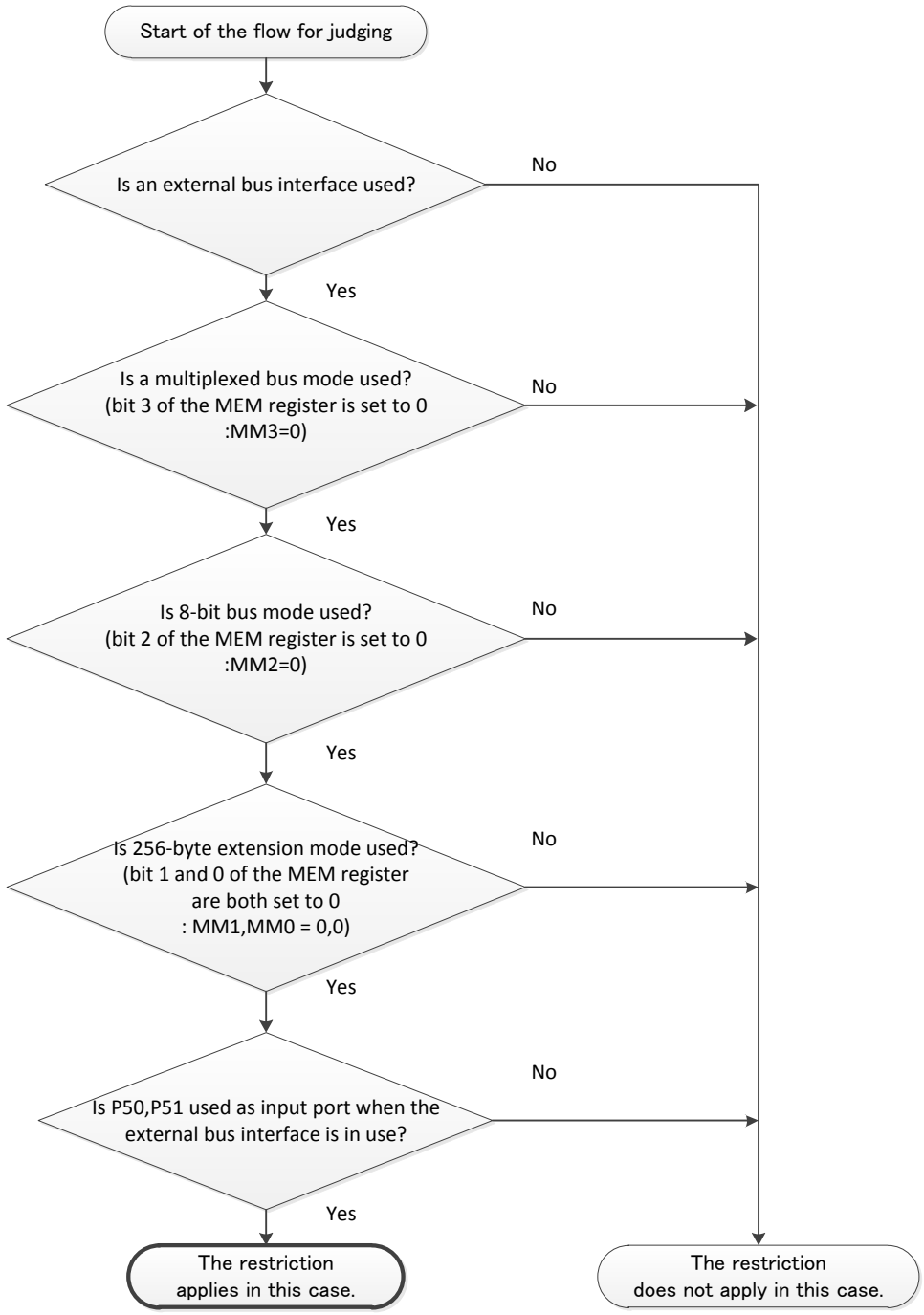
Do not use P50 and P51 as input port pins when the external bus interface function is in use. They can be used as output port pins whether or not the external bus interface is in use.

1.5 Others

This situation is handled as a restriction on usage.

1.6 Check flow

The way to check whether restriction is applied or not is shown in the flowchart.



2. Directions notified in the previous editions

2. Restriction on output level when the clock output and buzzer output controller is stopped

2.1 Usage to which this restriction applies

This restriction applies when a frequency-divided clock other than the original oscillator clock (f_{MAIN}, f_{SUB}) is selected in the CKS register (by setting bits CSELn, CCSn2, CCSn1, and CCSn0), and the clock output and buzzer output are disabled (by clearing the PCLOEn bit).

2.2 Problem

The level of the clock output/buzzer output must be low when the output is disabled, but in the usage mentioned above, the output stops at the level (high or low) for which the output was disabled.

2.3 Temporary workaround (restriction)

The output level will become low by selecting the original oscillation clock (f_{MAIN}, f_{SUB}) in the CKS register after the clock output and the buzzer output are disabled (by clearing the PCLOEn bit). Note that the output level will be low after a high pulse with a different width from the original one has been output.

2.4 Permanent workaround

The devices are being corrected so that the output is stopped at the low level even under the above-mentioned usage. See the *List of 78K0R/Kx3 Microcontroller Usage Restrictions* in attachment 1 for the products subject to correction.

Remark n = 0, 1

3. Restriction on simultaneous use of constant-period interrupt and alarm interrupt of real-time counter

3.1 Usage to which this restriction applies

This restriction applies when constant-period interrupts are enabled (CT2, CT1, and CT0 bits of RTCC0 register are not set to “0, 0, 0”), alarm interrupts are enabled (WALE and WALIE bits of RTCC1 register = 1), and a constant-period interrupt and an alarm interrupt are generated at the same time.

The cases where either constant-period interrupts or alarm interrupts are enabled, or both interrupts are enabled but are not generated concurrently, are not affected.

3.2 Problem

When an INTRTC interrupt occurs under the above-mentioned condition, the RIFG flag of the RTCC1 register is set at the same time. The WAFG flag is set one subsystem clock (about 30.52 μs) after the occurrence of the INTRTC interrupt. Consequently, the WAFG flag may be read during INTRTC interrupt servicing without being set yet.

3.3 Temporary workaround (usage restriction)

If an INTRTC interrupt occurs under the above-mentioned condition, first check the interrupt status flag RIFG. If RIFG = 1 (a constant-period interrupt has occurred), check the WAFG flag after one subsystem clock (about 30.52 μs) has elapsed since the occurrence of the INTRTC interrupt. If RIFG = 0 (no constant-period interrupts have occurred), it does not need to wait for one subsystem clock before reading the WAFG flag.

3.4 Permanent workaround

The devices are being corrected so that the WAFG and RIFG flags are set at the same time as the above-mentioned INTRTC interrupt occurrence. See the *List of 78K0R/Kx3 Microcontroller Usage Restrictions* in attachment 1 for the products subject to correction.

4. Restriction on year, month, week, day, hour, minute and second count registers after real-time counter operation is stopped

4.1 Usage to which this restriction applies

This restriction applies when the real-time counter (RTC) is stopped (RTCE bit of RTCC0 register is cleared) when the count value of the sub-count register (RSUBC) reaches 7FFDH[Note] or 7FFEH[Note].

4.2 Problem

The RTCE bit is cleared to “0” under the above-mentioned condition, but the second count register (SEC) may not stop and continues to count up at the f_{SUB} cycles. In such a case, the minute, hour, day, week, month, and year count registers will also continue to count up.

4.3 Temporary workaround (usage restriction)

Before stopping the RTC (clearing the RTCE bit), first set the RWAIT bit of the RTCC1 register, and then confirm that the RWST flag is set to “1”. Before resuming the RTC operation, set the RTCE bit and then clear the RWAIT bit. This procedure stops RTC when the RTCE bit is cleared and thus prevents the SEC register from counting up.

4.4 Permanent workaround

The devices are being corrected so that the second count register (SEC) stops under the above-mentioned usage. See the *List of 78K0R/Kx3 Microcontroller Usage Restrictions* in attachment 1 for the products subject to correction.

Note 7FFDH ±correction value or 7FFEH ±correction value when watch error correction is performed

5. Restriction on DMA transfer termination

If a DMA transfer trigger occurs on channels 0 and 1 and the transfer on either channel ends (because it is forced to by software or automatically ends because the transfer has been executed the specified number of times) at the same time, the DMA transfer on the channel on which transfer has not stopped might be executed twice.

5.1 Usage to which this restriction applies (when a transfer is terminated forcibly by software)

This restriction applies if, when channels 0 and 1 are used, DMA transfer trigger occur on channels 0 and 1, and the transfer is terminated forcibly by software (by clearing the DSTn bit of the DRCn register) at the same time.
This restriction applies when these three sources occur at the same time, and does not apply if any of them does not occur. That is, this restriction does not apply if both channels are not used at the same time, and, even if both channels are used at the same time, this restriction does not apply if the DMA transfer is not terminated forcibly by software.
This restriction does not apply if the transfer trigger on the channel on which the transfer has not terminated forcibly is for the last transfer (when the DBCn register value is 0001H).

5.1.1 Problem

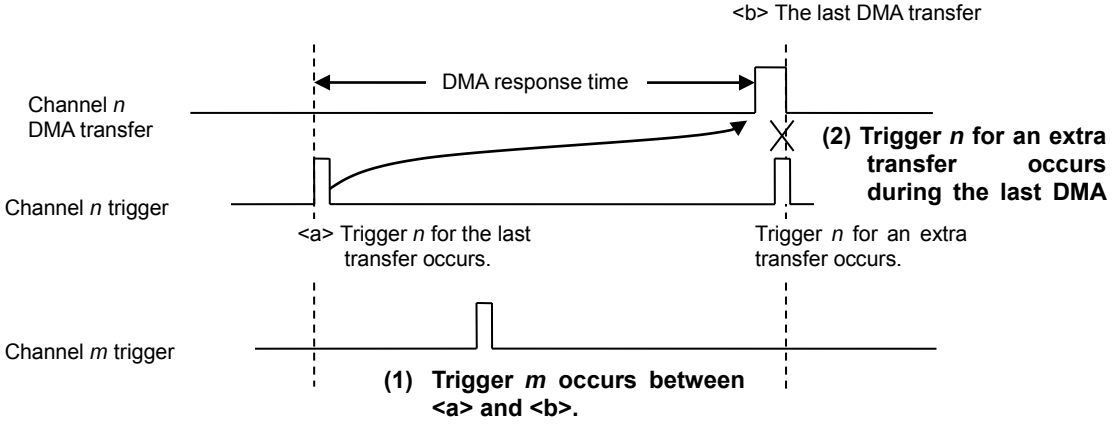
The DMA transfer on the channel on which the transfer is not terminated by clearing the DSTn bit might be executed twice in succession (one too many times), resulting in the DBCn register value specified for that channel being decremented by 2 (1 for each transfer).

5.2 Usage to which this restriction applies (when a transfer ends due to being completed the specified number of times)

This restriction applies if, when channels 0 and 1 are used, the conditions (1) and (2) below are satisfied when a DMA transfer is executed the specified number of times on channel n and then is completed.

Conditions:

(1) A DMA transfer trigger occurred on channel *m* at a time in the interval from when the last DMA transfer trigger on channel *n* occurred to when that transfer on channel *n* is completed.
(2) Another transfer trigger occurs on channel *n* during the last transfer on that channel.



This restriction does not apply if no transfer trigger occurs on channel *n* after the last transfer trigger occurred or if the trigger interval is specified as the DMA response time + at least 2 clock cycles, because the conflict described in (2) does not occur. This restriction also does not apply if the last transfer trigger occurred on channel *m* (when the DBCm register value is 0001H).

5.2.1 Problem

When (1) and (2) occur, the DMA transfer on channel *m* might be executed twice in succession (one too many times), resulting in the DBCm register value specified for channel *m* being decremented by 2 (1 for each transfer).

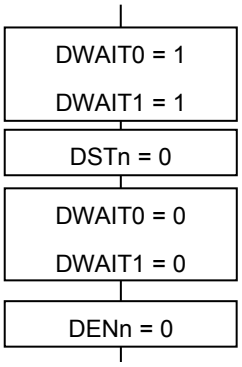
Remark (n, m) = (0, 1) or (1, 0)

5.3 Workaround (usage restriction)

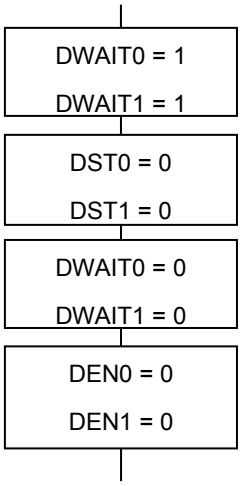
5.3.1 When a transfer is terminated forcibly by software

To terminate a DMA transfer by using software when two channels are used, set the DWAITn bit corresponding to each channel to hold the DMA transfer pending, clear the DSTn0 bit, clear the DWAITn bit for both channels to cancel the pending state, and then clear the DENn bit for both channels.

- Steps to terminate a transfer on either channel



- Steps to terminate transfers on both channels



Remark n = 0, 1

5.3.2 When a transfer ends due to being completed the specified number of times

Specify the interval between when transfer trigger occurs on a channel to be the maximum response time + at least 2 clock cycles. This restriction does not apply if the caution 3, which is described page 631 of the user's manual, is followed.

6. Restriction on holding a DMA transfer pending by using the DWAITn bit of the DMA controller

When DMA channels 0 and 1 are used and a DMA transfer on either channel is held pending by setting the DWAITn bit of the DMCn register, if another transfer trigger occurs for the transfer-pending channel and then a transfer trigger occurs on the other channel, the DMA transfer on the transfer-pending channel might be executed.

6.1 Usage to which this restriction applies

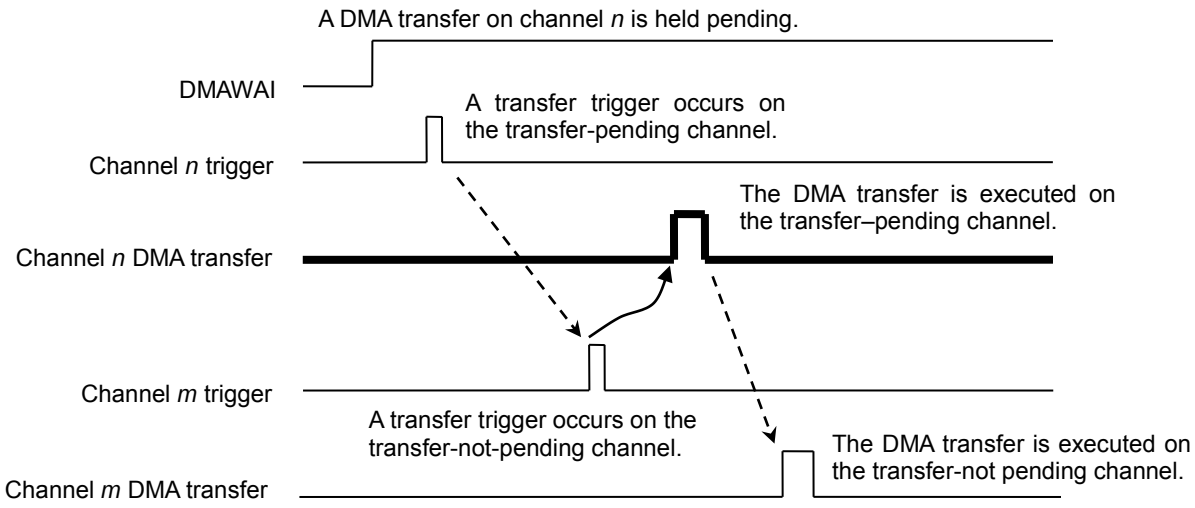
This restriction applies when DMA channels 0 and 1 are used, a DMA transfer on channel *n* is held pending by setting the DWAITn bit of the DMCn register, a transfer trigger occurs on channel *n*, and then transfer trigger occurs on channel *m*, on which a transfer is not held pending.

This restriction also applies when the same start source is specified as the transfer trigger for channels *n* and *m*, or transfer triggers occur at the same time on both channels.

This restriction does not apply when DMA transfers on both channels are held pending.

6.2 Problem

After a transfer trigger occurs on channel *m*, on which a transfer is not held pending, the DMA transfer on the transfer-pending channel *n* might be executed, and then the DMA transfer on channel *m* is executed. Only the DMA transfer on channel *m* should be executed. (The DMA transfer on channel n should be held pending.)



Remark (n, m) = (0, 1) or (1, 0)

6.3 Workaround (usage restriction)

To hold a DMA transfer pending by setting the DWAITn bit of the DMCn register when channels 0 and 1 are used, set the DWAITn bit for both channels.

Remark n = 0, 1

Attachment 1

List of 78K0R/Kx3 Microcontroller Usage Restrictions

		Conventional-Specification Products	Expanded-Specification Products	
Section	Description	KE3: μPD78F1142/F1143/ F1144/F1145/F1146 KF3: μPD78F1152/F1153/ F1154/F1155/F1156 KG3: μPD78F1162/F1163/ F1164/F1165/F1166/ F1167/F1168 KH3: μPD78F1174/F1175/ F1176/F1177/F1178	KE3: μPD78F1142A/ F1143A/F1144A/ F1145A/F1146A KF3: μPD78F1152A/ F1153A/F1154A/ F1155A/F1156A	KG3: μPD78F1162A/ F1163A/F1164A/ F1165A/F1166A/ F1167A/F1168A KH3: μPD78F1174A/ F1175A/F1176A/ F1177A/F1178A KJ3: μPD78F1184A/ F1185A/F1186A/ F1187A/F1188A
1	78K0R/Kx3 Restriction of P50 and P51 input access	○	○	×
2	Restriction on output level when the clock output and buzzer output controller is stopped	×	○	○
3	Restriction on simultaneous use of constant-period interrupt and alarm interrupt of real-time counter	×	○	○
4	Restriction on year, month, week, day, hour, minute and second count registers after real-time counter operation is stopped	×	○	○
5	Restriction on DMA transfer termination	×	×	×
6	Restriction on holding a DMA transfer pending by using the DWAITn bit of the DMA controller	×	×	×

Remark The meaning of each symbol is as follows.

×: Restriction applicable

○: Restriction not applicable