NEC

Customer Notification

78K0R/Kx3™

16-Bit Single-Chip Microcontroller

Operating Precautions

78K0R/KE3 Series
78K0R/KF3 Series
78K0R/KG3 Series
78K0R/KH3 Series
78K0R/KJ3 Series

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(2) "**PRODUCT(S)**" means any product developed or manufactured by or for NEC (as defined above).

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(A) Table of Operating Precautions

No.	Outline		μPD78F1142, μPD78F1143, μPD78F1144, μPD78F1145, μPD78F1146			
		Rev.	MP			
		Rank Note				
1	Clock Output/ Buzzer Output Controller (Technical Limitation)		×			
2	Simultaneous use of constant-period interrupt and alarm interrupt of the real-time counter (Technical Limitation)		×			
3	Stopping the real-time counter (Technical Limitation)		×			

✓: Not applicable
×: applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		μPD78F1152, μPD78F1153, μPD78F1154, μPD78F1155, μPD78F1156			
		Rev.	MP			
		Rank Note				
1	Clock Output/ Buzzer Output Controller (Technical Limitation)		×			
2	Simultaneous use of constant-period interrupt and alarm interrupt of the real-time counter (Technical Limitation)		×			
3	Stopping the real-time counter (Technical Limitation)		×			

✓: Not applicable
×: applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		μPD78F1162, μPD78F1163, μPD78F1164, μPD78F1165, μPD78F1166, μPD78F1167, μPD78F1168			
		Rev.	MP			
		Rank Note				
1	Clock Output/ Buzzer Output Controller (Technical Limitation)		×			
2	Simultaneous use of constant-period interrupt and alarm interrupt of the real-time counter (Technical Limitation)		×			
3	Stopping the real-time counter (Technical Limitation)		×			

✓: Not applicable
×: applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		μPD78F1174, μPD78F1175, μPD78F1176, μPD78F1177, μPD78F1178			
		Rev.	MP			
		Rank Note				
1	Clock Output/ Buzzer Output Controller (Technical Limitation)		×			
2	Simultaneous use of constant-period interrupt and alarm interrupt of the real-time counter (Technical Limitation)		×			
3	Stopping the real-time counter (Technical Limitation)		×			

✓: Not applicable
×: applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		μPD78F1184, μPD78F1185, μPD78F1186, μPD78F1187, μPD78F1188			
		Rev.	MP			
		Rank Note				
1	Clock Output/ Buzzer Output Controller (Technical Limitation)		×			
2	Simultaneous use of constant-period interrupt and alarm interrupt of the real-time counter (Technical Limitation)		×			
3	Stopping the real-time counter (Technical Limitation)		×			

✓: Not applicable
×: applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

(B) Description of Operating Precautions

No. 1	Clock Output/ Buzzer Output Controller (Technical Limitation)
	Details The level of the clock output/buzzer output may be kept high if a frequency-divided clock other than the original oscillation clock (f_{MAIN}, f_{SUB}) is selected for the output clock in the CKS register (by setting bits CSELn, CCSn2, CCSn1 and CCSn0) and the clock output and buzzer output are disabled (by clearing the PCLOEn bit). The level of the clock output/buzzer output must be low when the output is disabled, but in the usage mentioned above, the output stops at the level (high or low) for which the output was disabled. *Workaround:* Select the original oscillation clock (f_{MAIN}, f_{SUB}) in the CKS register after disabling the clock output and the buzzer output (by clearing the PCLOEn bit) by the software. Note that the output level will be low after a high pulse with a different width from the original one has been output. This issue is planned for correction. The product name after the correction will be μPD78F11xxA (**A-version**).

No. 2	Simultaneous use of constant-period interrupt and alarm interrupt of the real-time counter (Technical Limitation)
	Details When a constant-period interrupt and alarm interrupt are generated at the same time, the alarm detection status flag (WAFG) is set about 30.52 μs after the occurrence of the constant-period interrupt status flag (RIFG). When an INTRTC interrupt occurs under the above-mentioned condition, the RIFG flag of the RTCC1 register is set at the same time. The WAFG flag is set one subsystem clock (about 30.52 μs) after the occurrence of the INTRTC interrupt. Consequently, the WAFG flag may be read during INTRTC interrupt servicing without being set yet. *Workaround:* If an INTRTC interrupt occurs under the above-mentioned condition, first check the interrupt status flag RIFG. If RIFG = 1 (a constant-period interrupt has occurred), check the WAFG flag after one subsystem clock (about 30.52 μs) has elapsed since the occurrence of the INTRTC interrupt. If RIFG = 0 (no constant-period interrupts have occurred), it does not need to wait for one subsystem clock before reading the WAFG flag. This issue is planned for correction. The product name after the correction will be μPD78F11xxA (**A-version**).

No. 3	Stopping the real-time counter (Technical Limitation)

Details

If the real-time counter (RTC) is stopped (RTCE bit of RTCC0 register is cleared) when the count value of the sub-count register (RSUBC) reaches 7FFDH**Note** or 7FFEH**Note**, the count-up of the second, minute, hour, day, week, month, and year count registers may not stop.

Note

7FFDH ±correction value or 7FFEH ±correction value when watch error correction is Performed.

The RTCE bit is cleared to “0” under the above-mentioned condition, but the second count register (SEC) may not stop and continues to count up at the f_{SUB} cycles. In such a case, the minute, hour, day, week, month, and year count registers will also continue to count up.

Workaround:

Before stopping the RTC (clearing the RTCE bit), first set the RWAIT bit of the RTCC1 register, and then confirm that the RWST flag is set to “1”. Before resuming the RTC operation, set the RTCE bit and then clear the RWAIT bit. This procedure stops RTC when the RTCE bit is cleared and thus prevents the SEC register from counting up.

This issue is planned for correction. The product name after the correction will be μPD78F11xxA (**A-version**).

(C) Valid Specification

Item	Date published	Document No.	Document Title
1	August 2007	U17854EJ6V0UD00 or later	User's Manual 78K0R/KE3
2	August 2007	U17893EJ5V0UD00 or later	User's Manual 78K0R/KF3
3	June 2007	U17894EJ6V0UD00 or later	User's Manual 78K0R/KG3
4	September 2007	U18432EJ2V0UD00 or later	Preliminary User's Manual 78K0R/KH3
5	August 2007	U18417EJ2V0UD00 or later	Preliminary User's Manual 78K0R/KJ3

(D) Revision History

Item	Date published	Document No.	Comment
1	January 31, 2007	U18470EE1V0IF00	1st Release
2	January 14, 2008	U18470EE2V0IF00	1st Update 78K0R/KH3 Series and 78K0R/KJ3 Series added Item 1 Real-time counter, Reset sources, (Specification change) deleted New Item 1 added Items 2 to 4 added