Date: Jul. 28, 2011

RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan Renesas Electronics Corporation

| Product Category | MPU/MCU | Document No. | TN-78K-A001A/E | Rev. | 1.00 | |
|-----------------------|---|-------------------------|------------------------|---|------------------------|--|
| Title | Errata sheet 78K0/Lx3-M | Information Category | Technical Notification | | | |
| Applicable Product | 78K0/Lx3-M { μ PD78F8052, μ PD78F8053, μ PD78F8054, μ PD78F8055 } | Lot No. | Reference Document | 78K0/Lx3-M User's I Rev.2.00 R01UH0020EJ0200 (0 | Manual: F Oct. 2010 | |

I'll notify following corrections on a user's manual.

[Location of errors]

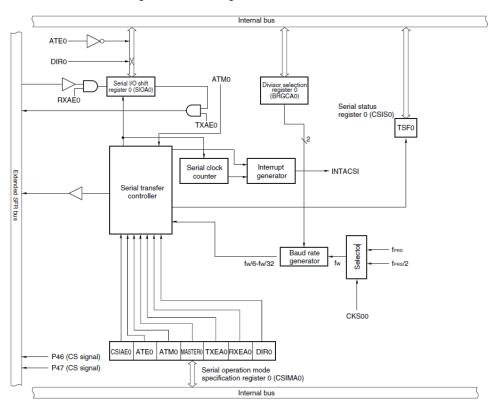
| Page | Item | No. |
|-------|---------------------------------------|-----|
| p.439 | CHAPTER 17 Figure 17-1. | (1) |
| p.441 | CHAPTER 17 Figure 17-3. | (2) |
| p.657 | CHAPTER 26 RESET FUNCTION Cautions 4. | (3) |
| p.740 | CHAPTER 33 ELECTRICAL SPECIFICATIONS | (4) |
| - | DC Characteristics(6/6) Notes 4. | |

Date: July 28, 2011

[Description]

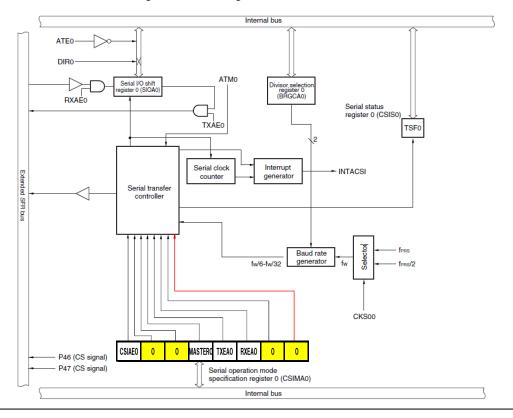
Error (1) CHAPTER 17 Figure 17-1.

Figure 17-1. Block Diagram of Extended SFR Interface



Correct(1)

Figure 17-1. Block Diagram of Extended SFR Interface



Error (2) CHAPTER 17 Figure 17-3.

Figure 17-3. Format of Serial Status Register 0 (CSIS0)

Address: FF91H After reset: 00H R/WNote1

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---|-------|---|---|---|---|---|------|
| CSIS0 | 0 | CKS00 | 0 | 0 | 0 | 0 | 0 | TSF0 |

| CSIAE0 | Control of extended SFR interface operation enable/disableNote 2 | | | | |
|--------|--|--------------|--------------------------|---------------|--|
| | | fprs = 2 MHz | f _{PRS} = 5 MHz | fprs = 10 MHz | |
| 0 | fPRS ^{Note 3} | 2 MHz | 5 MHz | 10 MHz | |
| 1 | fprs/2 | 1 MHz | 2.5 MHz | 5 MHz | |

| TSF0 | Transfer status detection flag | | |
|------|---|--|--|
| 0 | Bit 7 (CSIAE0) of serial operation mode specification register 0 (CSIMA0) = 0 | | |
| | At reset input | | |
| | At the end of the specified transfer | | |
| 1 | During data transfer | | |

Correct(2)

Figure 17-3. Format of Serial Status Register 0 (CSIS0)

Address: FF91H After reset: 00H R/WNote1

 Symbol
 7
 6
 5
 4
 3
 2
 1
 0

 CSIS0
 0
 CKS00
 0
 0
 0
 0
 0
 TSF0

| CKS00 | Control of extended SFR interface operation enable/disableNote 2 | | | | |
|-------|--|--------------|--------------------------|---------------|--|
| | | fprs = 2 MHz | f _{PRS} = 5 MHz | fprs = 10 MHz | |
| 0 | fPRS ^{Note 3} | 2 MHz | 5 MHz | 10 MHz | |
| 1 | fPRS/2 | 1 MHz | 2.5 MHz | 5 MHz | |

| TSF0 | Transfer status detection flag | | |
|------|---|--|--|
| 0 | • Bit 7 (CSIAE0) of serial operation mode specification register 0 (CSIMA0) = 0 | | |
| | At reset input | | |
| | At the end of the specified transfer | | |
| 1 | During data transfer | | |

Error (3) CHAPTER 26 RESET FUNCTION Cautions 4.

Cautions 1. For an external reset, input a low level for 10 μ s or more to the RESET pin.

- 2. During reset input, the X1 clock, XT1 clock, internal high-speed oscillation clock, and internal low-speed oscillation clock stop oscillating. External main system clock input becomes invalid.
- 3. When the STOP mode is released by a reset, the STOP mode contents are held during reset input. However, the port pins become high-impedance.
- 4. Extended SFRs are not reset by internal resets. To reset an extended SFR, set P17 to 1, clear it to 0, and then set it to 1 again.

Date: July 28, 2011

Correct(3)

- Cautions 1. For an external reset, input a low level for 10 μ s or more to the RESET pin.
 - 2. During reset input, the X1 clock, XT1 clock, internal high-speed oscillation clock, and internal low-speed oscillation clock stop oscillating. External main system clock input becomes invalid.
 - 3. When the STOP mode is released by a reset, the STOP mode contents are held during reset input. However, the port pins become high-impedance.
 - 4. Extended SFRs are not reset by internal resets. To reset an extended SFR, clear P17 to 0, set it to 1, and then clear it to 0 again.

Error (4)

- Notes 1. This includes only the current that flows through the watchdog timer (including the operating current of the 240 kHz internal oscillator). When the watchdog timer is operating, the current value of the 78K0/Lx3-M microcontrollers is obtained by adding Iwpt to the supply current (Ipp1, Ipp2, or Ipp3).
 - 2. This includes only the current that flows through the LVI circuit. When the LVI circuit is operating, the current value of the 78K0/Lx3-M microcontrollers is obtained by adding I_{LVI} to the supply current (I_{DD1}, I_{DD2}, or I_{DD3}).
 - 3. This includes only the current that flows through the successive approximation type A/D converter (AV_{REF}-AV_{ss}). When the successive approximation type A/D converter is operating in operation mode or HALT mode, the current value of the 78K0/Lx3-M microcontrollers is obtained by adding I_{ADC1} to the supply current (I_{DD1} or I_{DD2}).
 - 4. This includes only the current that flows through the ΔΣ-type A/D converter(AV_{DD}). When the ΔΣ-type A/D converter is operating in operation mode or HALT mode, the current value of the 78K0/Lx3-M microcontrollers is obtained by adding I_{ADC2} to the supply current (I_{DD1} or I_{DD2}).
 - 5. This includes only the current that flows through the LCD controller/driver. Not including the current that flows through the LCD divider resistor. The current value of the 78K0/Lx3-M microcontrollers is obtained by adding the LCD operating current (ILCD1 or ILCD2) to the supply current (IDD1, IDD2, or IDD3).

Correct(4)

- Notes 1. This includes only the current that flows through the watchdog timer (including the operating current of the 240 kHz internal oscillator). When the watchdog timer is operating, the current value of the 78K0/Lx3-M microcontrollers is obtained by adding IWDT to the supply current (IDD1, IDD2, or IDD3).
 - 2. This includes only the current that flows through the LVI circuit. When the LVI circuit is operating, the current value of the 78K0/Lx3-M microcontrollers is obtained by adding |LVI to the supply current (|IDD1, |IDD2, or |IDD3).
 - 3. This includes only the current that flows through the successive approximation type A/D converter (AV_{REF}-AV_{SS}). When the successive approximation type A/D converter is operating in operation mode or HALT mode, the current value of the 78K0/Lx3-M microcontrollers is obtained by adding I_{ADC1} to the supply current (I_{DD1} or I_{DD2}).
 - 4. This includes only the current that flows through the $\Delta \Sigma$ -type A/D converter (AV_{DD}=3.9mA, LV_{DD}=4.2mA). When the $\Delta \Sigma$ -type A/D converter is operating in operation mode or HALT mode, the current value of the 78KO/Lx3-M microcontrollers is obtained by adding I_{ADC2} to the supply current (I_{DD1} or I_{DD2}).
 - 5. This includes only the current that flows through the LCD controller/driver. Not including the current that flows through the LCD divider resistor. The current value of the 78K0/Lx3-M microcontrollers is obtained by adding the LCD operating current (ILCD1 or ILCD2) to the supply current (IDD1, IDD2, or IDD3).

