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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-32R-A081A/E	Rev.	1.00
Title	Error correction about DMAC of the hardware manual for 32180 Group, 32182 Group, 32185/32186 Group, 32192/32195/32196 Group		Information Category	Technical Notification		
Applicable Product	32180 Group, 32182 Group, 32185/32186 Group, 32192/32195/32196 Group	Lot No.	Reference Document	Hardware manual for the product left		

We will inform the correction of the contents of the DMAC chapter in the hardware manual of the above products.

When you use the hardware manual of the above products, should be used in conjunction with this document.

In addition, page numbers, and diagram numbers are described in Example 32185/32186 the group. For the number of table /figure and page of other products, please refer to the table on the last page.

<Corrections>
Page 9-49
We correct the following description of "Table 9.4.1 DMAC Related Registers That Can or Cannot Be Accessed for Write".

[Error]
Table 9.4.1 DMAC Related Registers That Can or Cannot Be Accessed for Write

Status	DMA transfer enable bit	DMA transfer request flag bit	DMA interrupt related registers	Other DMAC related registers
Transfer enabled	Can be accessed	Can be accessed	Can be accessed	Cannot be accessed
Transfer disabled	Can be accessed	Can be accessed	Can be accessed	Can be accessed

[Correction]
Table 9.4.1 DMAC Related Registers That Can or Cannot Be Accessed for Write

Status	DMA transfer enable bit	DMA transfer request flag bit	DMA interrupt related registers	Other DMAC related registers
Transfer enabled	Can be accessed with conditions (note 1)	Can be accessed with conditions (note 1)	Can be accessed	Cannot be accessed
Transfer disabled	Can be accessed	Can be accessed	Can be accessed	Can be accessed

(Note 1)
Can be accessed if one of the following conditions is met (cannot be accessed otherwise).
- The DMA transfer enable bit and DMA transfer request flag bit in the DMAn channel control register are both written to "1".
- These bits are written while no DMA transfer request is generated (Note 2).

(Note 2)
The DMA transfer request can be generated at any time, including while the DMA transfer request flag bit is read. Please use one of the following settings to disable the DMA transfer request while accessing to these bits.

[1] Set the LOCK bit in order not to accept the bus request from other than CPU
Execute the LOCK instruction to the dummy access area of SFR to set the LOCK bit. When the LOCK bit is set, it is disabled to accept the bus request from DMAC and other modules except for CPU. After setting the LOCK bit and writing to the DMAn channel control register 0, make sure to execute the UNLOCK instruction to the dummy access area in order to clear the LOCK bit. If a DMA transfer request is generated while the LOCK bit is set, it is accepted after the LOCK bit is cleared. Please refer to the "Supplementary Explanation for BSET, BCLR, LOCK and UNLOCK Instruction Execution" for LOCK/UNLOCK instructions and details of the LOCK bit.

[2] Make sure to stop operation of the DMA transfer request source not to generate the DMA transfer
Stop operation of the internal peripheral I/O which is selected for the DMA transfer request source. If the selected internal peripheral I/O is in operation, either stop its operation or disable the DMA transfer request output setting. Please note that the DMA transfer request may be accepted depending on the stop or disabling timing.

[3] Change the extended DMA transfer request source not to generate the DMA transfer request
When the extended DMA transfer request source is selected as a DMA transfer request source, change it to the internal peripheral I/O which does not generate the DMA transfer request. The extended DMA transfer request source select bit cannot be written while DMA transfer is enabled. The bit, however, can be written only if the bit is changed to the internal peripheral I/O which does not generate the DMA transfer request.

<Supplement>
Since there is no dummy access area of SFR in 32180/32182 group, address H'0080 0600 ~ H'0080 0603 can be used as a dummy access area. Writing to this area is invalid and reading from this area returns an undefined value. The write or read access to this area does not have any influence on the other SFR areas.

<Related Documents>

Product	Manual name, Document No.	Page number	Table No.
32180 Group,	32180 Group USER'S MANUAL Rev.1.00 (MEJ06B0048-0100Z)	Page 9-38	Table 9.4.1
32182 Group,	32182 Group User's Manual Rev.1.00 (REJ09B0014-0100Z)	Page 9-38	Table 9.4.1
32185/32186 Group,	32185/32186 Group Hardware Manual Rev.1.10 (REJ09B0235-0110)	Page 9-49	Table 9.4.1
32192/32195/32196 Group	32192/32195/32196 Group Hardware Manual Rev.1.10 (REJ09B0123-0110)	Page 9-49	Table 9.4.1