Contents

List of Figures

List of Tables

1 SSOP14 Package

The ZSC31150 is available assembled in a SSOP14 (sales codes ZSC31150**G1-*) RoHS-compliant package (5.3mm body) with a lead-pitch of 0.65mm.

Package R_{th}: ~120W/K **Weight:** ≤ 0.3 g

Package Body Material: Low-Stress Epoxy

Lead Material: FeNi-Alloy or Cu-Alloy **Lead Finish:** Solder Plating **Lead Form:** Z-Bends

1.1. SSOP14 Package Dimensions

Figure 1.1 Package View

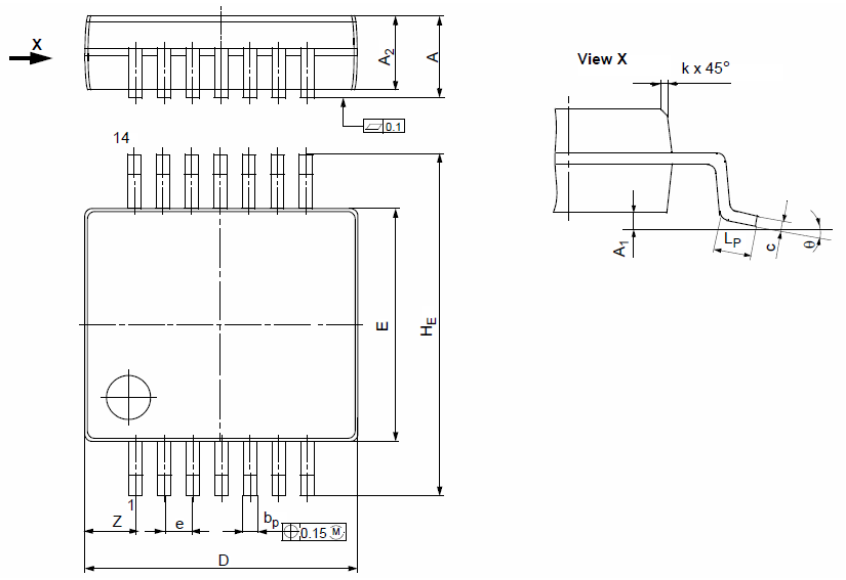


Table 1.1 Package Dimension

Package Dimensions					
Dimension	**Value**	**Dimension**	**Value**	**Dimension**	**Value**
A_{max}	1.99mm	c_{min}	0.09mm	H_{Emin}	7.65mm
A_{min}	1.73mm	c_{max}	0.20mm	H_{Emax}	7.90mm
$A1_{min}$	0.05mm	D_{min}*	6.07mm	k_{min}	0.25mm
$A1_{max}$	0.21mm	D_{max}*	6.33mm	LP_{min}	0.63mm
$A2_{min}$	1.68mm	E_{min}*	5.20mm	Z_{max}	1.22mm
$A2_{max}$	1.78mm	E_{max}*	5.38mm	θ_{min}	0°
b_{Pmin}	0.25mm	e_{nom}	0.65mm	θ_{max}	10°
b_{Pmax}	0.38mm	* without mold-flash			

1.2. SSOP14 Package Marking and Pin Assignments

Table 1.2 SSOP14 Package Marking

Top Side		Comments
1st Line	ZSC	
2nd Line	31150%$G1	% = Revision Identifier; $ = Temperature Range Identifier; example: ZSC31150AAG1
3rd Line	XXXXXXXX	Production Lot Number
4th Line	YYWW	Package Assembly Date: YEAR,YEAR,WEEK,WEEK

Table 1.3 Pin Assignments

Pin	Name	Description	Notes	Usage/ Connection [1)]	Latch-up Related Application Circuit Restrictions and/or Notes
1	VDDA	Positive analog supply voltage	Analog IO	Required/N.A.	
2	VSSA	Negative analog supply voltage	Analog IO	Required/N.A.	
3	SDA	I²C™* data IO	Digital IO, pull-up	N.A./VDDA	Trigger current/voltage to VDDA/VSSA: +/-100mA or 8/-4V
4	SCL	I²C™ clock	Digital IN, pull-up	N.A./VDDA	
5	N.C.	No connection			
6	VDD	Positive digital supply voltage	Analog IO	Required or open/N.A.	Only capacitor to VSSA is allowed; otherwise no application access
7	VDDE	Positive external supply voltage	Supply	Required/N.A.	Trigger current/voltage: -100mA/33V
8	VSSE	Negative external supply voltage	Ground	Required/N.A.	
9	AOUT	Analog output and one-wire Interface I/O	IO	Required/N.A.	Trigger Current/Voltage: -100mA/33V
10	VBN	Negative input sensor bridge	Analog IN	Required/N.A.	
11	VBR_B	Bridge bottom potential	Analog IO	Required/VSSA	Depending on application circuit, short to VDDA/VSSA possible
12	VBP	Positive input sensor bridge	Analog IN	Required/N.A.	
13	VBR_T	Bridge top potential	Analog IO	Required/VDDA	
14	IRTEMP	Temperature sensor and current source resistor	Analog IO	N.A./VDDA, VSSA	Depending on application circuit

1) **Usage**: If “Required” is specified, an electrical connection is necessary.
Connection: To be connected to this potential if not used or if no application/configuration-related constraints are given.
N.A.: Not applicable.

* I²C™ is a trademark of NXP>

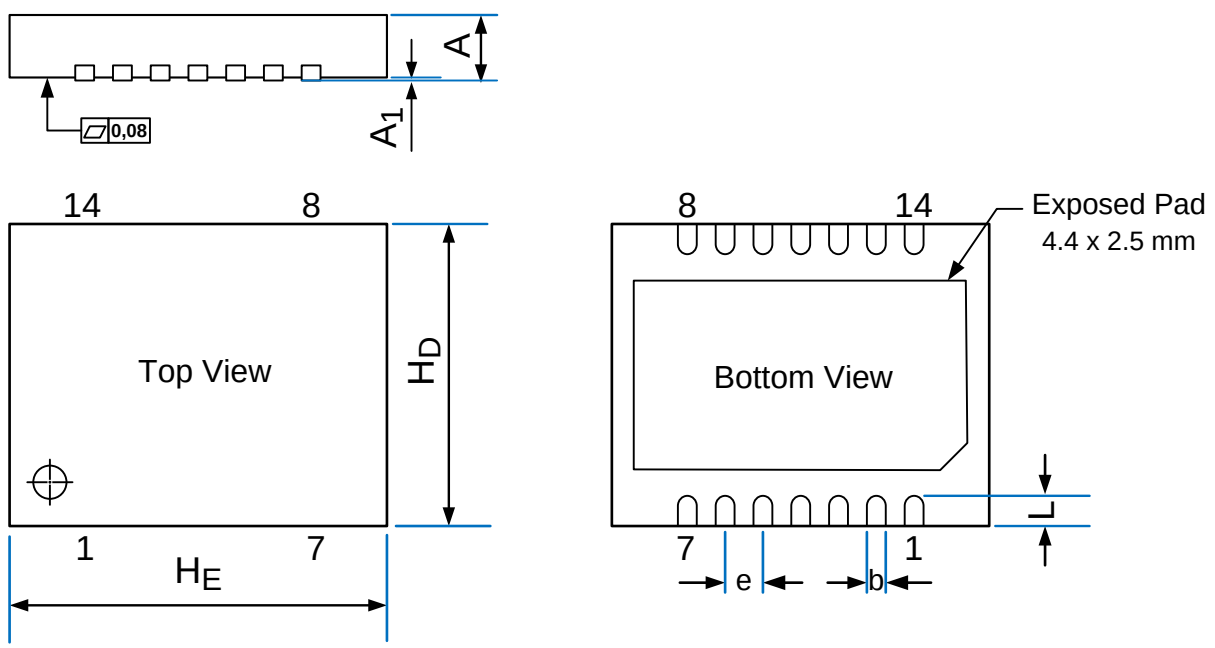
2 DFN14 Package

The ZSC31150 is also available assembled in a DFN14 package (sales codes ZSC31150**G2-*) with wettable flanks. For this package option, the pin assignments are the same as for the SSOP14 option.

2.1. DFN14 Package Dimensions

Figure 5.2 provides the dimensions for the DFN14 package option, which are based on JEDEC MO-229.

Figure 2.1 Outline Drawing for DFN14 Package with Wettable Flanks



Dimension	Minimum (mm)	Maximum (mm)
A	0.8	0.9
A_1	0	0.05
b	0.2	0.3
e	0.5 nominal	
H_D	3.9	4.1
H_E	4.9	5.1
L	0.3	0.5

2.2. Footprint and Wettable Flank Description

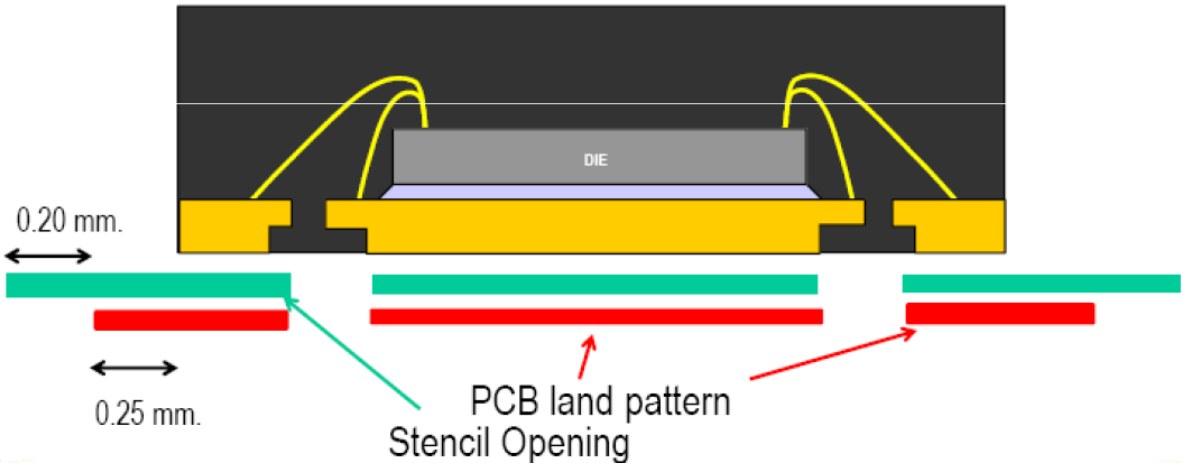
Figure 2.2 illustrates the general concept of the wettable flank (side plating), which allows automatic optical inspection when using the DFN14 package option.

Figure 2.2 Wettable Flank General Concept

Figure 2.3 illustrates a suggested footprint for printed circuit board (PCB) designs using the ZSC31150 DFN14.

- The exposed area of the ZSC31150 landing pattern is 0.25mm for the unit edge.
- The stencil opening excess is about 0.2mm from the landing pattern.

Figure 2.3 Footprint Dimensions for DFN14 with Wettable Flanks



2.3. DFN14 Package Marking

Table 2.1 DFN14 Package Marking

Top Side		Comments
1st Line	31150	
2nd Line	%$YWW	% = Revision Identifier; $ = Temperature Range Identifier; Y = Year (e.g., 4 for 2014, 5 for 2015, ...); WW = Workweek (e.g., 15)
3rd Line	XXXXX	Last five digits of IDT lot number

3 Pin Short-Circuit Information

Table 3.1 Pin Short-Circuit Description

Pin#	Name	Short to Pin	Behavior/Comment
1	VDDA	VSSA	Internal supply voltage is shorted with short current depending on the short resistance; abortion of signal conditioning functions if the reset threshold is reached by the resulting VDDA-VSSA potential. AOUT is switched to a high impedance condition (tri-state) in this case. Resulting alternating behavior of power on and off is possible.
2	VSSA	SDA	***No I²C™* communication:*** Current flow via the internal pull-up resistor (50kΩ). No effect on signal conditioning functions. ***I²C™ communication***: Communication abortion depending on short resistance. No internal current limitation.
3	SDA	SCL	***No I²C™ communication:*** Current flow via the internal pull-up resistor (50kΩ). No effect on signal conditioning function. ***I²C™ communication***: Communication abortion depending on short resistance. No internal current limitation.
4	SCL	n.c.	No effect on signal conditioning functions.
5	n.c.	VDD	No effect on signal conditioning functions.
6	VDD	VDDE	No effect on signal conditioning functions; protection function (overvoltage and reverse polarity) does not operate.
7	VDDE	VSSE	Abortion of signal conditioning functions if reset threshold is reached by resulting VDDA-VSSA potential. AOUT is switched to a high impedance condition (tri-state) in this case.

* I²C™ is a trademark of NXP.

Pin#	Name	Short to Pin	Behavior/Comment
8	VSSE	AOUT	AOUT current is limited to 20mA maximum. After activating the current limitation, the AOUT signal measured by the ECU is incorrect.
9	AOUT	VBN	The AOUT signal measured by the ECU is incorrect. Depending on short resistance, these failures can be detected in most cases by the built-in failsafe tasks SSC, SCC, and CMV (see section 7).
10	VBN	VBR_B	
11	VBR_B	VBP	
12	VBP	VBR_T	
13	VBR_T	IRTEMP	Wrong temperature measurement. Depending on the short resistance, failure can be detected by the built-in temperature sensor (TS) check failsafe task.
14	IRTEMP	VDDA	

4 Temperature Profile

ZSC31150*EG* and ZSC31150*AG* are qualified according to the AEC-Q100 automotive reliability standard.

ZSC31150*EG* is qualified to AEC-Q100 grade 0, which has a summed temperature stress rating of 1000h at 150°C.

ZSC31150*LG* is qualified according to AEC-Q100 grade 0 with an extended temperature stress of 5000h at 150°C.

ZSC31150*AG* is qualified for the same summed temperature stress, but the maximum temperature in applications is limited to 125°C (AEC-Q100 grade 1).

An actual temperature profile for an application can be checked by using the Arrhenius equation with a given temperature stress level of 1000h at 150°C or 5000h at 150°C. For these calculations, use an activation energy of 0.7eV.

Refer to calculation sheet *ZMDI Temperature Profile Calculation Sheet* for details.

5 Storage Conditions

For detailed information about storage conditions requirements, refer to the document *IDT Storage Conditions*. This document is included in all deliveries of packaged parts. It is also available upon request.

6 Related Documents

Document
ZSC31150 Feature Sheet
ZSC31150 Data Sheet
IDT Temperature Profile Calculation Sheet
*ZSC31150 Technical Note – Die and Pad Dimensions**
IDT Wafer Dicing Guidelines

Visit the ZSC31150 product page (www.IDT.com/ZSC31150) or contact your nearest sales office for the latest version of these documents.

* Note: Documents marked with an asterisk (*) are available upon request.

7 Glossary

Term	Description
AEC	Automotive Electronics Council
CMV	Common Mode Voltage Check
SCC	Sensor Connection Check
SSC	Sensor Signal Conditioner or Sensor Short Check, depending on context

8 Document Revision History

Revision	Date	Description
1.01	August 3, 2008	First revision of document.
1.02	November 29, 2010	Section for “Traceability” added. ZMD31151 removed. Changed to new IDT naming conventions and template.
1.03	August 16, 2011	Temperature profile for ZSC31150*LG1 (refer to section 4).
1.04	December 19, 2012	Update for package marking definitions. Minor edits and update for contact information.
1.05	January 28, 2013	Minor edits to illustrations for clarity.
1.06	February 11, 2014	Added wafer drawing and defined scribe line. Update for cover imagery and contact information.
1.07	April 6, 2014	DFN14 package and pin assignment added; temperature profile grades assigned according to the products. Corrections for pad names. Minor edits to “Related Documents” section.
1.10	April 29, 2014	Wettable flanks concept and PCB design recommendations added.
1.20	October 7, 2014	Temperature profile grades added for DFN packages. Minor edits for clarity. Updates for contact information.
1.30	November 24, 2015	Split revision 1.20 into separate documents for die (on-request only) and for SSOP14/DFN14 package specifications. Update for contact information.
	April 26, 2016	Changed to IDT branding.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.