RS-232/RS-485 Transceivers

Designing a 3-Wire, Half-Duplex, Dual Protocol Interface Using the ISL3330 and ISL3331

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Abstract

The ISL3330 and ISL3331 are dual protocol (RS-232/RS-485) transceivers that can be configured for a variety of operating modes. Many of these configurations require multiple bus and UART I/O lines that increase interface complexity.

This tech brief describes a special configuration of the dual mode transceivers, enabling them to support half-duplex transmission in RS-485 and RS-232 modes using the simplest interface design.

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1. Operating Modes

The ISL3330 and ISL3331 consist of a single differential RS-485 transmitter and receiver pair and two single-ended RS-232 transmitter and receiver pairs (Figure 1). The function matrix in Table 1 shows that in standard mode, the 485/$\overline{232}$ pin selects the desired protocol, the ON-pin enables the charge pump in RS-232 mode, and the RXEN and DEN pins turn the drivers on and off.

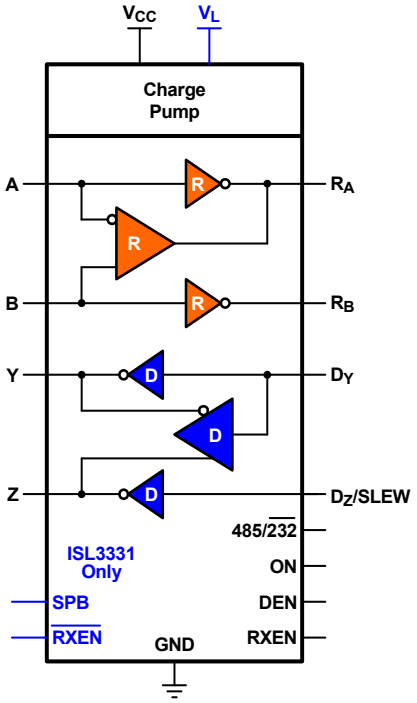

Figure 1. Block Diagram

Table 1. Function Table of the Dual Protocol Transceivers

Line #	Control Inputs					Receiver Outputs		Driver Outputs		Comments	Mode
	485/$\overline{232}$	ON	RXEN	DEN	Slew	R_A	R_B	Y	Z		
1	0	1	0	0	N/A	High-Z	High-Z	High-Z	High-Z	Drivers and Receivers Off	RS-232
2	0	1	0	1	N/A	High-Z	High-Z	On	On	Drivers On, Receivers Off	RS-232
3	0	1	1	0	N/A	On	On	High-Z	High-Z	Receivers On, Drivers Off	RS-232
4	0	1	1	1	N/A	On	On	On	On	Drivers and Receivers On	RS-232
5	0	0	0	1	N/A	High-Z	High-Z	On	High-Z	Single Driver On	RS-232
6	0	0	1	0	N/A	High-Z	On	On	High-Z	Single Driver and Receiver On	RS-232
7	0	0	1	1	N/A	On	On	On	On	Loopback	RS-232
8	X	0	0	0	X	High-Z	High-Z	High-Z	High-Z	Driver and Receiver Off	Shutdown
9	1	1	0	0	X	High-Z	High-Z	High-Z	High-Z	Driver and Receiver Off	RS-485
10	1	X	0	1	1/0	High-Z	High-Z	On	On	Driver On, Receiver Off	RS-485
11	1	X	1	0	X	On	High-Z	High-Z	High-Z	Receiver On, Driver Off	RS-485
12	1	1	1	1	1/0	On	High-Z	On	On	Driver and Receiver On	RS-485
13	1	0	1	1	1/0	On	High-Z	On	On	Loopback	RS-485

2. Half-Duplex Configuration

For true half-duplex operation the combination of certain control inputs as shown in Figure 3 and Table 1, Line 6 is required to activate an RS-232 sub mode, known as Single Transceiver mode.

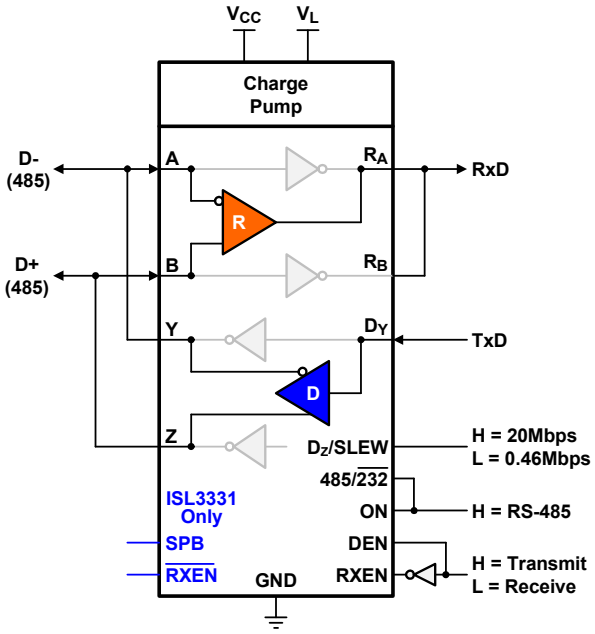

Figure 2. Half-Duplex Operation in RS-485 Mode

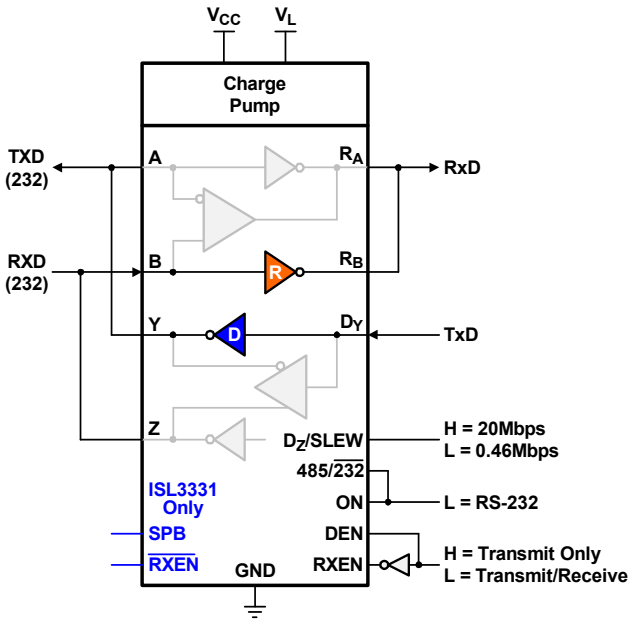

Figure 3. Half-Duplex Operation in RS-232 Mode

To establish a half-duplex bus, connect the inverting driver output (Y) with the inverting receiver input (A) and the non-inverting driver output (Z) with the noninverting receiver input (B). On the logic side, construct a single receive data output (RxD) by connecting R_A with R_B. This is necessary to support the single transceiver function in RS-232 mode. Finally, use the driver input (D_Y) as the single transmit data input for both protocols.

Applying logic high to the 485/$\overline{232}$ pin puts the device in RS-485 mode, disabling all RS-232 related drivers and receivers (Figure 2). To distinguish between transmit and receive operation, DEN is connected to RXEN through an inverter gate. This ensures that a high at DEN disables the 485 receiver and activates the driver to transmit data. Data entered at TxD leaves the device on the differential bus lines D+ and D-.

Asserting DEN low disables the driver and activates the receiver. Thus, differential data signals on the D+ and D- bus line enter the receiver at the A and B inputs and exit the device through the receiver output R_A onto the UART's receive data line, RxD. Both modes correspond to the RS-485 modes listed in the highlighted lines 10 and 11 of Table 1 on page 2.

Simply switching to RS-232 mode by turning 485/$\overline{232}$ low would activate both RS-232 driver and receiver pairs, and therefore connect each bus line with an active driver. In this case, the bus line connecting to an RS-232 driver at the other cable end would suffer bus contention. To prevent such a dilemma, the previously mentioned Single Transceiver mode is implemented. This mode is initiated by combining the ON pin with the 485/232 pin. When switching to RS-232 mode, both pins are low, which disables not only the RS-485 driver and receiver, but also the RS-232 driver of one pair and an RS-232 receiver of the other pair (Figure 3).

In this mode, the logic levels at RXEN and DEN determine whether the device is in Single Transmitter or Single Transceiver mode (meaning the driver is always enabled). Rather than toggling DEN between logic states (half-duplex operation), the user can choose to maintain DEN logic high to enable full-duplex transmission. Both modes correspond to the RS-232 modes listed in the highlighted lines 5 and 6 of Table 1.

3. Circuit Schematics

To ease the design of half-duplex dual protocol interfaces using the ISL3330 and ISL3331, Figures 4 and 5 show the circuit schematics for both transceivers. The ISL3330 comes in a 20 Ld TSSOP package and requires an external inverter gate for half-duplex operation.

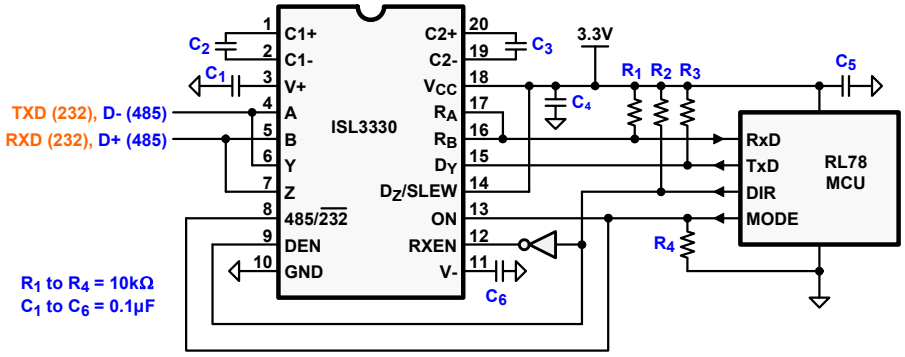

Figure 4. Half-Duplex Configuration for the ISL3330

The ISL3331 is available in a 40 Ld QFN package and includes two additional control pins, $\overline{RXEN}$ and SPB, as well as an internal level shifter for a reduced logic supply, V_L.

- $\overline{RXEN}$ can be directly connected to DEN, which eliminates the need for an external inverter. In this case however, RXEN must be connected to ground.
- In RS-485 mode, SPB allows the user to choose between the two slew-rate limited data rates of 115kbps and 460kbps, if D_Z/SLEW is low. The 115kbps rate uses even slower edge rates than the 460kbps version for EMI sensitive designs, to allow longer bus lengths, or to minimize the risk of termination issues on slower data rate networks. Asserting D_Z/SLEW high selects the high-speed mode of 20Mbps, and SPB has no impact.
- V_L is used to interface the ISL3331 to UARTs or microcontrollers that are powered by a supply voltage lower than 3.3V. Tying V_L to the lower supply voltage shifts the input thresholds and output voltages of the logic pins to values compatible with the lower supply (Figure 5).

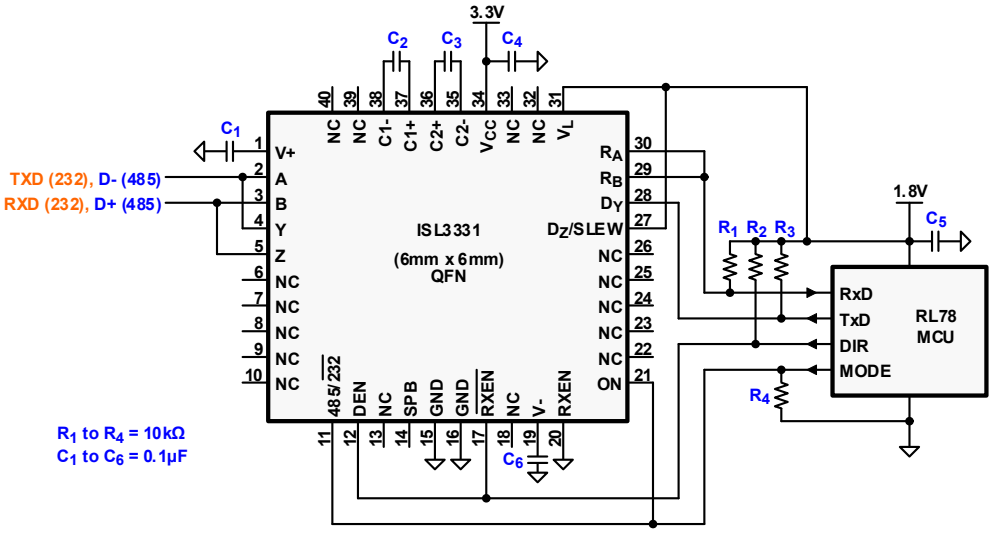

Figure 5. Half-Duplex Configuration for the ISL3331

4. Revision History

Rev.	Date	Description
1.01	Oct 25, 2019	Updated Figure 3. Updated Disclaimer.
1.00	May 16, 2018	Corrected typo for inputs A and B on Figure 3. Corrected typo “486/232” to “485/232” on page 3.
0.00	Mar 29, 2018	Initial release

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