Introduction

Certain Intersil ceramic packages include bottom metal or bottom heat sinks (also called heat slugs). When present, these features will be noted on Intersil's product datasheet Package Outline Drawings (POD). The POD includes the bottom metal or bottom heat sinks features and their dimensions. The bottom metal or heat sink provide for a direct thermal path out of the bottom of the package, which can significantly improve thermal performance.

Packages with such built-in thermal enhancements are generally based on styles such as ceramic quad flat-packs and ceramic dual flat-packs (see Figures 1 and 2). This tech brief provides guidance to help optimize the board design to take full advantage of such a package’s built-in thermal enhancements.

It should be emphasized that these guidelines are general in nature and should only be considered a starting point in this effort. The user must apply their actual experiences and development efforts to optimize designs and processes for their manufacturing practices and the needs of varying end-use applications.

General Design Guidelines for Thermally Enhanced Packages

The bottom metal or heat sink features are intended to be mounted directly to a matching “thermal land” pad pattern on the printed circuit board (PCB). The mounting should be accomplished using materials such as solder, thermal and or electrically conductive or non-conductive epoxy. Choice of mounting material may be affected by whether or not electrical connection between the package bottom and PCB is needed, by board assembly facility capabilities or various application requirements (temperature extremes involved, low out-gassing properties, etc.).

To take full advantage of the bottom heat-escape path, the board design should include thermal vias dropped down beneath the “thermal land” to one or more buried or back-side planes. This helps overcome the PCB’s base material’s relatively poor thermal conductivity.

The closer thermal coupling of the device to the buried planes results in more efficient heat spreading and more uniform temperature distribution across the board. This combination of vias for vertical heat escape and planes (and/or higher conductivity board material) for heat spreading, helps enable the IC device to achieve its full performance potential.
**Land Pattern Guidelines**

**Peripheral I/O Lands**

Packages with such built-in thermal enhancements are generally based on styles such as ceramic dual flat-packs and ceramic quad flat-packs and typically use the same peripheral I/O lead designs. These leads are generally formed with gull-wing shapes prior to soldering to the board.

For the peripheral I/O lands on the board, the standard design methodology (for packages without bottom metal or heat sinks) can be used. Note that the vertical level of the bottom of formed lead feet should:

- **In the case of solder-mounting of the base:** Peripheral I/O leads should be formed to coincide with the package bottom plane.
- **In the case of “thick” epoxy, etc. mounting of the base:** Peripheral I/O leads should be formed lower than the package bottom plane by an amount coinciding with the thickness of the base mounting material (i.e. so that the peripheral I/O leads will be allowed to sit fully down on their board I/O lands during solder reflow).

**Board Thermal Land**

The board thermal land (beneath the package’s bottom metal or heat sink), should have an X-Y size approximately the “same-size-as” to 0.2mm larger than the nominal bottom metal or heat sink size. If the base will be solder mounted, an overly large thermal land (and solder mask opening) should be avoided since this could adversely affect the “self-alignment” tendency of the package during solder reflow. See Figures 3 and 4 for examples of thermal land patterns with and without plugged vias.

**Thermal Vias**

A grid of 1.0mm to 1.2mm pitch thermal vias, which drop down and connect to the buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter, with the barrel plated to about 1.0 ounce copper. Use this type of via scheme, or similar designs as appropriate based on manufacturing capabilities or preferences.

Although adding more vias (such as by decreasing via pitch) will improve thermal performance, diminishing returns will be seen as more and more vias are added. Therefore, simply use as many vias as practical for the thermal land size and your board design ground rules.

**Solder Mask Design**

Two types of land patterns are used for surface mount packages:

- **Solder Mask Defined (SMD):** Solder mask openings smaller than metal pads.
- **Non-Solder Mask Defined (NSMD):** Solder mask openings larger than metal pads.

Better control of the copper etching process as compared to the solder masking process makes NSMD preferable. Also, the SMD pad definition can introduce stress concentrations near the solder mask overlap region that can result in solder joints cracking under extreme fatigue conditions. Using NSMD instead improves the reliability of solder joints as solder is allowed to “wrap around” the sides of the metal pads on the board.

For these reasons, NSMD is recommended for the perimeter I/O lands and generally for the thermal land as well.
Solder Masking of I/O Lands

For NSMD lands, the solder mask opening should be about 120mm to 150mm+ larger than the I/O land size, providing a 60mm to 75mm+ design clearance between the copper land and solder mask.

Typically each I/O land on the PCB should have its own solder mask opening with a web of solder mask between adjacent pads. The lead pitch of ceramic/metal packages is generally large enough to accomplish this. A less-preferred alternate method is to use one big opening, designed around a whole strip of I/O lands (for instance all the lands on one side of a package) with no solder mask in between them.

Solder Masking of the Thermal Land (for the case of solder mounting the package base)

For NSMD lands, the solder mask opening should be about 120µm to 150µm+ larger than the thermal land size, providing a 60µm to 75µm+ design clearance between the copper land and solder mask.

When the package bottom metal or heat sink is solder mounted, solder masking is also required for thermal vias to prevent solder wicking inside the vias, drawing solder away from the thermal land interface. The solder mask diameter should be about 100µm larger than the via diameter. The vias can be plugged or tented with solder mask, either from the bottom or top surface of the PCB (see Figure 3). Tenting from the top is considered a better option as it results in smaller voids under the die pad. Solder masking of vias from the bottom side can result in increased outgassing during reflow, creating bigger voids around vias. Note that small voids in this area are not unusual and will have little effect on thermal or electrical performance.

Stencil Guidelines

Stencil Design for I/O Lands

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing such optimized, reliable joints.

Stencil aperture size-to-land size should typically be a 1:1 ratio. For finer pitch parts, the aperture width may be reduced slightly if desired to help prevent solder bridging between adjacent I/O lands.

Stencil Design for Thermal Land (for the case of solder mounting the package base)

To reduce solder paste volume on the thermal land, it is recommended that an array of small paste dispensing apertures be used instead of one large aperture. The smaller apertures can be circular or square and of various dimensions and array sizes; but the main goal should be a dimensional combination that results in 50% to 80% solder paste coverage across the thermal land.

The thermal land's solder paste coverage should not be reduced too low since this could potentially affect “self-alignment” of the package during solder reflow and could contribute to increased solder voiding.

Stencil Type and Thickness

A laser-cut, stainless steel stencil with electro-polished trapezoidal walls is recommended. Electropolishing “smooths” aperture walls, resulting in reduced surface friction, good paste release and void reduction. Using a trapezoidal section aperture (TSA) promotes paste release and also forms “brick-like” paste deposits that assist in firm component placement.

A 0.15mm to 0.2mm stencil thickness is generally recommended for typical ceramic/metal packages.

Solder Paste and Reflow Profile

A system board reflow profile depends on the thermal mass of the entire populated board, so it’s not practical to define a specific soldering profile just for a specific package/product. Consult with paste manufacturers to choose a suitable solder paste type, and use a reflow profile appropriate for the specifics of the particular board design. Use the lowest practical peak reflow temperature which still provides for thorough solder reflow and good solder joint quality across the entire populated board.
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   - “Standard”: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, industrial robots, etc.

   - “High Quality”: Transportation equipment (automobiles, trains, ships, etc.), traffic control (traffic lights), large-scale communication equipment, key financial terminal systems, safety control equipment, etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implants, etc.), or may cause serious property damage (space systems; underwater vehicles; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the range specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified range.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain usage conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to, redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

© 2018 Renesas Electronics Corporation. All rights reserved.
Colophon 7.0