IDT CLOCKS FOR XILINX ULTRASCALE FPGAS

INTRODUCTION

IDT's high-performance synthesizer clock family and jitter attenuator + clock translator family, optimize customers' applications in key markets. These products are part of a portfolio specifically designed with ultra-low phase noise and jitter performance in mind. This makes them ideal for meeting the stringent timing requirements for Xilinx® UltraScale™ FPGAs used in communications, data center, industrial and broadcast video applications.

MEETING TOUGH PHASE NOISE REQUIREMENTS

Tables 1 and 2 below show the phase noise mask for the QPLL and CPLL Transceiver Ref Clock required by the Xilinx UltraScale FPGAs. In table 1, the specifications shown are for a reference clock of 312.5 MHz as defined by Xilinx, while table 2 calculates the requirements at 156.25 MHz by adjusting the 312.5 MHz specification in table 1 by 20*log (N/312.5), where N = 156.25 in this case.

Table 1

UltraScale Transceiver 312.5MHz Ref Clock PN Spec		
Carrier Offset	QPLL PN Spec (dBc/Hz)	CPLL PN Spec (dBc/Hz)
10 KHz	-105	-105
100 KHz	-124	-124
1 MHz	-130	-130
50 MHz	not spec.	-140

Table 2

UltraScale Transceiver 156.25MHz Ref Clock PN Spec		
Carrier Offset	QPLL PN Spec (dBc/Hz)	CPLL PN Spec (dBc/Hz)
10 KHz	-111	-111
100 KHz	-130	-130
1 MHz	-136	-136
50 MHz	not spec.	-146

IDT's third generation Universal Frequency Translator and FemtoClock® NG jitter attenuators and synthesizers, as well as VersaClock® 6 programmable clocks and XU crystal oscillators, are a perfect fit to meet the requirements set forth for these FPGAs. IDT's newest family of SyncE port synchronizers and SETS devices, including variants with an integrated DCO to support frequency and Phase/ToD synchronization via IEEE 1588 PTP packets, also meet the timing requirements for Xilinx UltraScale FPGAs.

Our portfolio includes devices which offer:

- Translations from virtually any input frequency to any output frequency
- Up to fourteen independently-programmable clocking outputs with the flexibility to generate many different frequencies
- Ultra-low phase jitter of less than 100 fs RMS (12 kHz to 20 MHz)
- SETS and 1588 DCO-enabled devices

These industry-leading, stand-alone devices deliver reliable, solid jitter performance in many different applications and provide jitter attenuation and consistent phase noise performance at any loop bandwidth setting. Table 3 shows select IDT devices that exceed Xilinx's specifications requirements.

Table 3

	RMS Phase Jitter (156.25 MHz, 12 KHz to 20 MHz)	# of Inputs, and Type	Input Frequency (MHz)	Outputs	Output Types	Output Voltage (V)	Output Frequency	Synthesizer Mode	Jitter Attenuator Mode	SETS (T0 DPLL), 1588 (DCO)
8T49NS010	84 fs	XTAL (or REF)	25 to 100	10	LVPECL	3.3	100 to 2500 (MHz)	✓	N/A	N/A
8T49N00x	228 fs	XTAL (or REF)	10 to 312.5	4, 6, 8	LVDS LVPECL	2.5, 3.3	15.16 to 1250 (MHz)	✓	N/A	N/A
8T49N285 8T49N286 8T49N287	<300 fs	XTAL (or two REF)	0.008 to 875	8	LVDS LVPECL HCSL LVCMOS	3.3, 2.5	0.008 to 1000 (MHz)	✓	✓	N/A
8T49N241 8T49N242	<300 fs	XTAL (or two REF)	0.008 to 875	4	LVDS LVPECL HCSL LVCMOS	3.3, 2.5	0.008 to 1000 (MHz)	✓	✓	N/A
82P33741	<300 fs (APLL3)	16 inputs SE and Diff	1 pps to 650 MHz	14	LVDS LVPECL LVCMOS	3.3	10/100/1000 Ethernet 10GE SONET/SDH WAN-PHY LAN-PHY	✓	✓	N/A
82P33731 82P33831	<300 fs (APLL3)	16 inputs SE and Diff	1 pps to 650 MHz	14	LVDS LVPECL LVCMOS	3.3	10/100/1000 Ethernet 10GE SONET/SDH WAN-PHY LAN-PHY	✓	✓	731 (DPLL) 831 (DPLL+ DCO)
5P49V6901	500 fs	XTAL or REF	1 to 350	4	LVDS LVPECL HCSL LVCMOS	3.3, 2.5, 1.8	1 to 350 (MHz)	✓	N/A	N/A
XUP, XUL Oscillators	300 fs	N/A	N/A	1	LVDS, LVPECL	3.3, 2.5, 1.8	0.016 to 1500 (MHz)	✓	N/A	N/A

Select IDT Devices that meet the Xilinx UltraScale™ Transceiver Phase Noise Specs

Tables 4a and 4b, below, highlight a direct comparison of the devices in table 3, above, versus the specifications for the Xilinx UltraScale FPGAs, while figure 1 shows the overall jitter performance of the 8V49NS0312 versus the specific jitter mask required for each Xilinx FPGA. These results clearly show that IDT's line of jitter attenuators and clock generators not only meets the requirements, but greatly exceed the requirements in all cases.

Table 4a

UltraScale™ Transceiver 312.5 MHz Ref Clock PN Spec			Synthesizers				
Carrier Offset	QPLL PN Spec (dBc/Hz)	CPLL PN Spec (dBc/Hz)	5P49V6901 VersaClock® 6	8V49NS0312	8T49NS1012	8T49NS010	8T49N00x
10 KHz	-105	-105	-118.6	-130.6	-123.6	-130.8	-119.9
100 KHz	-124	-124	-125.4	-136.5	-128.7	-137.9	-125.0
1 MHz	-130	-130	-133.0	-151.9	-140.0	-151.7	-134.0
50 MHz	not spec.	-140	-150	-158.1	-150	-158.5	-151
RMS Phase Jitter (10 KHz to 1 MHz)	487 fs		265 fs	57fs	154 fs	52 fs	255 fs
			• 4 universal • 4 indep. freqs • low power • 24-QFN	• 12 LVDS/LVPECL • 4 indep. freqs • 64-QFN	• 12 universal • 9 indep. freqs • 72-QFN	• 10 copies • Diff (AC/DC) • 56-QFN	• 4/6/8 copies • LVDS or LVPECL • 32/40-QFN

Jitter Labs Phase Noise Calculator

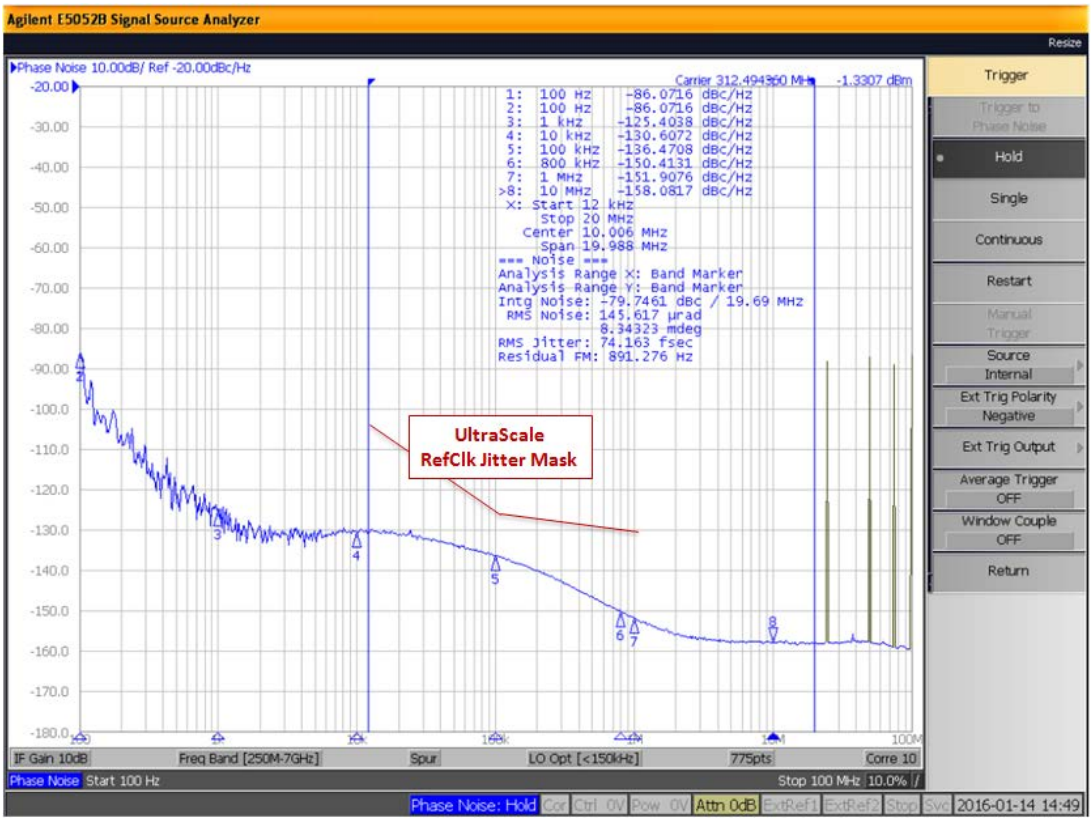
Table 4b

UltraScale™ Transceiver 312.5 MHz Ref Clock PN Spec			Synthesizer -or- JA + Translator			
Carrier Offset	QPLL PN Spec (dBc/Hz)	CPLL PN Spec (dBc/Hz)	8T49N28x Universal Frequency Translator 3G	8T49N24x Universal Frequency Translator 3G	82P33741 1588/SyncE Port Synchronizer	82P33731 (T0 DPLL) SyncE SETS 82P33831 (T0 DPLL + DCO) 1588/SyncE SETS
10 KHz	-105	-105	-122.4	-122.1	-124.9	-124.9
100 KHz	-124	-124	-128.8	-127.6	-128.3	-128.3
1 MHz	-130	-130	-140.8	-140.6	-133.3	-133.3
50 MHz	not spec.	-140	-153	-153	-154	-154
RMS Phase Jitter (10 KHz to 1 MHz)	487 fs		153 fs	167 fs	205.6 fs	205.6 fs
			• 8 universal output • 4 indep. freqs • 2/4 inputs (JA) • 56/72-QFN	• 4 universal outputs • 4 indep. freqs • 2 inputs (JA) • 40-QFN	• 14 outputs, mix of SE and Diff • 3 indep. freq domains • 16 inputs (JA) • 1pps input sync, input skew ctl • 144-CABGA	• 14 outputs, mix of SE and Diff • 3 indep. freq domains • 16 inputs (JA) • '33831 (includes 1588 DCO) • 144-CABGA

Jitter Labs Phase Noise Calculator

IDT Performance @ 312.5 MHz vs. Xilinx Defined Mask

Figure 1



8V49NS0312 Phase Noise Plot at 312.5 MHz

CONCLUSION

IDT is the world leader in silicon timing solutions boasting the largest portfolio of devices with mixed I/Os, voltage levels and frequencies. IDT's broad portfolio of timing devices satisfies timing budget requirements for the serial transceivers in today's industry leading FPGA families. The third generation Universal Frequency Translator, Femtoclock NG, VersaClock 6, IEEE1588 and SyncE Port Synchronizers and SETS devices, and XU crystal oscillator families delivers the reliable, solid jitter performance required by Xilinx's line of UltraScale FPGAs. The high performance APLL design implemented in these devices not only helps meet, but also helps customers exceed the requirements in most cases, adding margin and reliability to their design. This allows designers to worry less about the timing portion of their design, freeing their time up to focus attention on other areas of concern. This is just another reason why IDT consistently delivers extraordinary value to its customers.