

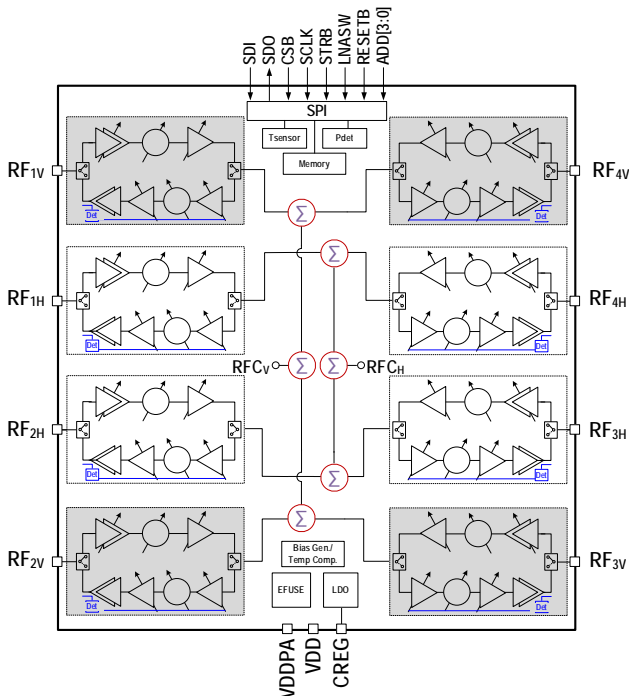
F5268

26GHz 8-Channel, Half-Duplex Transceiver IC

The F5268 is an 8-channel half-duplex transceiver (TRX) silicon integrated circuit (IC) designed using a SiGe BiCMOS process for dual-polarization 5G phased-array applications at the n258 band. The core IC has highly flexible gain and phase control on each channel to achieve fine beam steering and gain compensation between radiating channels.

The F5268 includes a standard SPI protocol that operates up to 95MHz with fast beam switching and fast beam-state loading. Up to 16 devices can be supported on the same SPI bus using dedicated address pins. Each device uses a 2.5V analog supply and a 2.5V–3.3V programmable PA supply to provide TX power modes. The digital core and SPI use a 1.8V supply generated by an on-chip LDO.

Block Diagram



Features

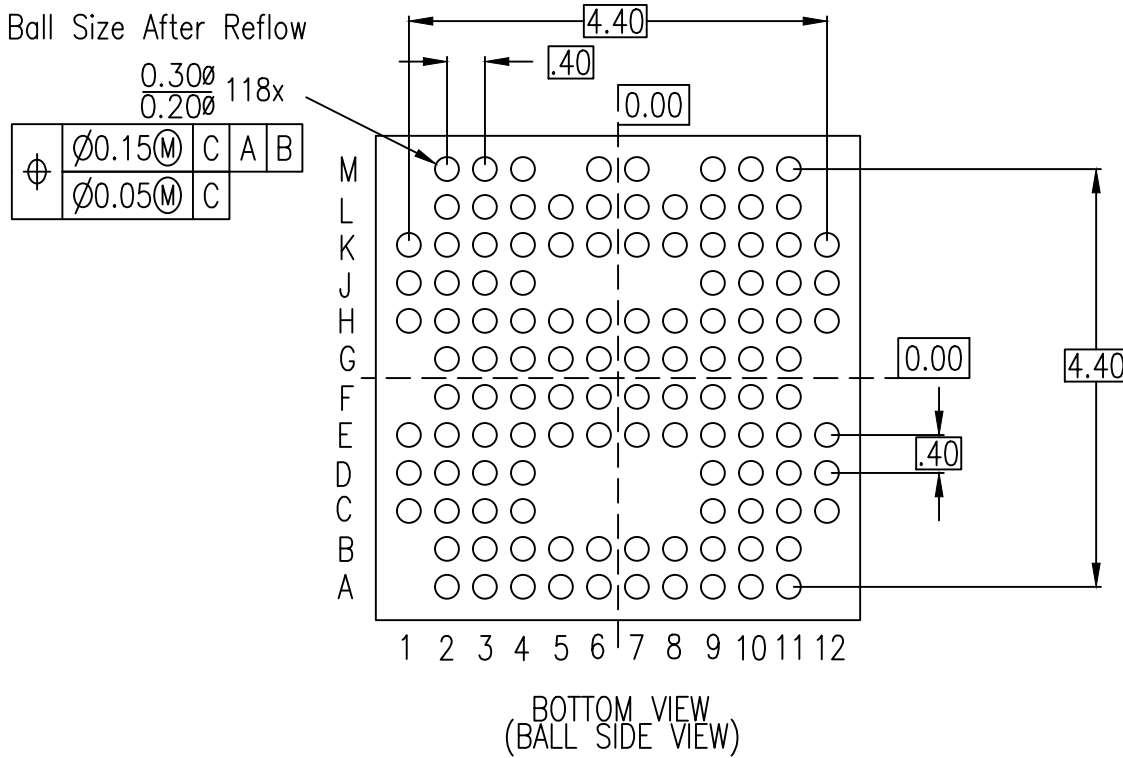
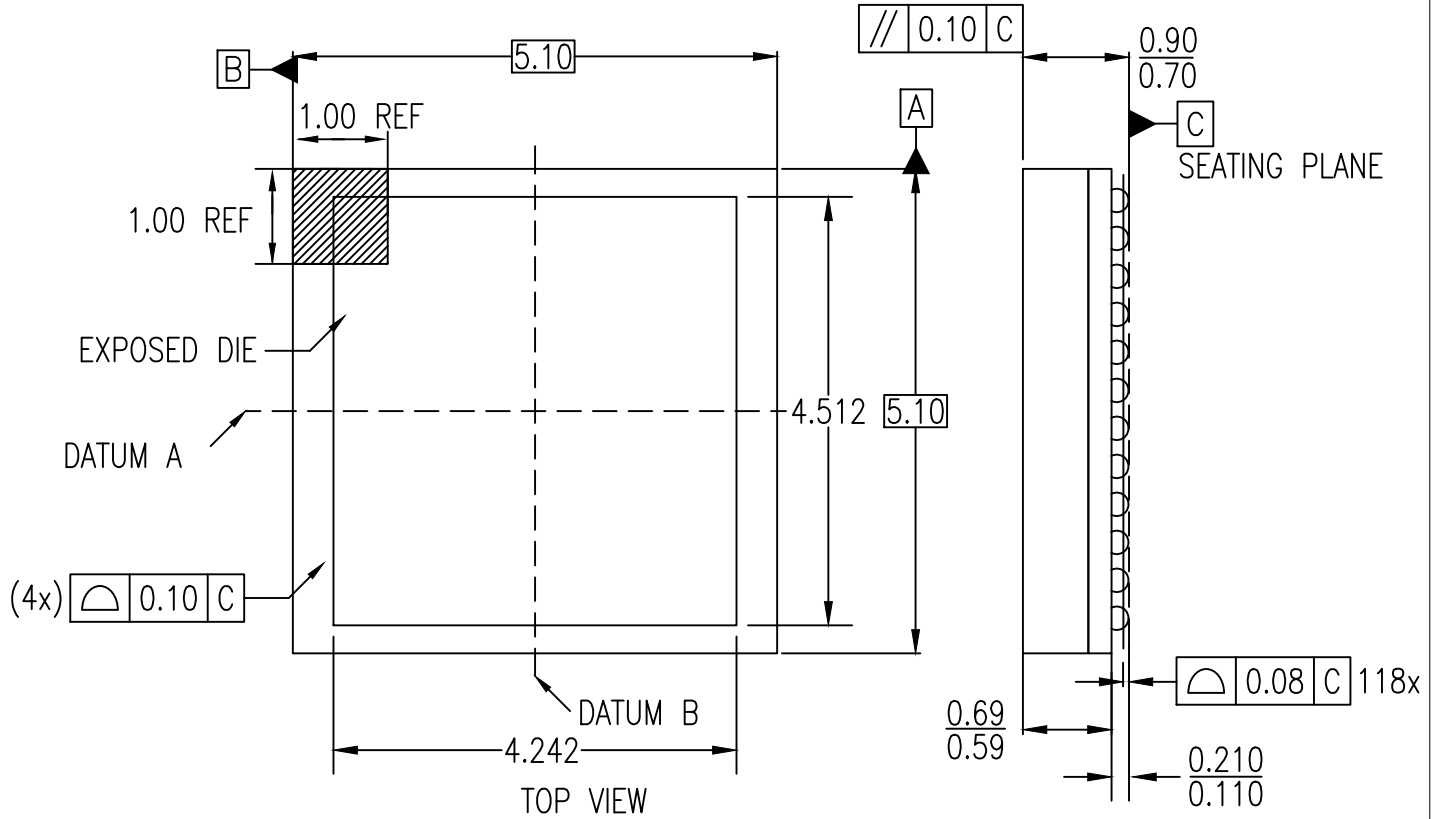
- 24.25GHz – 27.5GHz operation (5G NR n258)
- 8 radiation channels
- 100ns typical TX/RX mode switching time
- 20ns typical gain and phase settling time
- 1.2°/1.7° typical TX/RX RMS phase error
- 0.18dB/0.13dB typical TX/RX RMS gain step error
- 30.5dB gain attenuation range
- Integrated PTAT, PTAT2, and Bandgap generator
- Internal temperature sensor and power detector
- 4-bit chip address (hard-wired/programmable)
- Up to 95MHz SPI control
- 2048 on-chip programmable beam states
- Analog supply voltage: +2.4V to +2.6V
- Dedicated PA supply voltage: selectable between +2.4V to +2.6V and +3.0V to +3.3V
- 5.1 × 5.1 × 0.8 mm, 118-FCCSP package
- -40°C to +95°C operating temperature range

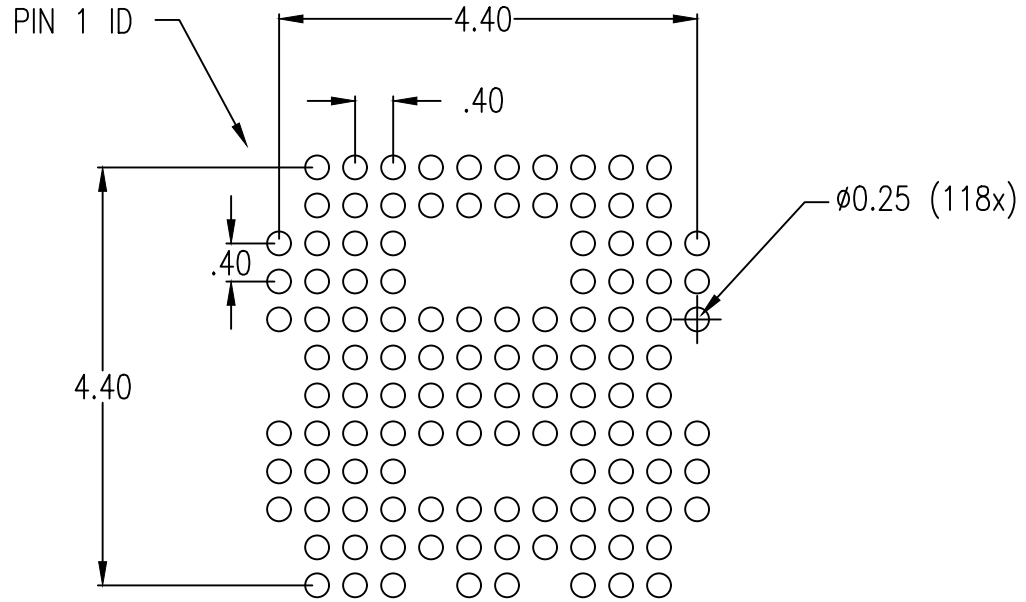
Applications

- 5G Single/Dual-Polarization Phased-Array Antenna System, Beam Steering, and similar applications

Ordering Information

Part Number	Package (mm)	Carrier Type
RA81F5268STGBX#BC0	5.1 × 5.1 × 0.8 <a href="#">118-FCCSP</a>	Tray
RA81F5268STGBX#HC0	5.1 × 5.1 × 0.8 <a href="#">118-FCCSP</a>	Reel
RTKA81F5268ST000RU	Eval. Board	-





RECOMMENDED LAND PATTERN DIMENSION  
(TOP VIEW)

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Oct. 26 2020	Rev 00	Initial Release

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(Disclaimer Rev.1.0 Mar 2020)

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