

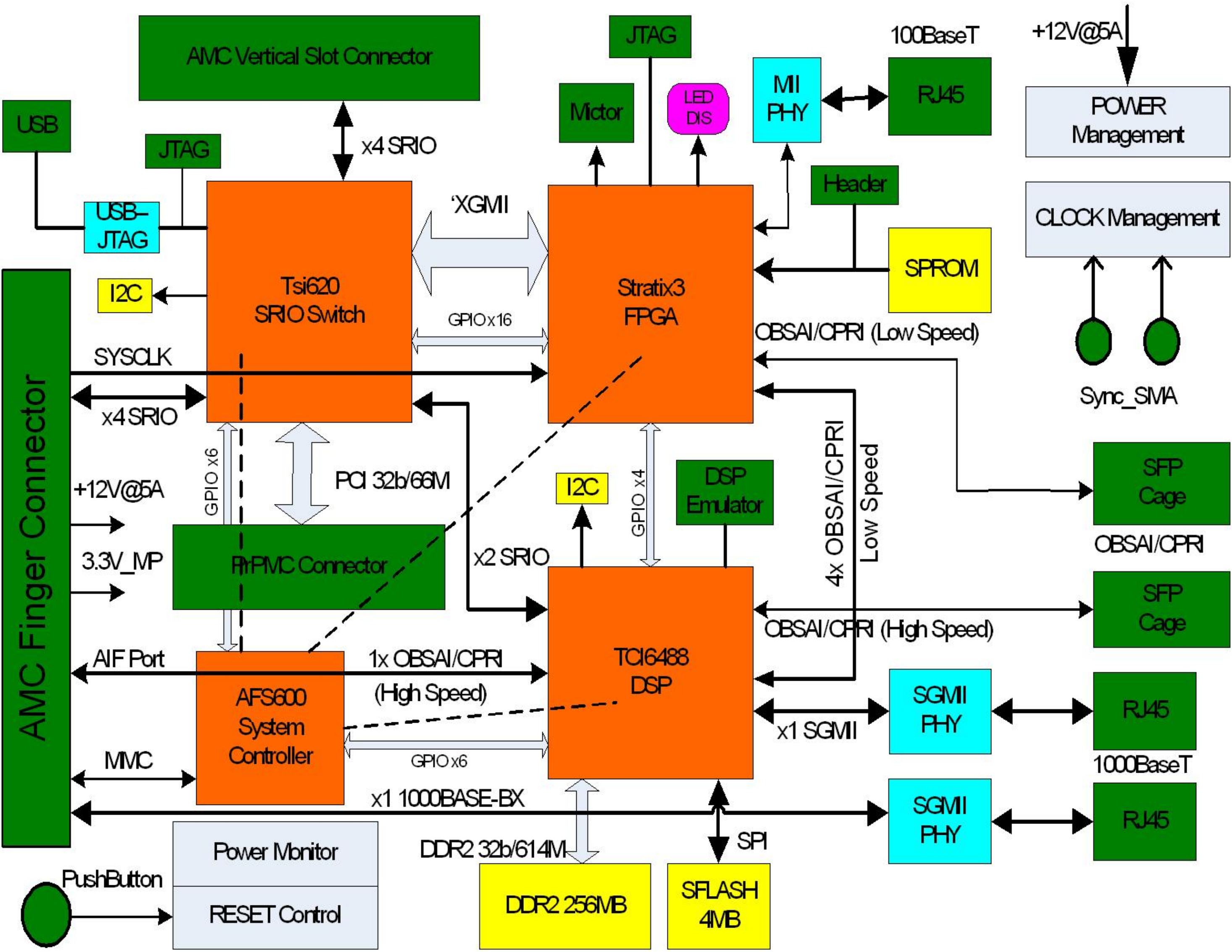
Tsi620 Evaluation Board Schematic

-Rev.1

Index

1. Function Block Diagram
2. Placement Illustration
3. AMC Connectors
4. Tsi620 - PCI I/F and sRIO Ports
5. PrPMC Module
6. Tsi620 - GPIO & MISC
7. Tsi620 - FPGA XGMII I/F
8. Tsi620 - Power & GND
9. Tsi620 - Decoupling
- 10.FPGA - AMC Clock, DSP GPIO, Frame Sync
- 11.FPGA - Tsi620 GPIO and LED Display
- 12.FPGA - RIO XGMII Interface
- 13.FPGA - Antenna Interface
- 14.FPGA - 100BaseT RJ45 & Configuration
- 15.FPGA - Power, GND, & Decoupling
- 16.DSP - AIF, sRIO, & SGMII Ports
- 17.DSP - DDR2 Memory Block
- 18.DSP - Configuration & Emulator
- 19.DSP - Power Supply & Decoupling
- 20.Antenna I/F SFP Connectors
- 21.AMC GigE SMGII PHY & RJ45
- 22.DSP GigE SGMII PHY & RJ45
- 23.USB I/F to Tsi620 JTAG
- 24.Clocking Distribution
- 25.Power - 5V & 3.3V
- 26.Power - FPGA 1.1V & DSP Core 1.1V
- 27.Power - 1.2V, 1.5V, 1.8V, & 2.5V
- 28.AFS600 - Digital Block
- 29.AFS600 - Analog Block
- 30.Power - 12Vin, Sequencing, Mangement Power

Function Block Digram



TITLE :

FUNCTION BLOCK DIAGRAM

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02	Rev 1	System Engineering

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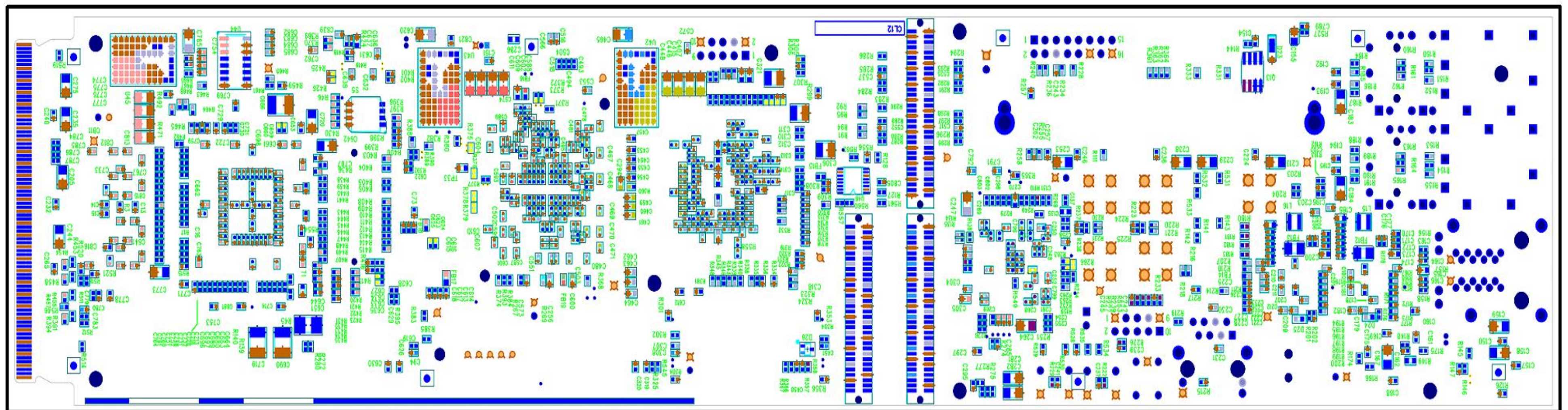
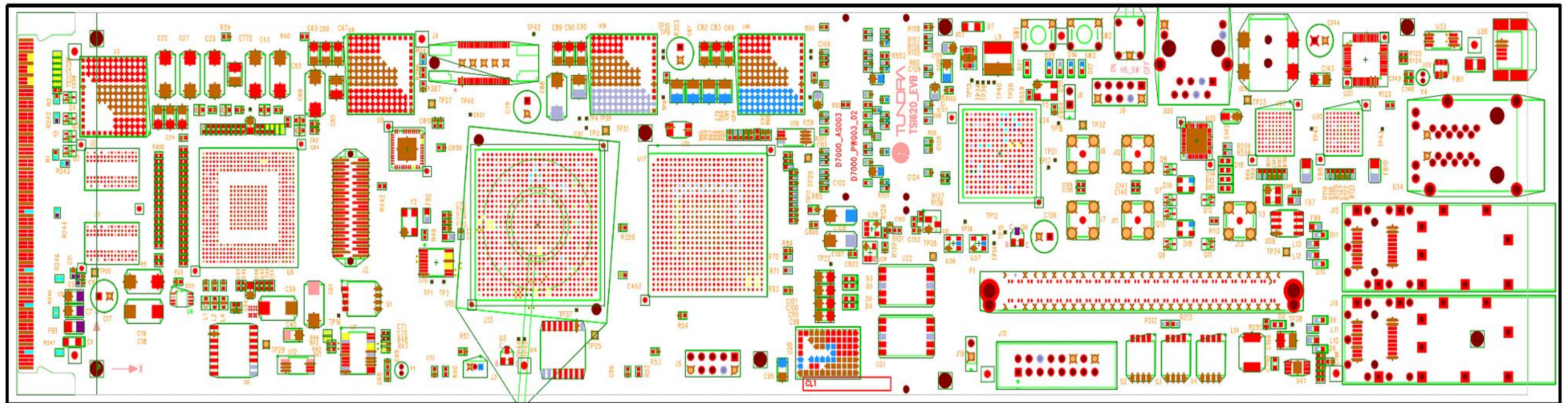
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1

OF

30

Components Placement Illustration



Revision Notes

-April 2nd, 2009: final editing for the customer release.



TITLE : **PLACEMENT ILLUSTRATION**

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60D7000	SC003_02	Rev 1	System Engineering

LAST MODIFIED DATE : 4-2-2009 14:17	SHEET 2 OF 30
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60D7000	SC003_02		System Engineering

LAST MODIFIED DATE : 3-30-2009_16:48 SHEET 4 OF 30

F

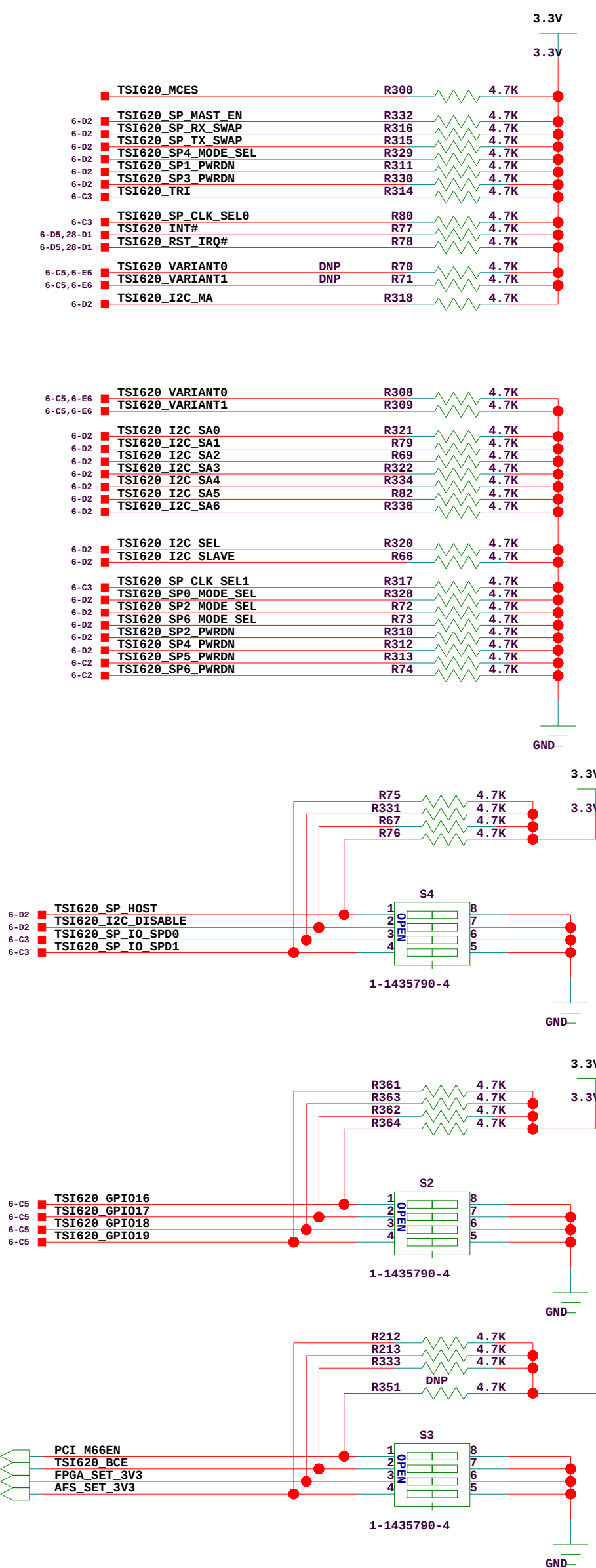


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TITLE :			
TSI620 GPIO & MISC			
SIZE C	DRAWING NUMBER : 60D7000_SC003_02	Version: Rev 0	DESIGNER : System Engineering
LAST MODIFIED DATE : 3-30-2009_16:48		SHEET	
		6 OF	

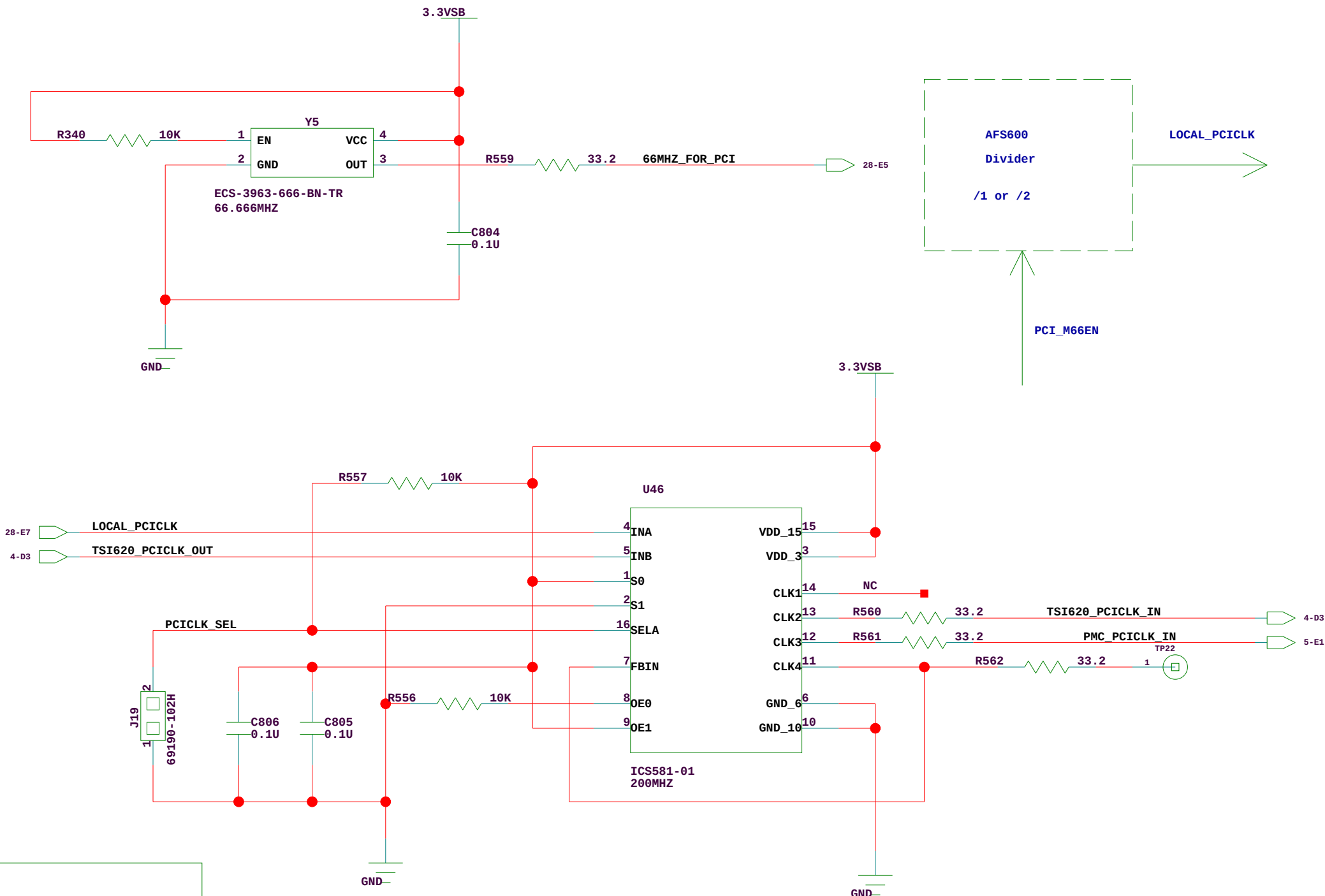
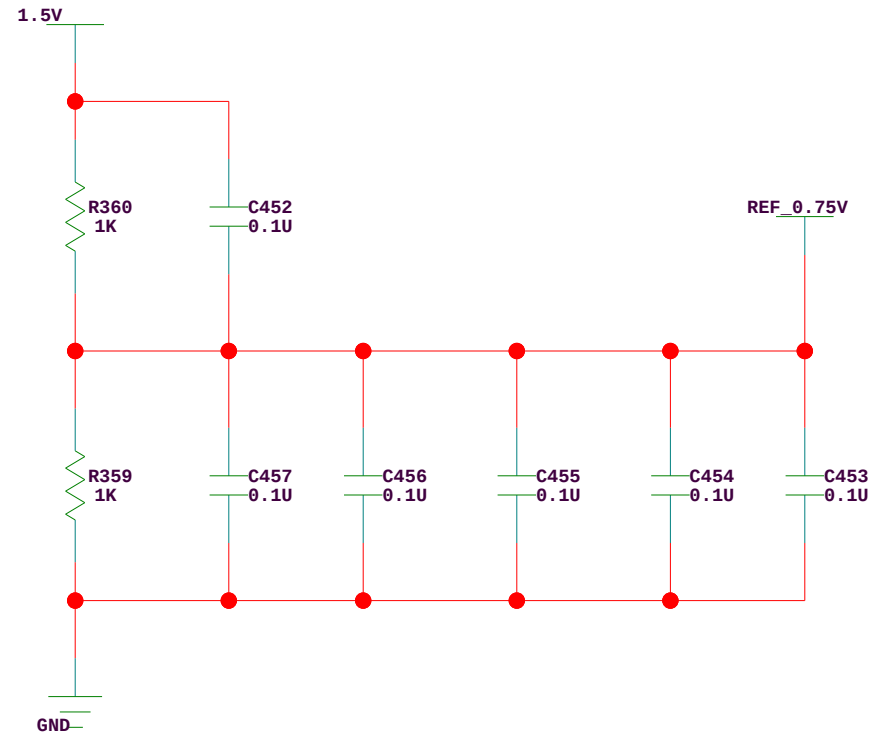
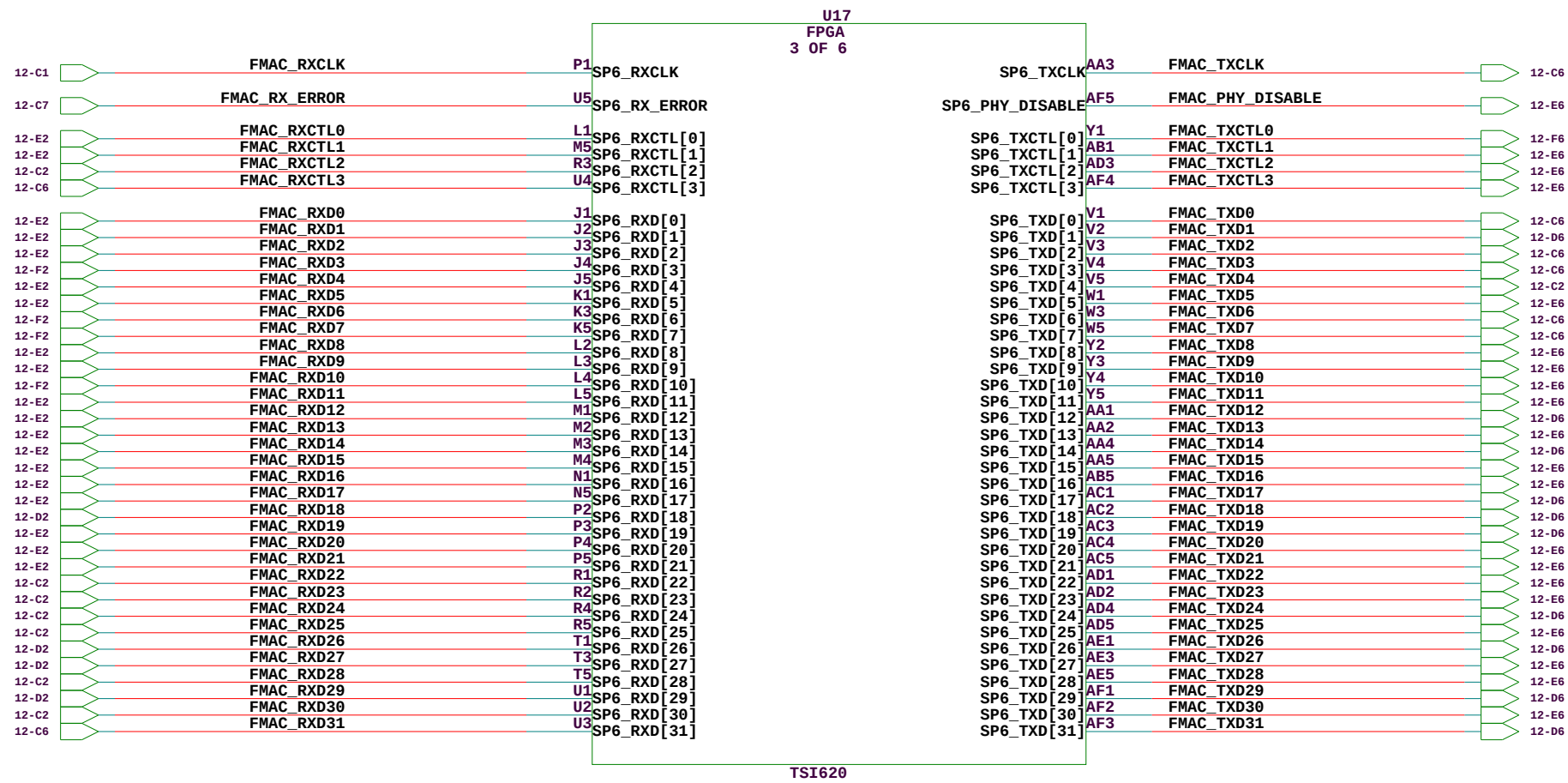


Tsi620 JTAG header only active when USB_RST# is low.

Tsi620 - FPGA XGMII Interface and PCI Clocking

Notes:

- 1) Tsi620 drives HSTL-15 Class-I output which is terminated on FPGA with parallel ODT.
- 2) Tsi620 recieves HSTL-15 Class-II from FPGA with source series ODT.



Notes:

- [1] S[1:0] = 01 : 19/75MHz
- [2] Jumper J19 OFF: Select INA



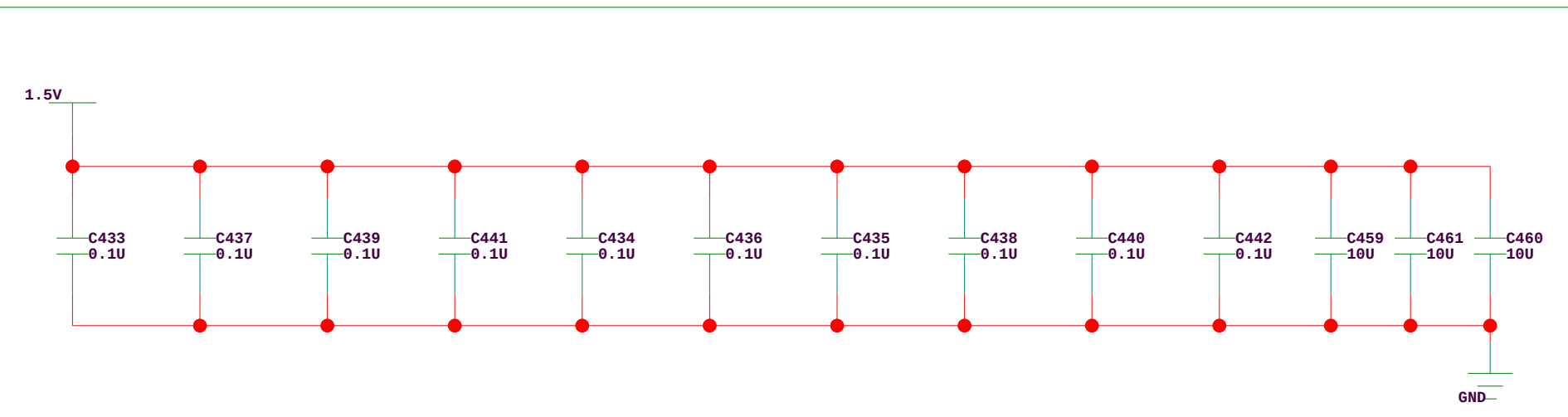
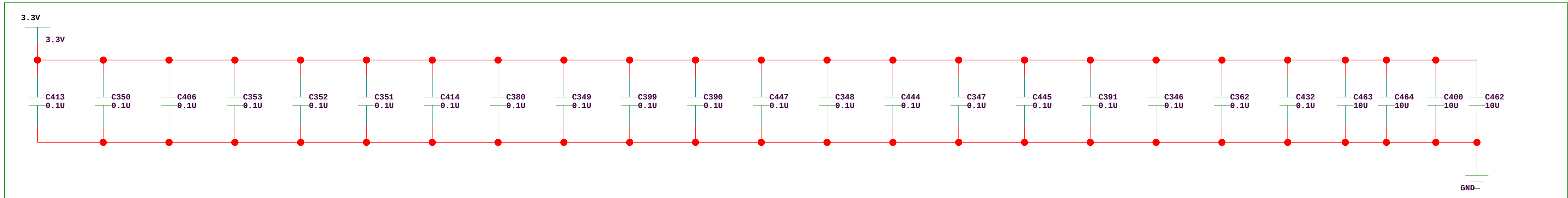
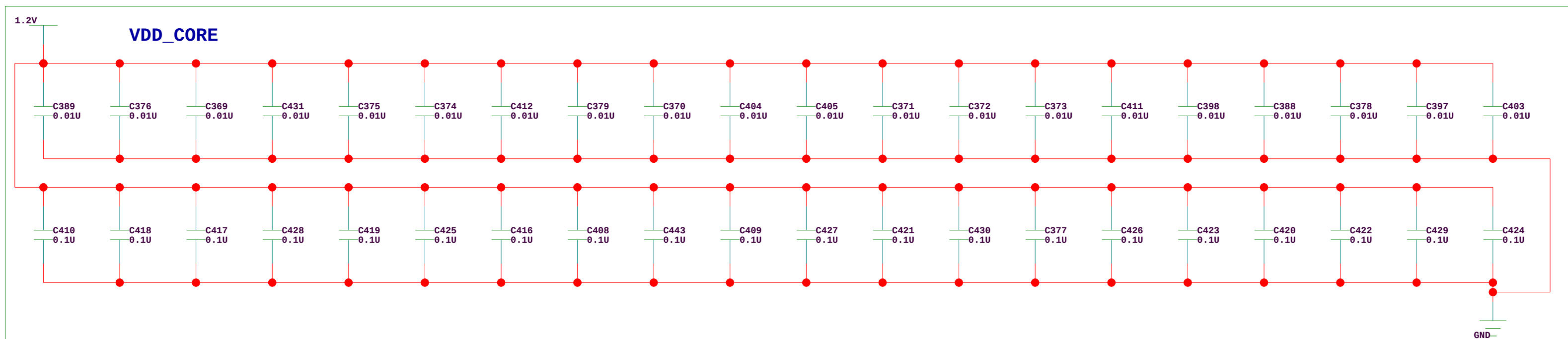
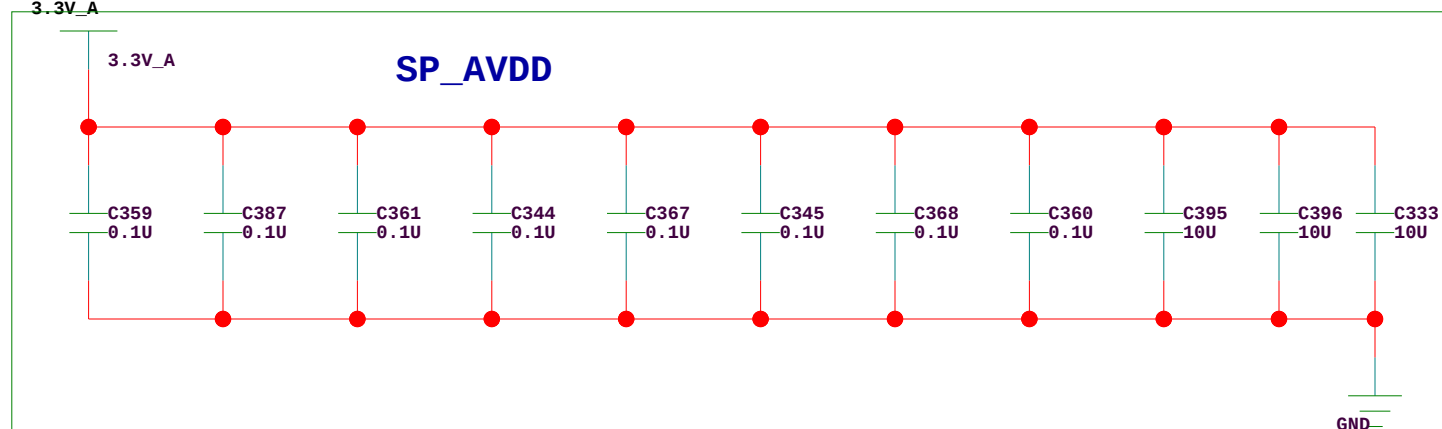
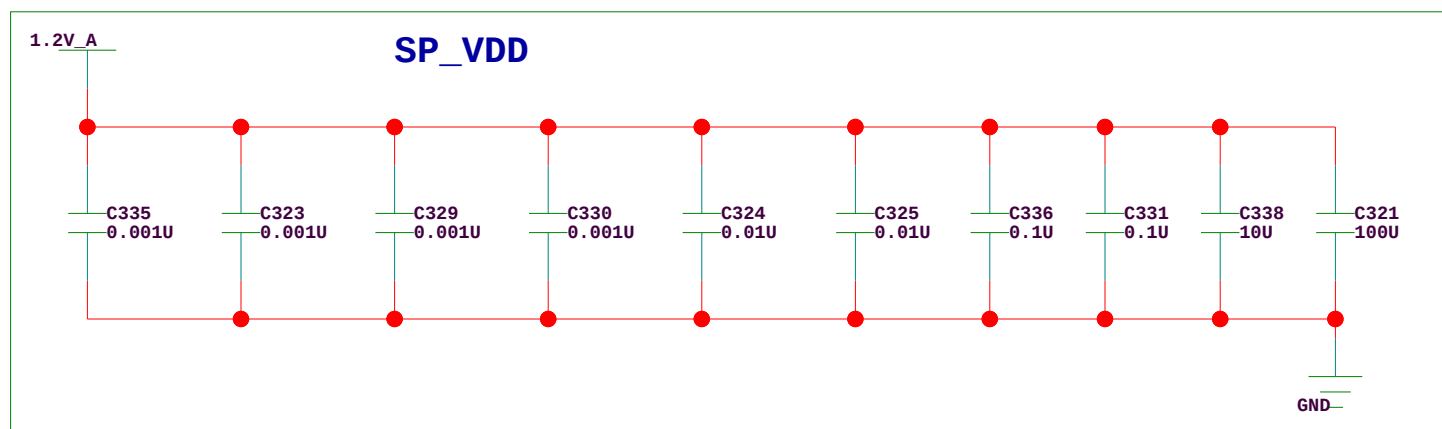
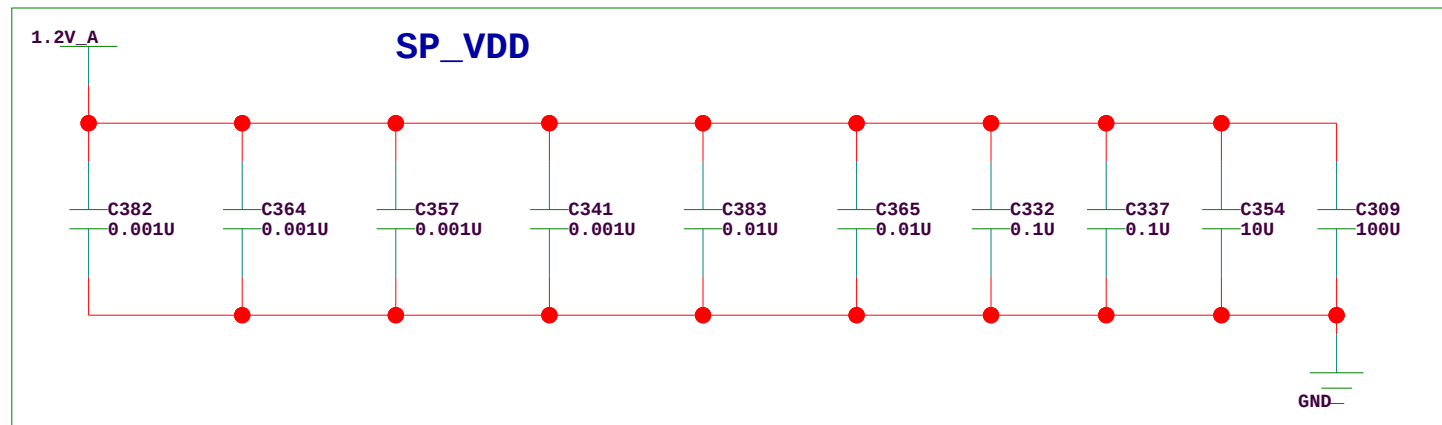
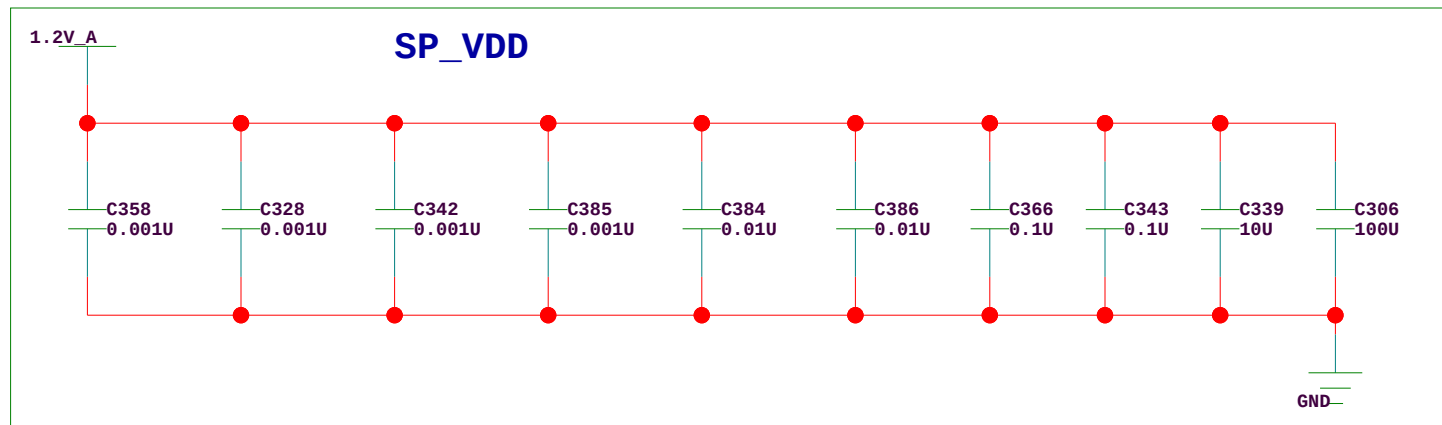
TITLE : TSI620 FPGA I/F & PCI_CLK

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02	Rev 0	System Engineering

LAST MODIFIED DATE : 3-30-2009_16:48 SHEET 7 OF 30

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02	Rev 0	System Engineering

Tsi620 - Decoupling



TITLE : TSI620 DECOUPLING			
SIZE C	DRAWING NUMBER : 60D7000_SC003_02	Version: Rev 0	DESIGNER : System Engineering
LAST MODIFIED DATE : 3-30-2009_16:48		SHEET 9 OF 30	

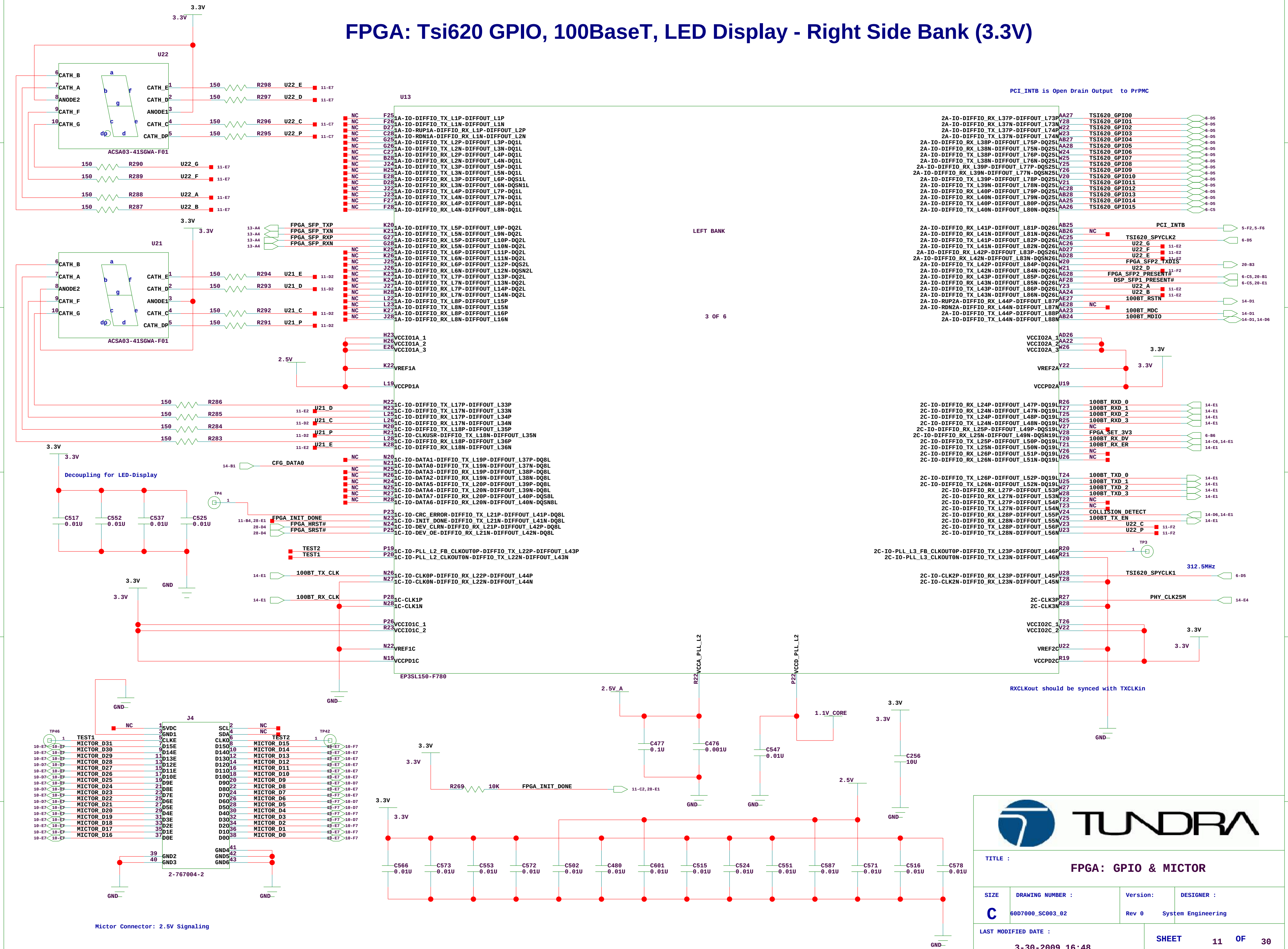
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SIZE C	DRAWING NUMBER : 6007000_SC003_02	Version:	DESIGNER : System Engineering
LAST MODIFIED DATE : 3-30-2009_16:48		SHEET 10 OF 30	

FPGA: Tsi620 GPIO, 100BaseT, LED Display - Right Side Bank (3.3V)





TITLE : **FPGA: GPIO & MICTOR**

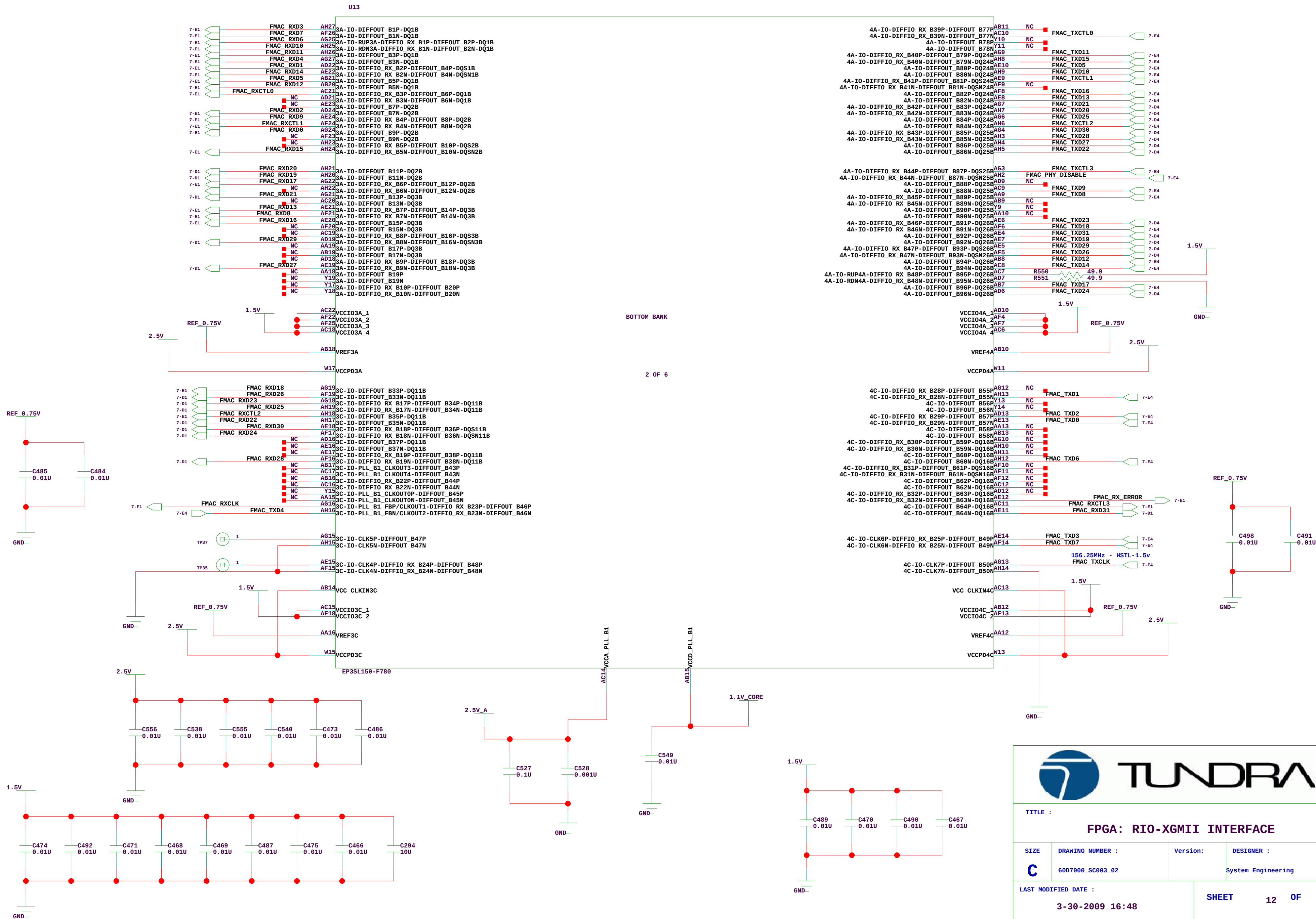
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	6007000_SC003_02	Rev 0	System Engineering

LAST MODIFIED DATE : **3-30-2009_16:48**

SHEET 11 OF 30

FPGA: RIO-XGMII Interface - Bottom Bank (1.5V HSTL)

FPGA driving RX as HSTL-15 Class-II with 25ohm source serial termination





TITLE :

FPGA: RIO-XGMII INTERFACE

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C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE :

3-30-2009_16:48

SHEET

12

OF

30

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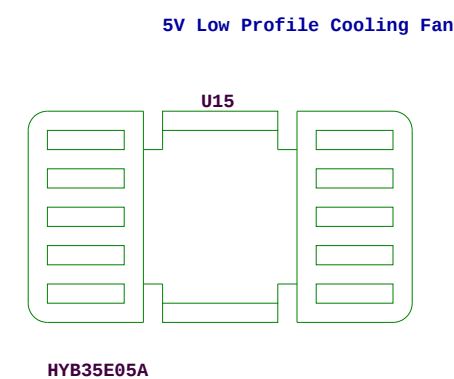


FPGA: CONFIG & RJ45

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LAST MODIFIED DATE : 3-30-2009_16:47 SHEET 14 OF 30

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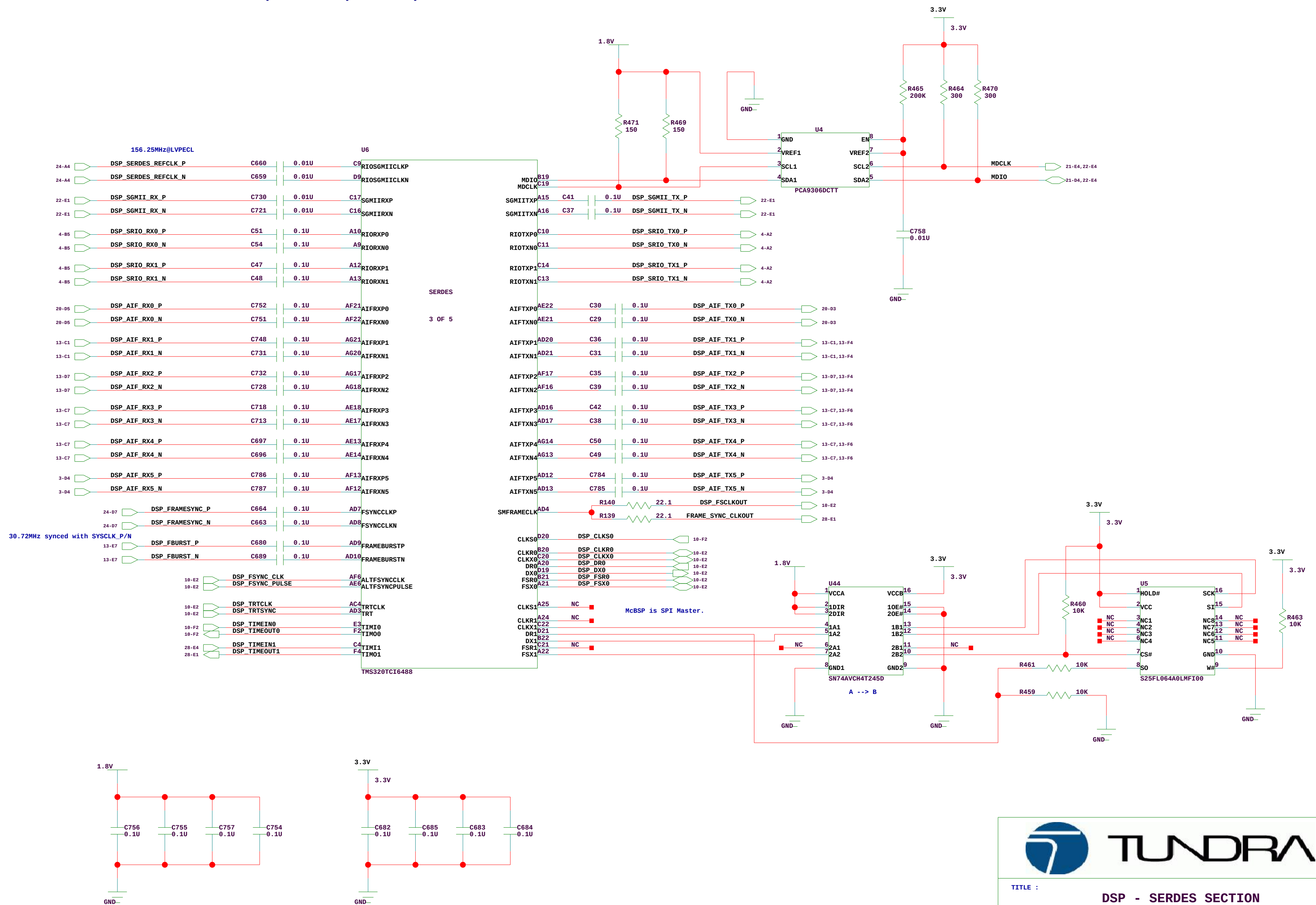
FPGA: POWER & GROUND

System Engineering

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SHEET 15 OF 30

DSP - SERDES Section: AIF, SGMII, sRIO, and S-Flash

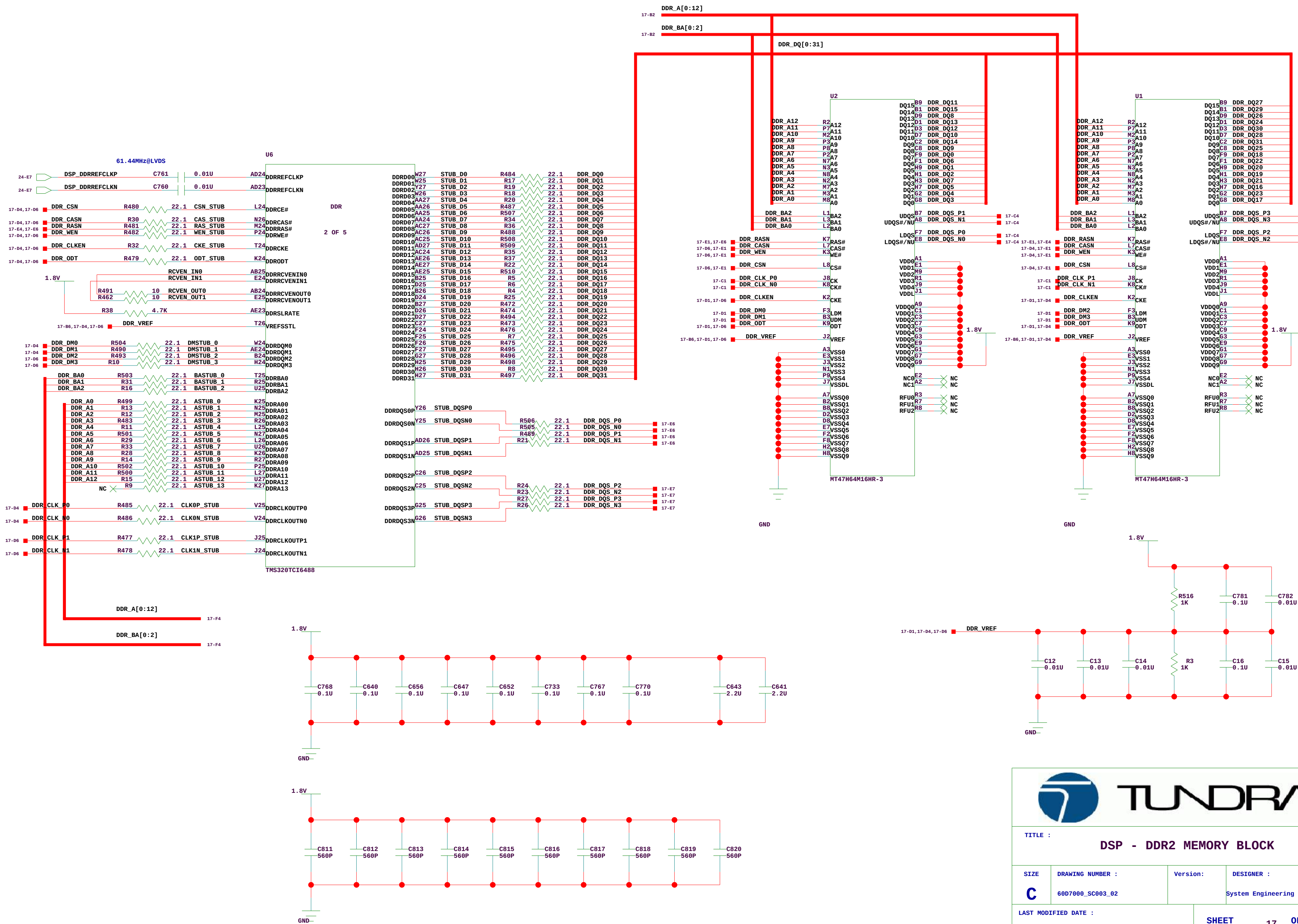


TITLE : **DSP - SERDES SECTION**

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE :	SHEET	16	OF	30
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DSP - DDR2 Memory Block



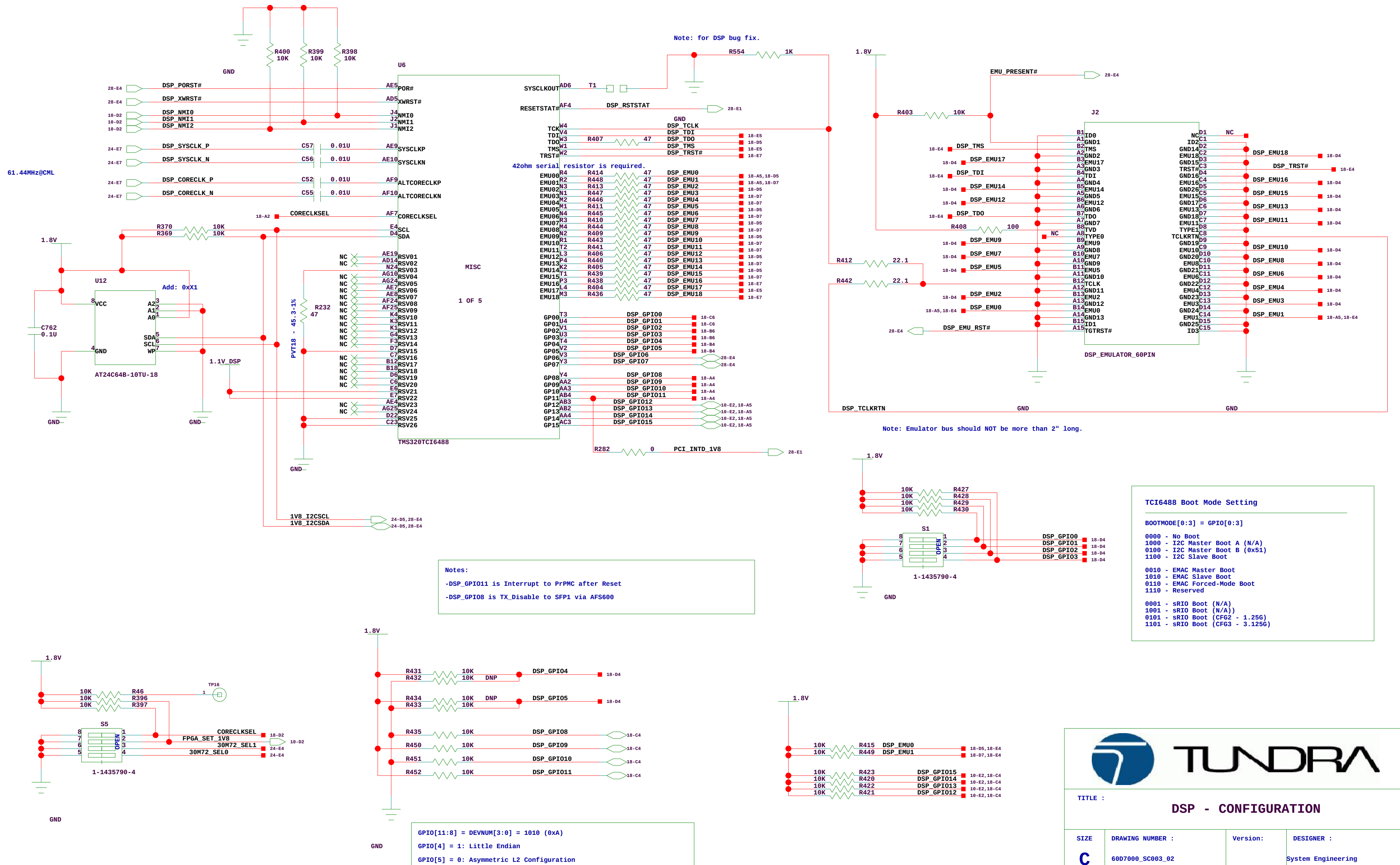


TITLE : **DSP - DDR2 MEMORY BLOCK**

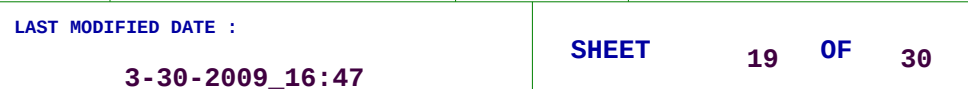
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C	60D7000_SC003_02		System Engineering

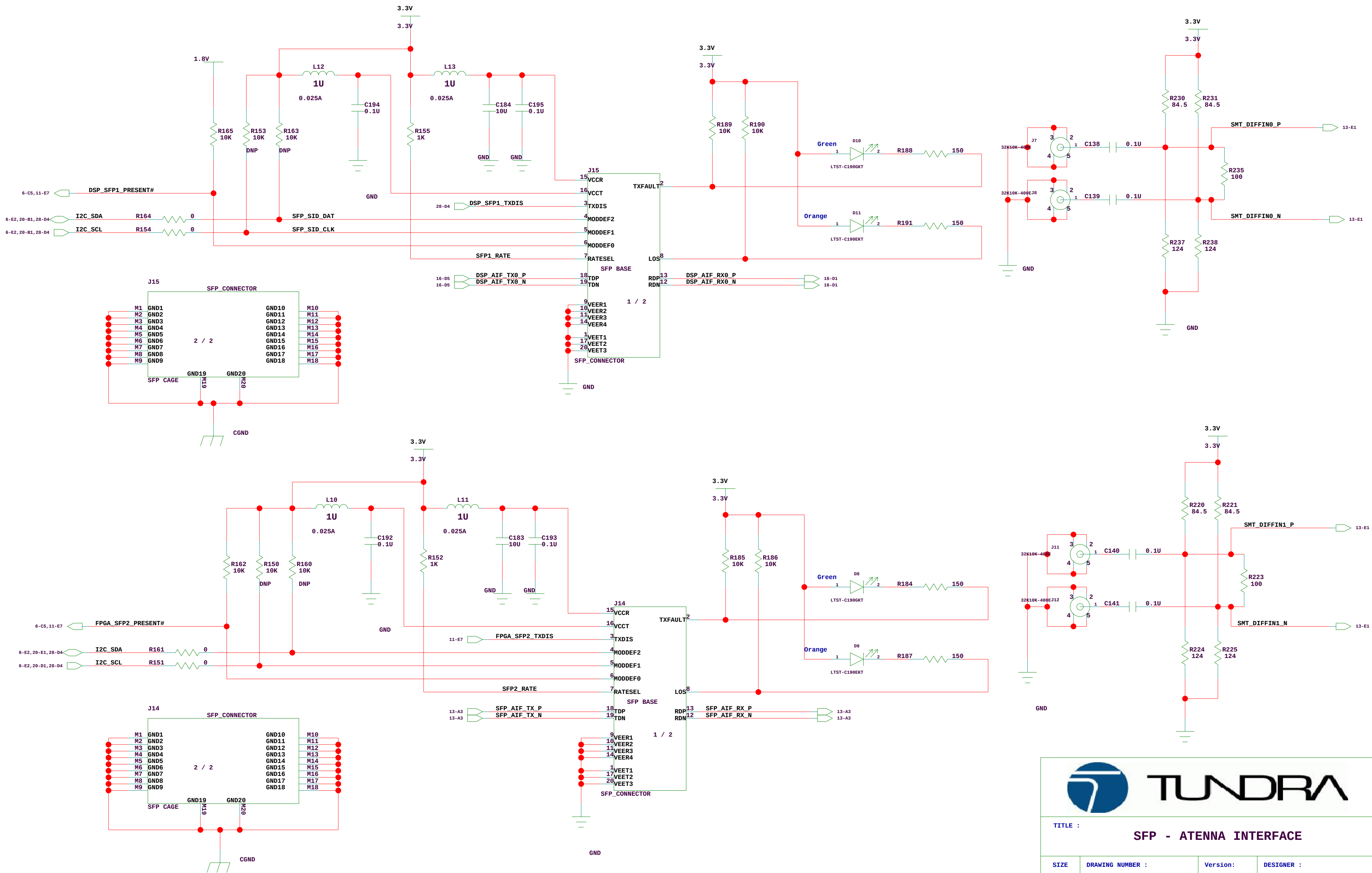
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F



SFP Antenna Interface Connectors





TITLE :

SFP - ATENNA INTERFACE

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE :

3-30-2009_16:47

SHEET

20

OF

30

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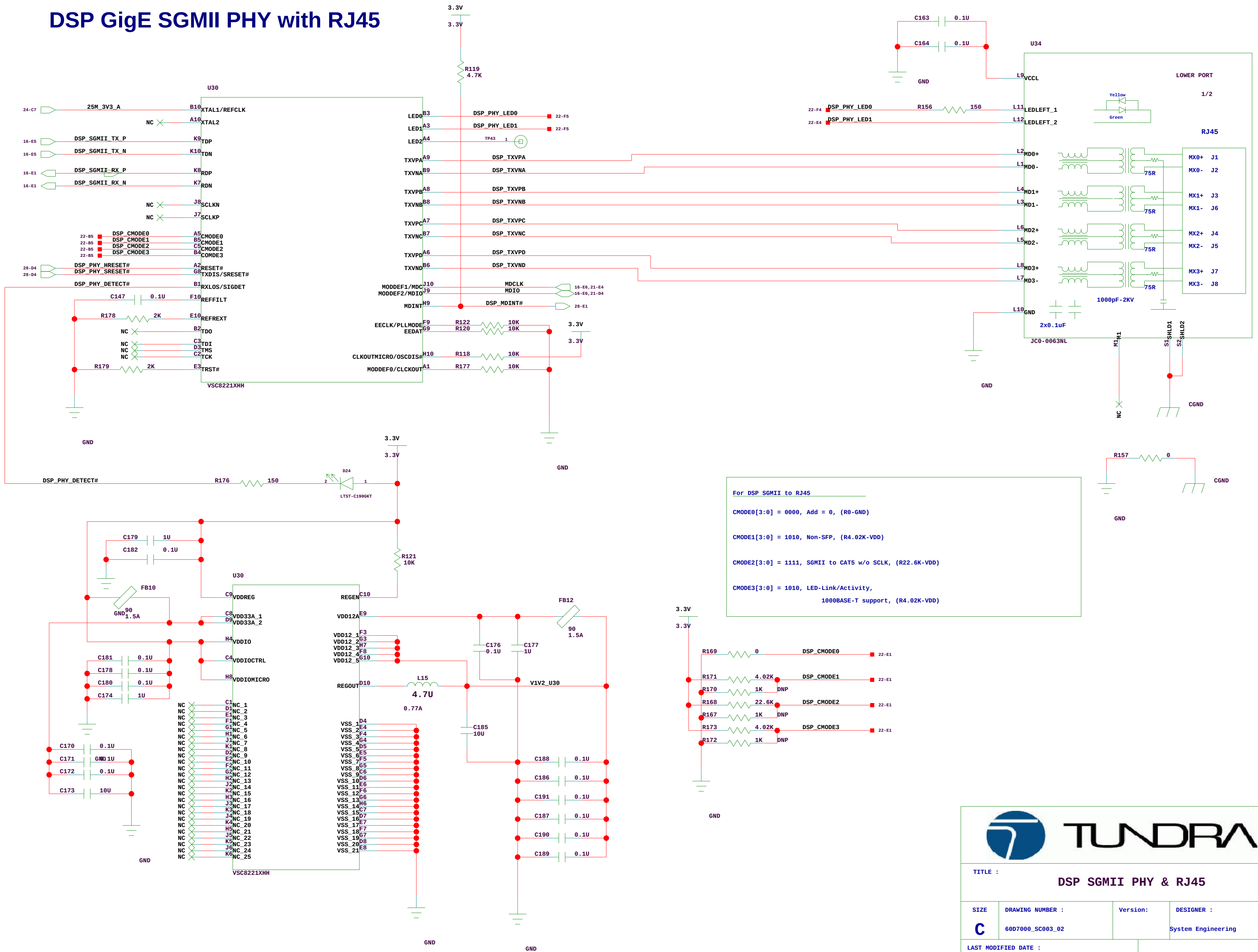
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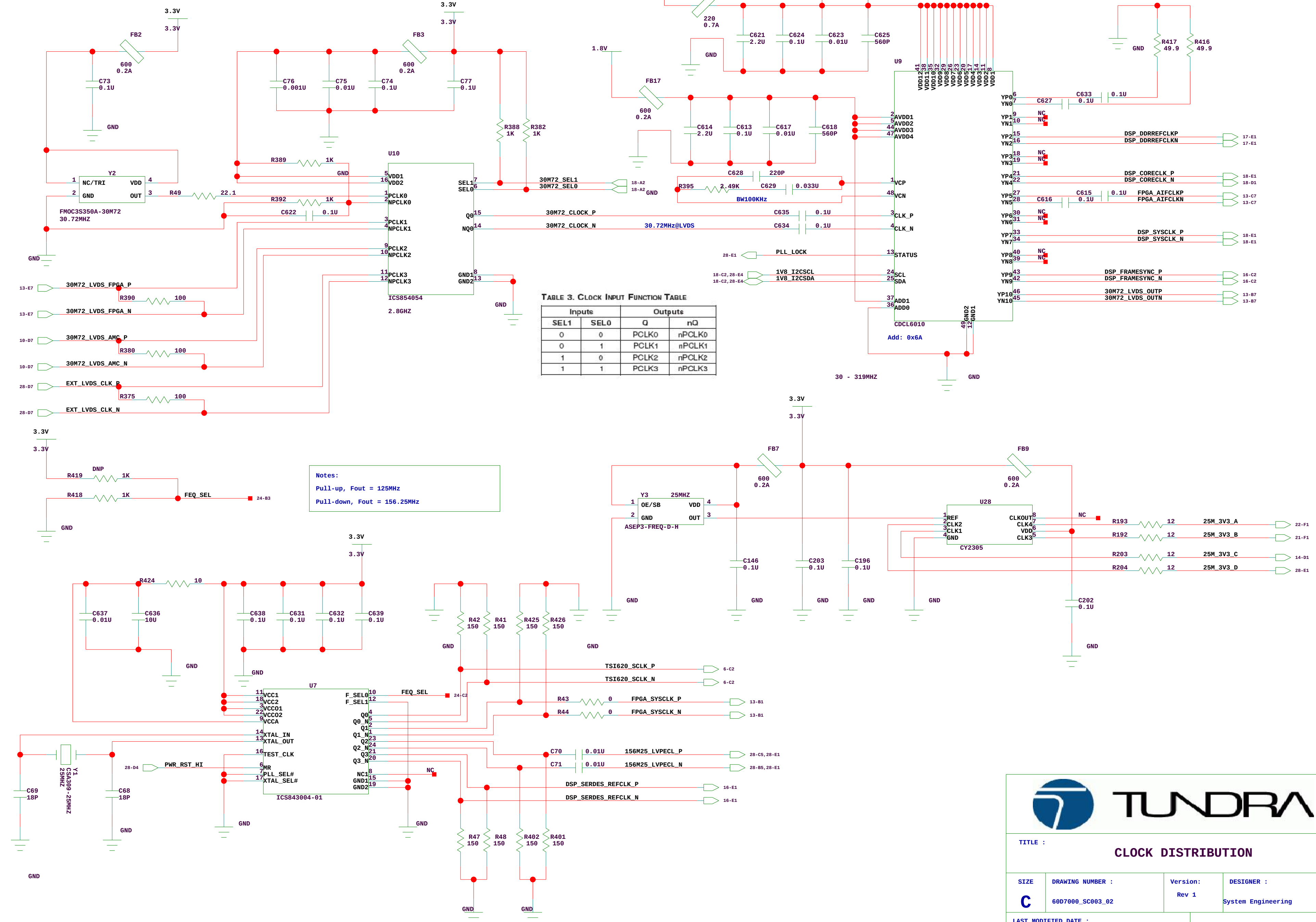
DSP GigE SGMII PHY with RJ45



USB TO TSI620 JTAG

SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
	60D7000_SC003_02	Rev 0	System Engineering
LAST MODIFIED DATE : 3-30-2009_16:47		SHEET 23 OF 30	

Clocking Distribution Block

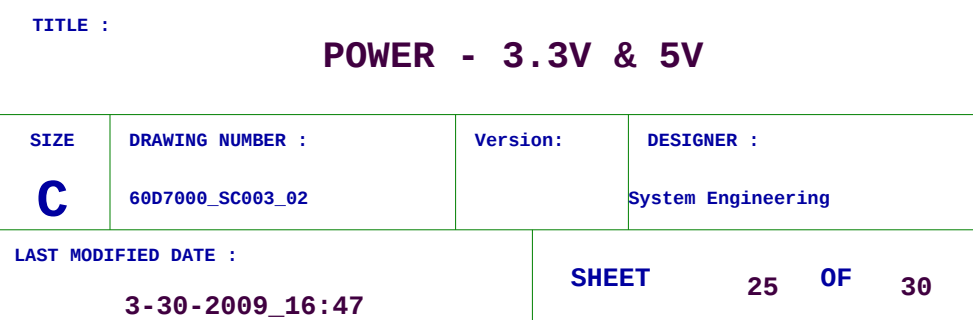


Inputs		Outputs	
SEL1	SEL0	Q	nQ
0	0	PCLK0	nPCLK0
0	1	PCLK1	nPCLK1
1	0	PCLK2	nPCLK2
1	1	PCLK3	nPCLK3



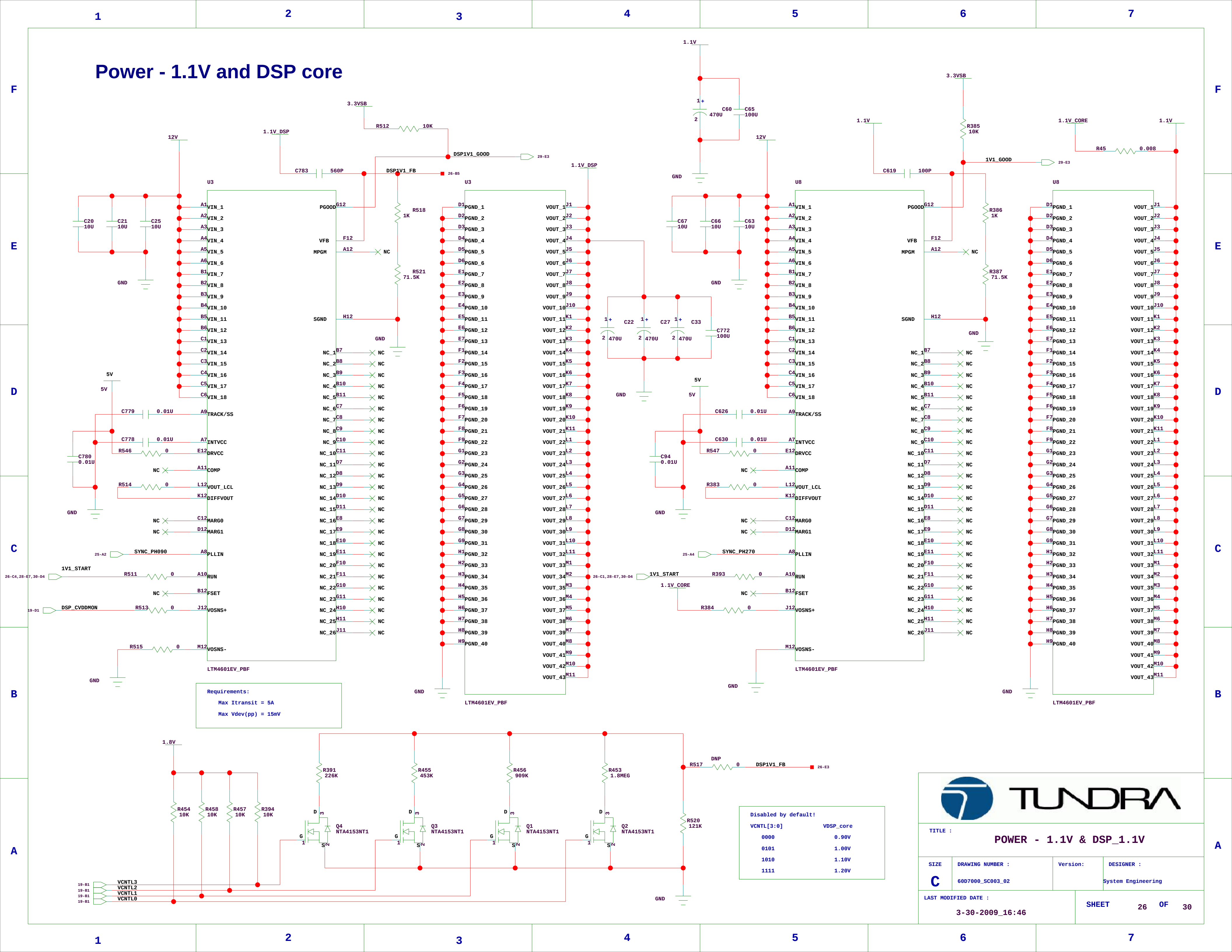
CLOCK DISTRIBUTION			
SIZE C	DRAWING NUMBER : 60D7000_SC003_02	Version: Rev 1	DESIGNER : System Engineering
LAST MODIFIED DATE : 3-30-2009_16:47			SHEET 24 OF

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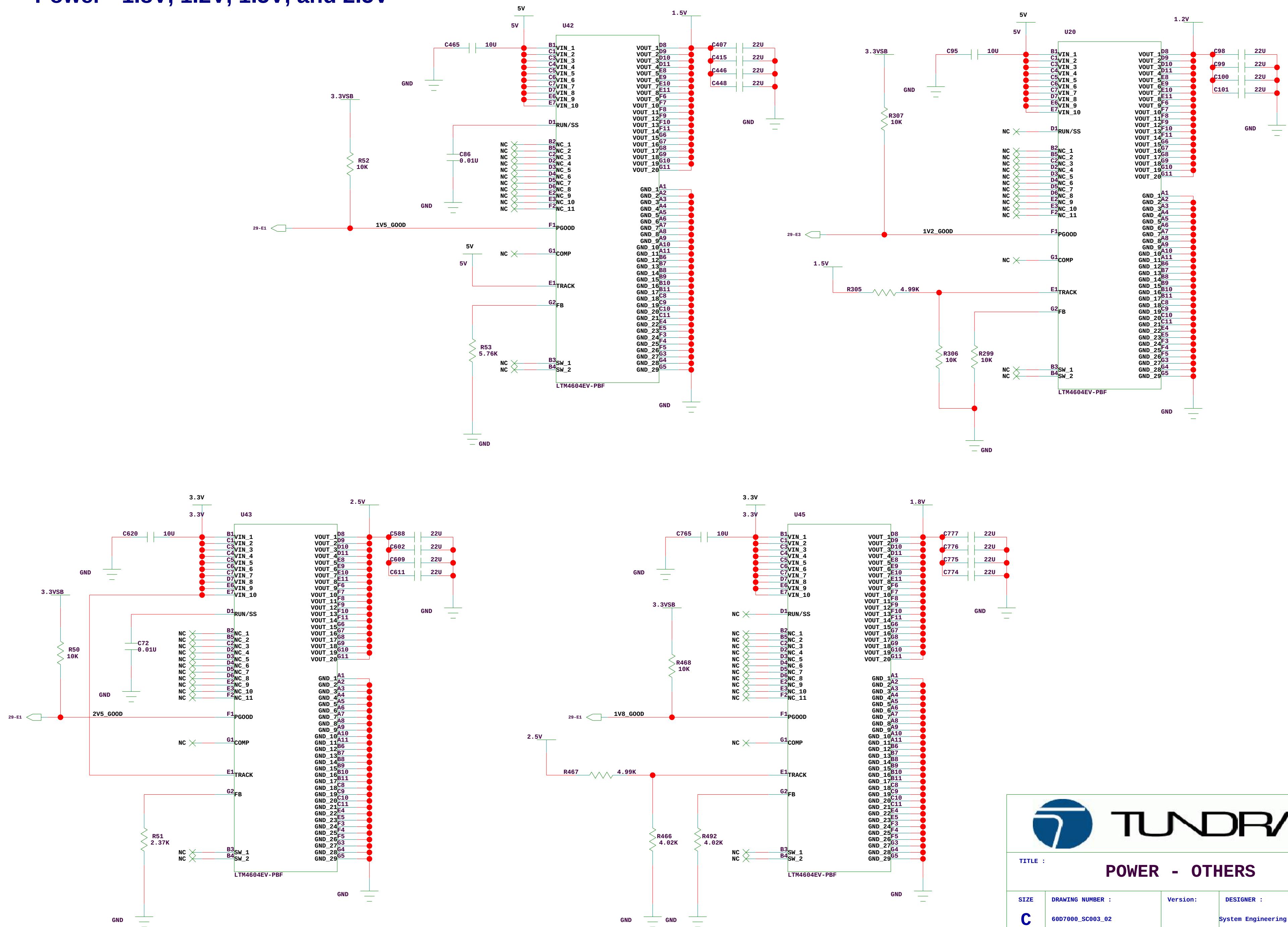


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C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE : 3-30-2009 16:46	SHEET 26 OF 30
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Power - 1.8V, 1.2V, 1.5V, and 2.5V



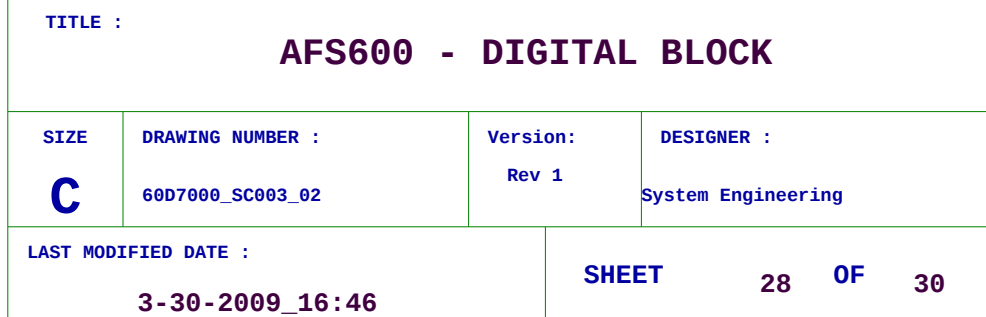
**TUNDRA**

TITLE :
POWER - OTHERS

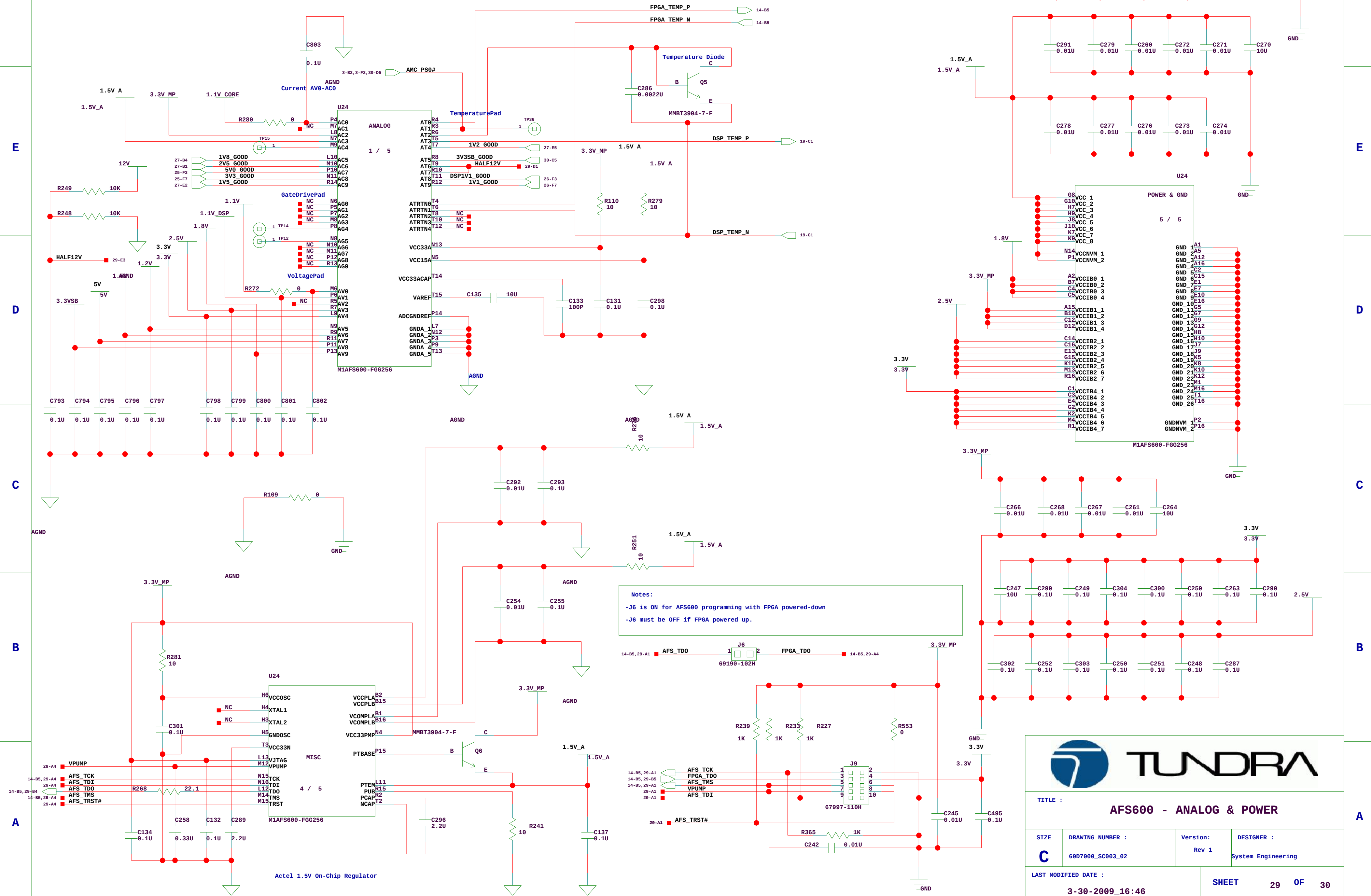
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System Controller: Analog, MISC, and Power





TITLE : AFS600 - ANALOG & POWER			
SIZE C	DRAWING NUMBER : 60D7000_SC003_02	Version: Rev 1	DESIGNER : System Engineering
LAST MODIFIED DATE : 3-30-2009_16:46		SHEET 29 OF 30	

F

