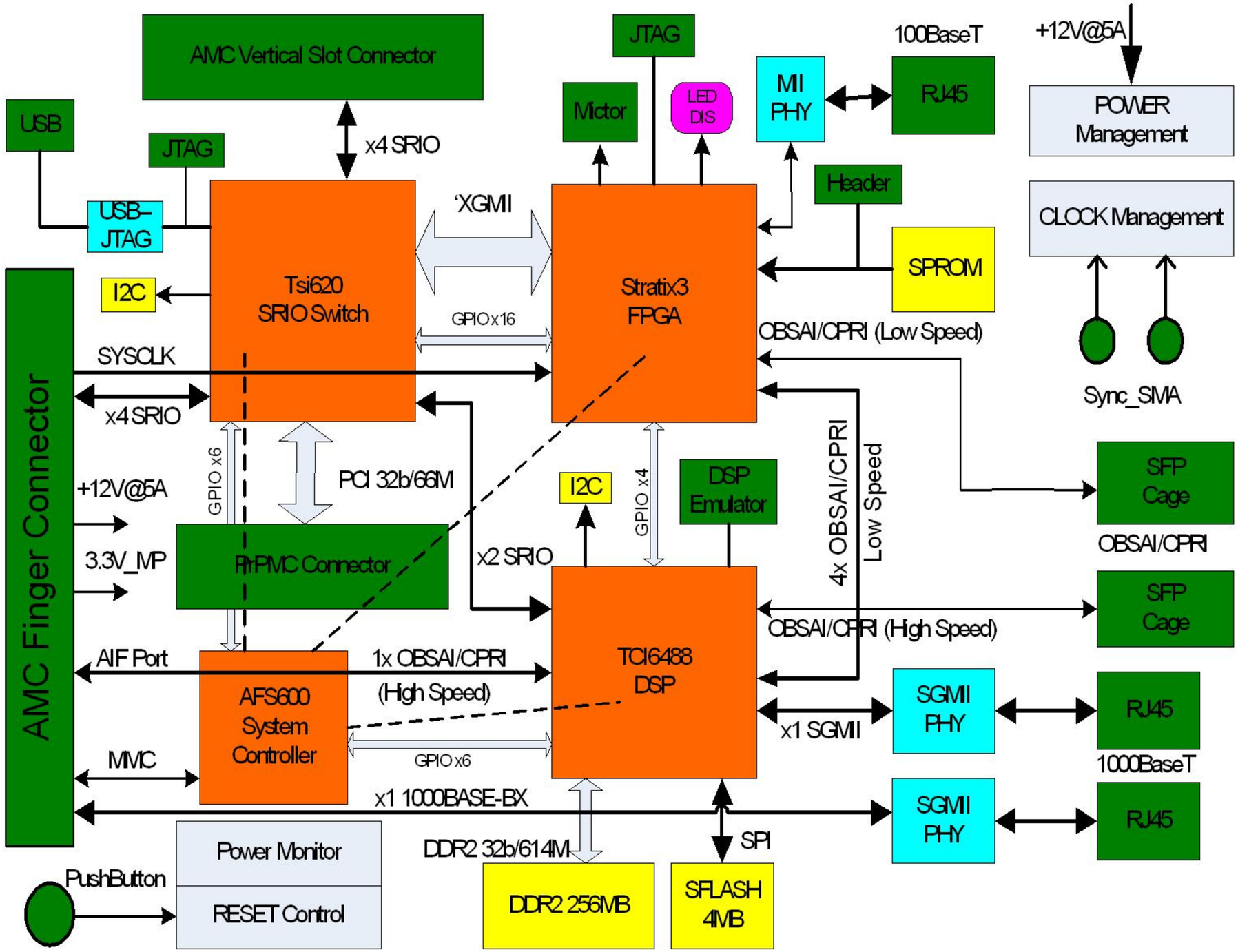
Tsi620 Evaluation Board Schematic

-Rev.1

Function Block Digram



Index

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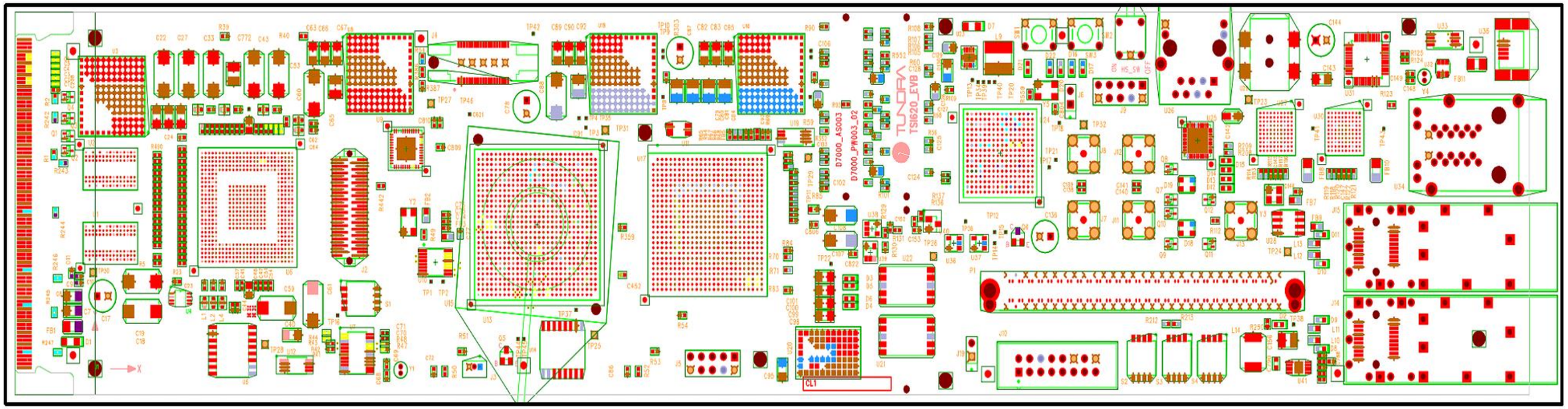
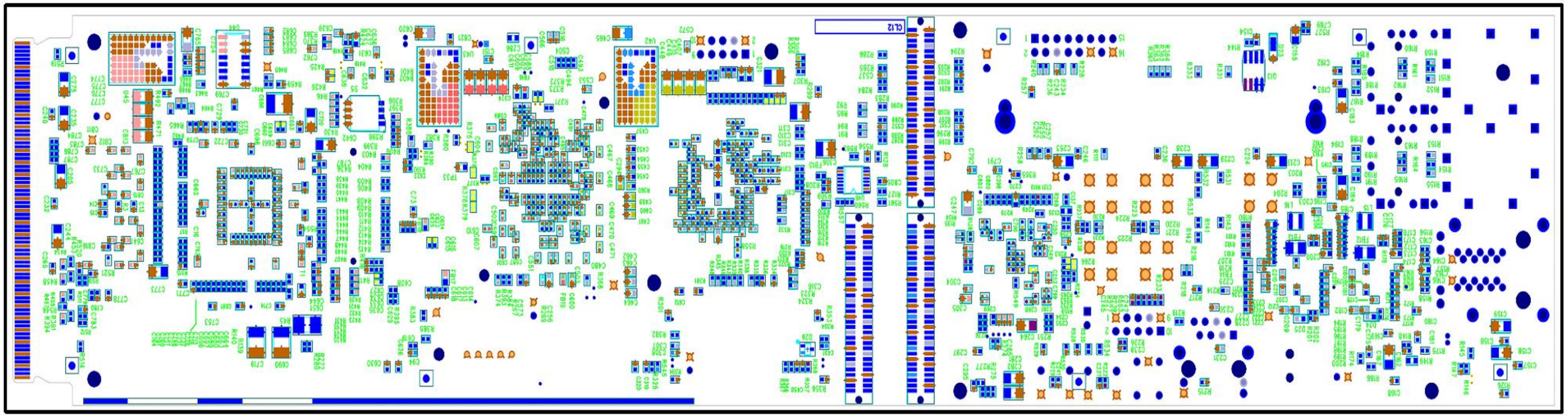
3. AMC Connectors
4. Tsi620 - PCI I/F and sRIO Ports
5. PrPMC Module
6. Tsi620 - GPIO & MISC
7. Tsi620 - FPGA XGMII I/F
8. Tsi620 - Power & GND
9. Tsi620 - Decoupling
10.FPGA - AMC Clock, DSP GPIO, Frame Sync
11.FPGA - Tsi620 GPIO and LED Display
12.FPGA - RIO XGMII Interface
13.FPGA - Antenna Interface
14.FPGA - 100BaseT RJ45 & Configuration
15.FPGA - Power, GND, & Decoupling
16.DSP - AIF, sRIO, & SGMII Ports
17.DSP - DDR2 Memory Block
18.DSP - Configuration & Emulator
19.DSP - Power Supply & Decoupling
20.Antenna I/F SFP Connectors
21.AMC GigE SMGII PHY & RJ45
22.DSP GigE SGMII PHY & RJ45
23.USB I/F to Tsi620 JTAG
24.Clocking Distribution
25.Power - 5V & 3.3V
26.Power - FPGA 1.1V & DSP Core 1.1V
27.Power - 1.2V, 1.5V, 1.8V, & 2.5V
28.AFS600 - Digital Block
29.AFS600 - Analog Block
30.Power - 12Vin, Sequencing, Mangement Power

TUNDRA

TITLE :			
FUNCTION BLOCK DIAGRAM			
SIZE C	DRAWING NUMBER : 60D7000_SC003_02	Version: Rev 1	DESIGNER : System Engineering
LAST MODIFIED DATE : 3-30-2009_16:48		SHEET 1 OF 30	

Components Placement Illustration





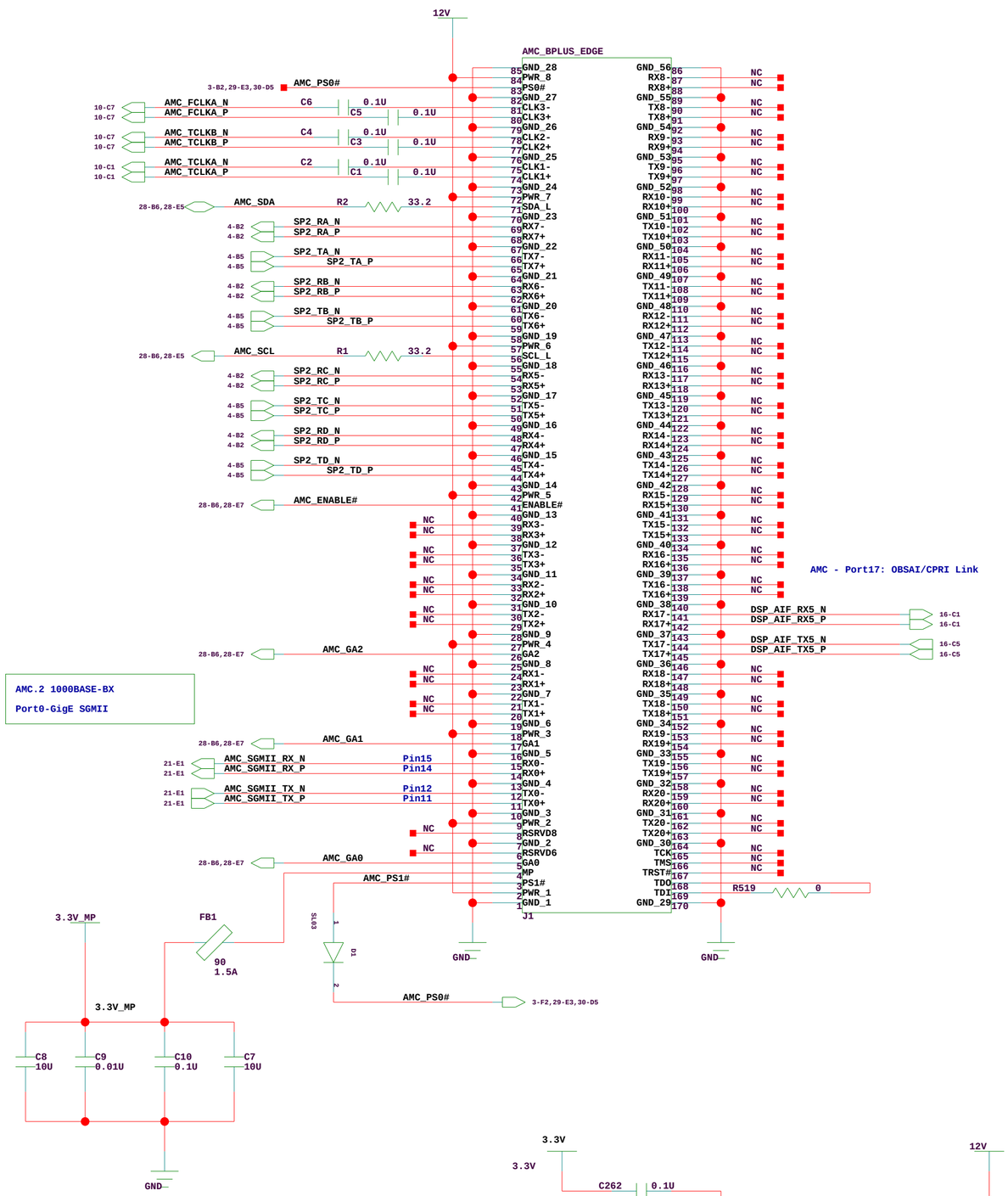
Revision Notes

-April 2nd, 2009: final editing for the customer release.

TUNDRA

TITLE : PLACEMENT ILLUSTRATION			
SIZE C	DRAWING NUMBER : 60D7000_SC003_02	Version: Rev 1	DESIGNER : System Engineering
LAST MODIFIED DATE : 4-2-2009_14:17		SHEET 2 OF 30	

AMC Finger Connector and AMC Slot Connector



AMC.2 1000BASE-BX

Port0-GigE SGMII

Tsi620 sRIO line reverse is required.

Note:

SAMC no JTAG I/F

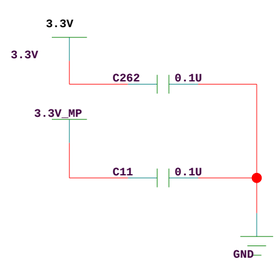
SAMC no System Management I/F (MMC, I2C)

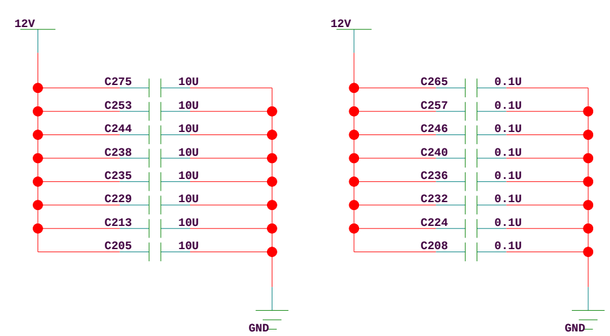
SAMC no Sync Clock I/F

SAMC site number: 8 (UPU)

IPMB address: 80h

SAMC no Port0-GigE

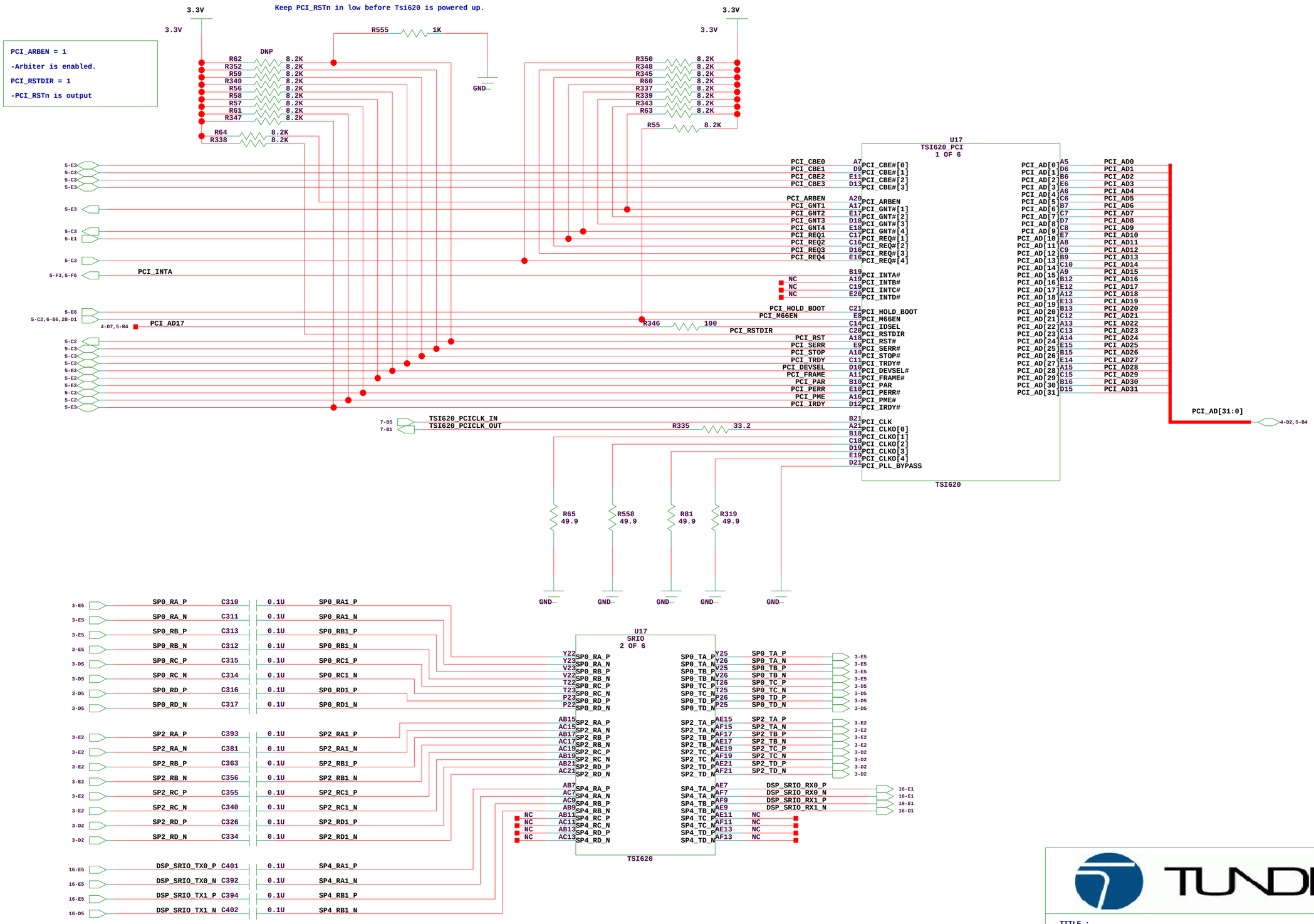




TUNDRA

TITLE : SRIO-AMC CONNECTIONS			
SIZE C	DRAWING NUMBER : 60D7000_SC003_02	Version: Rev 1	DESIGNER : System Engineering
LAST MODIFIED DATE : 3-30-2009_16:48	SHEET 3 OF 30		

Tsi620 - PCI Interface and sRIO Ports



TUNDRA

TITLE : TSI620 PCI I/F & SRIO PORTS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02	Rev 0	System Engineering

LAST MODIFIED DATE : 3-30-2009_16:48

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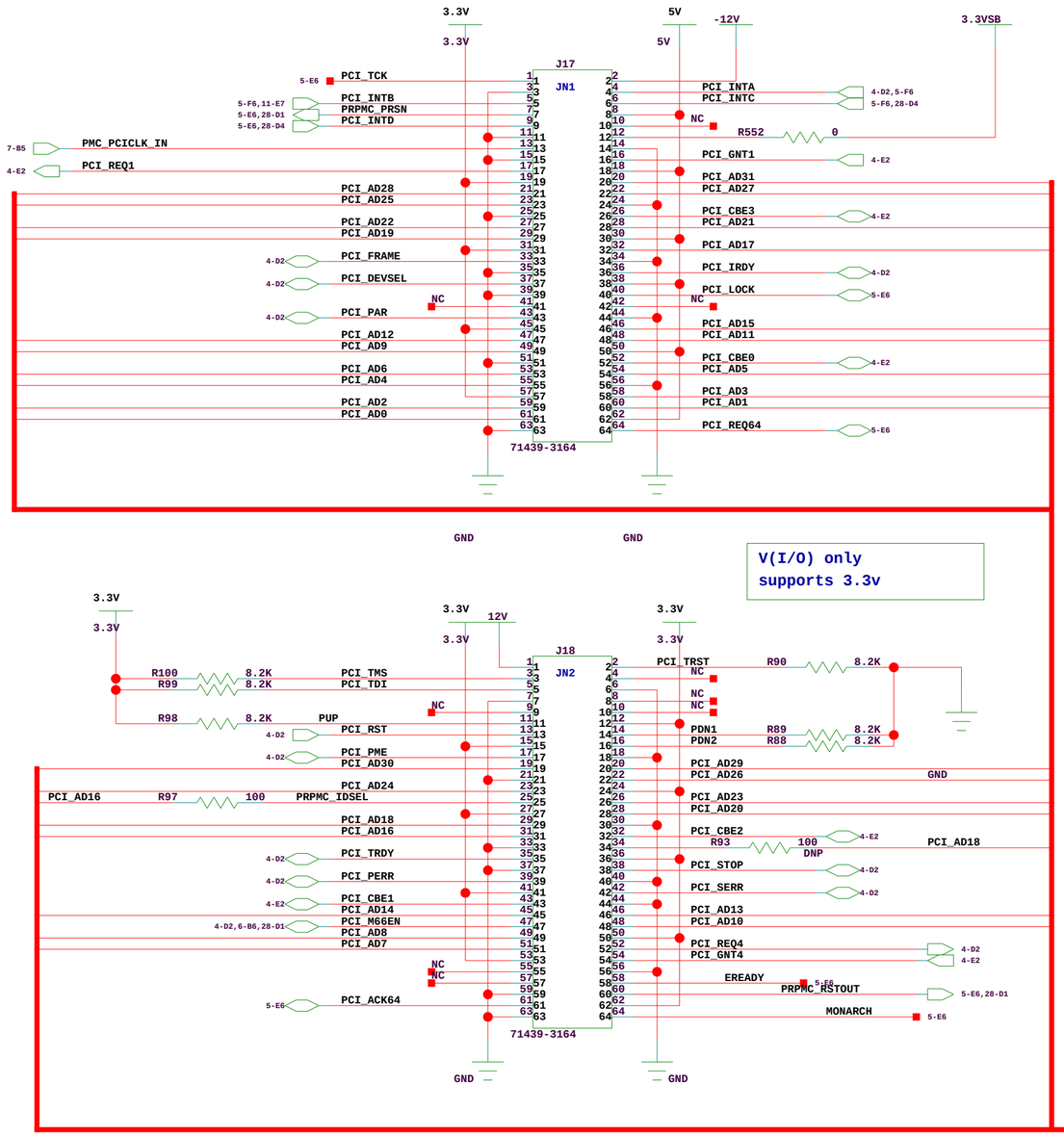
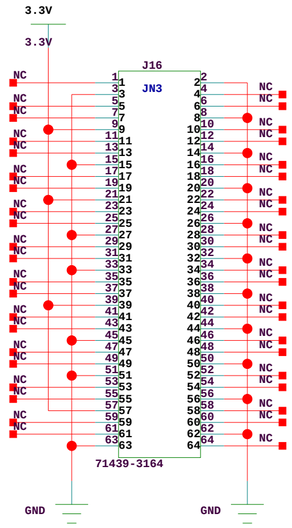
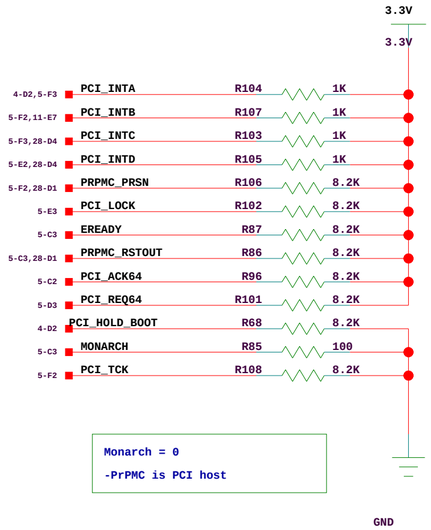
PrPMC Module







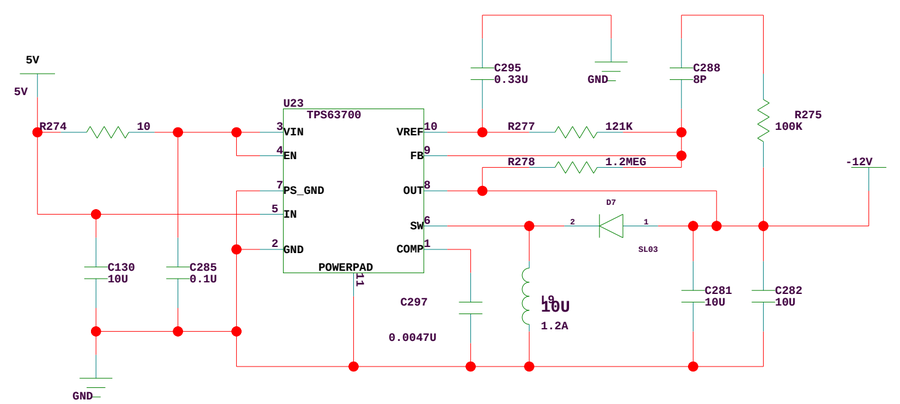
Monarch = 0

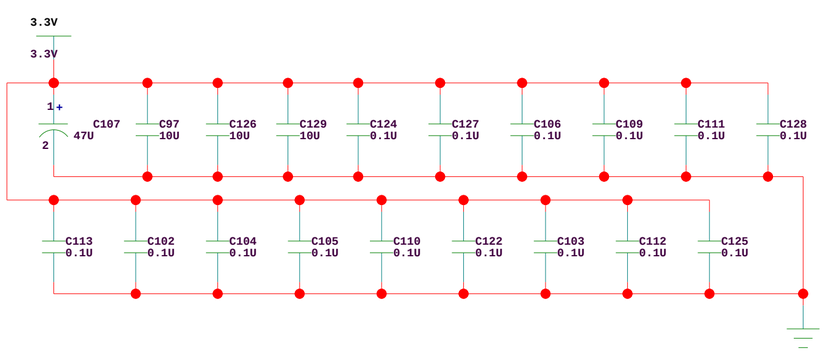
-PrPMC is PCI host

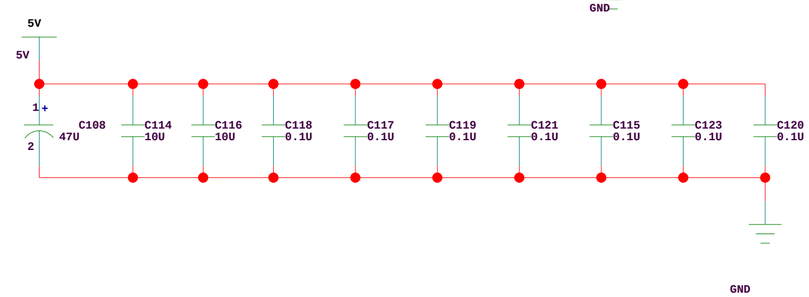
V(I/O) only supports 3.3v

PrPMC Interrupt Assignment:

- -INTA: Tsi620 PCI Interrupt
- -INTB: FPGA Interrupt
- -INTC: System Controller (AFS600) Interrupt
- -INTD: DSP GPIO11 Interrupt



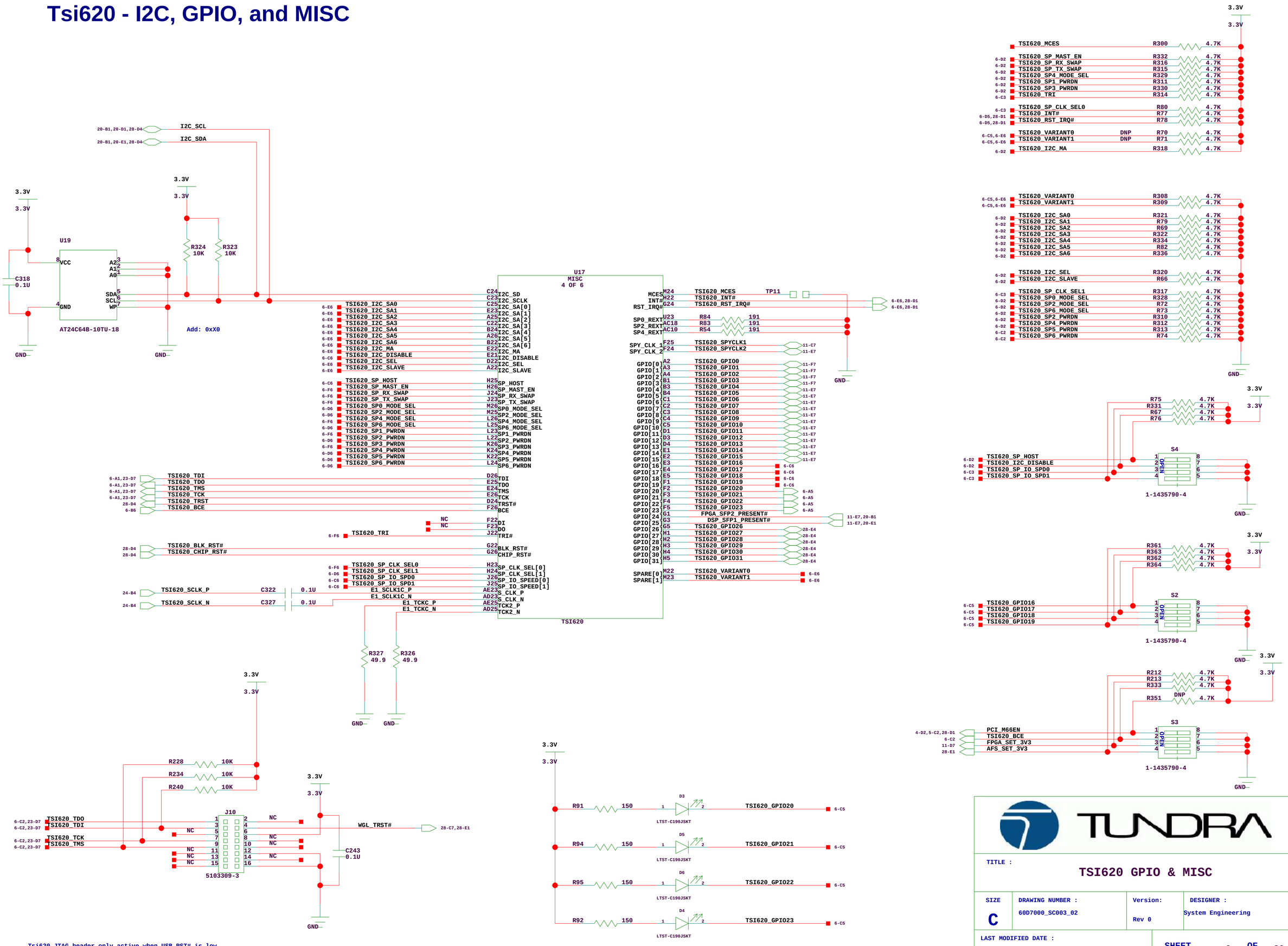




TUNDRA

TITLE :			
PRPMC MODULE			
SIZE: C	DRAWING NUMBER : 60D7000_SC003_02	Version:	DESIGNER : System Engineering
LAST MODIFIED DATE : 3-30-2009_16:48	SHEET 5 OF 30		

Tsi620 - I2C, GPIO, and MISC



Tsi620 JTAG header only active when USB_RST# is low.

TUNDRA

TITLE : TSI620 GPIO & MISC

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02	Rev 0	System Engineering

LAST MODIFIED DATE : 3-30-2009_16:48

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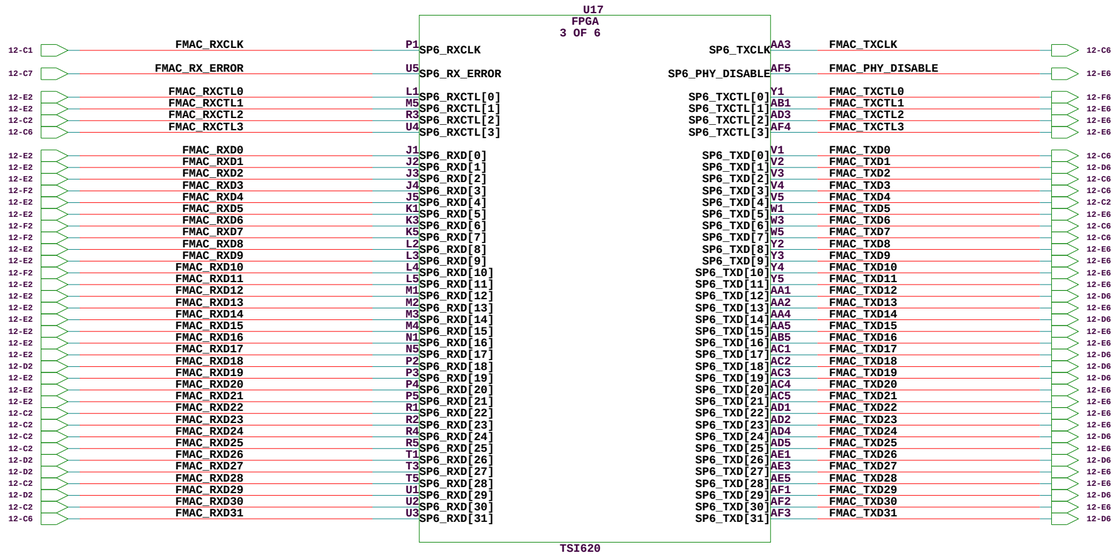
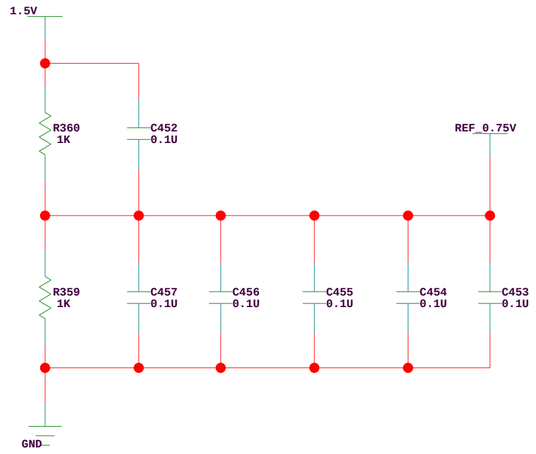
Tsi620 - FPGA XGMII Interface and PCI Clocking

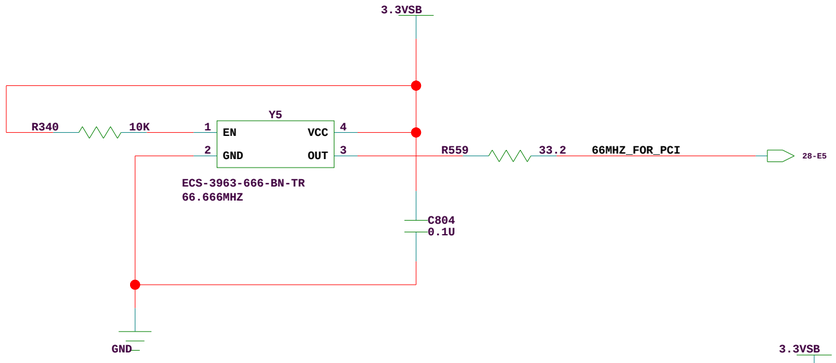
Notes:

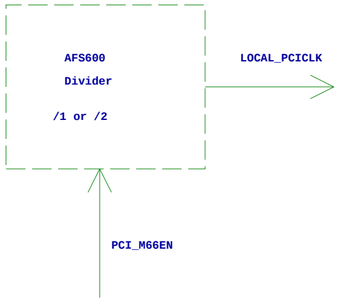
1) Tsi620 drives HSTL-15 Class-I output which is terminated on FPGA with parallel ODT.

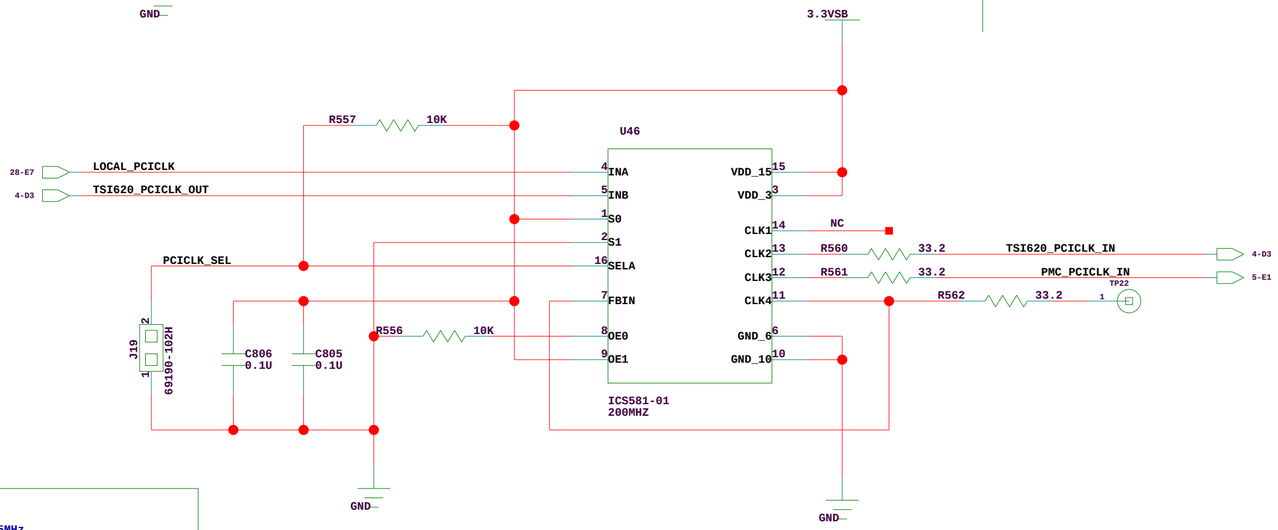
2) Tsi620 recieves HSTL-15 Class-II from FPGA with source series ODT.











Notes:

[1] S[1:0] = 01 : 19/75MHz

[2] Jumper J19 OFF: Select INA

TUNDRA

TITLE :

TSI620 FPGA I/F & PCI_CLK

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02	Rev 0	System Engineering

LAST MODIFIED DATE :

3-30-2009_16:48

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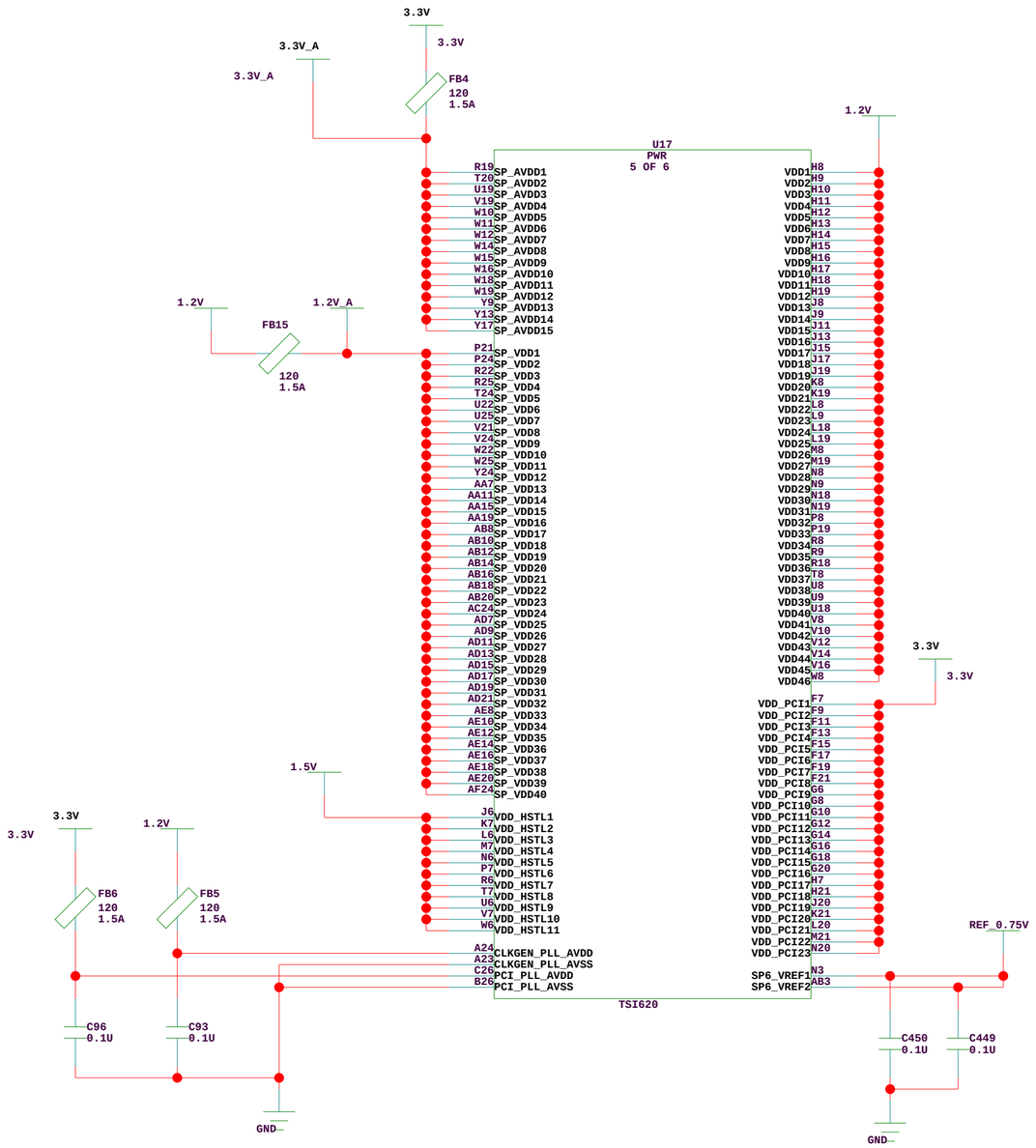
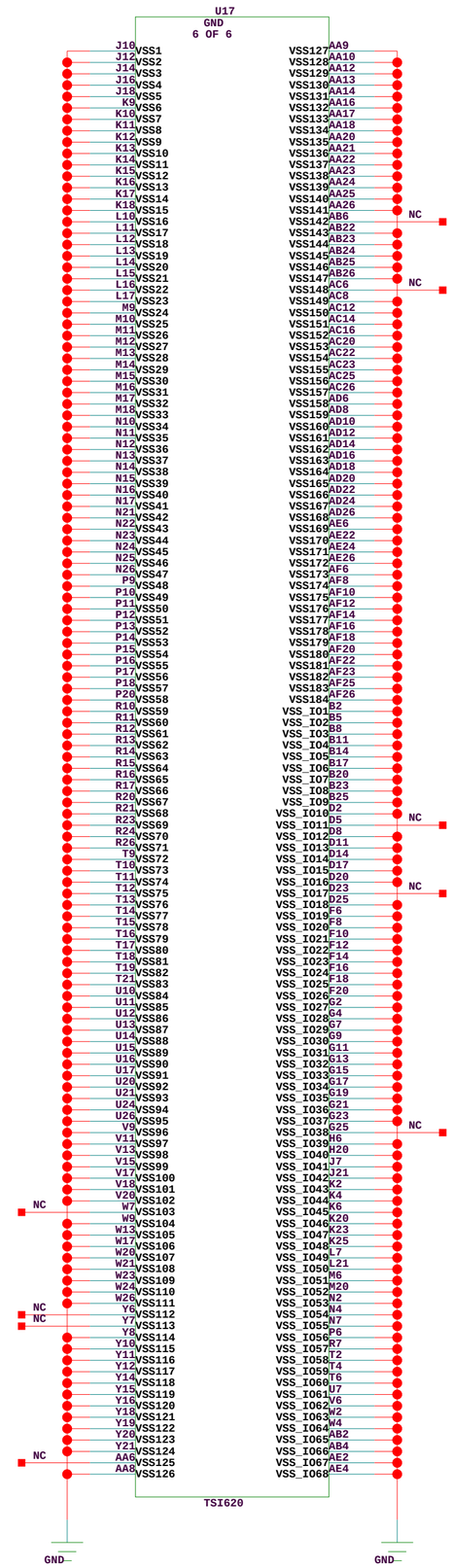
Tsi620 - Power and GND

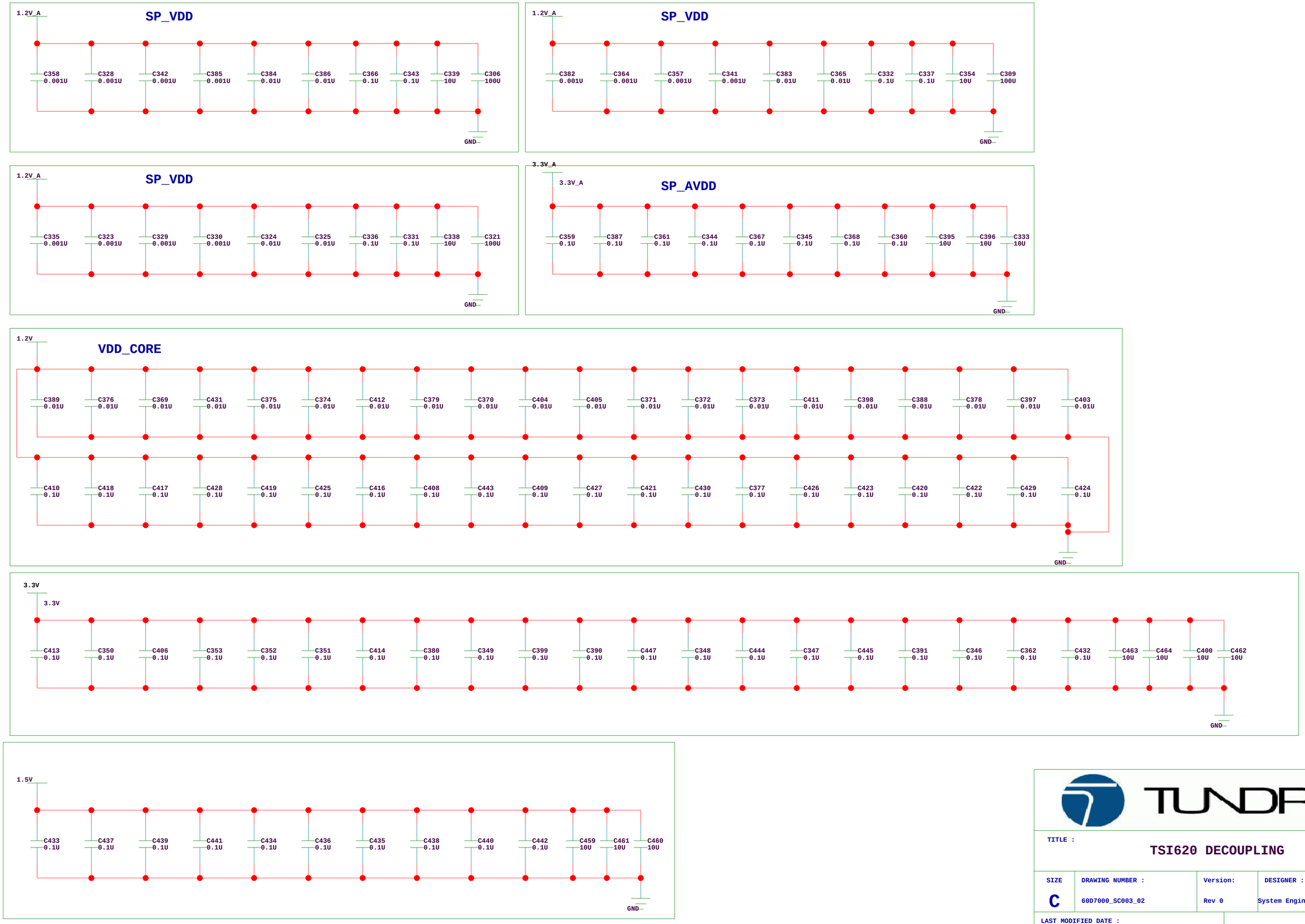




TUNDRA

TITLE : TSI620 - POWER & GND			
SIZE C	DRAWING NUMBER : 60D7000_SC003_02	Version: Rev 0	DESIGNER : System Engineering
LAST MODIFIED DATE : 3-30-2009_16:48		SHEET 8 OF 30	

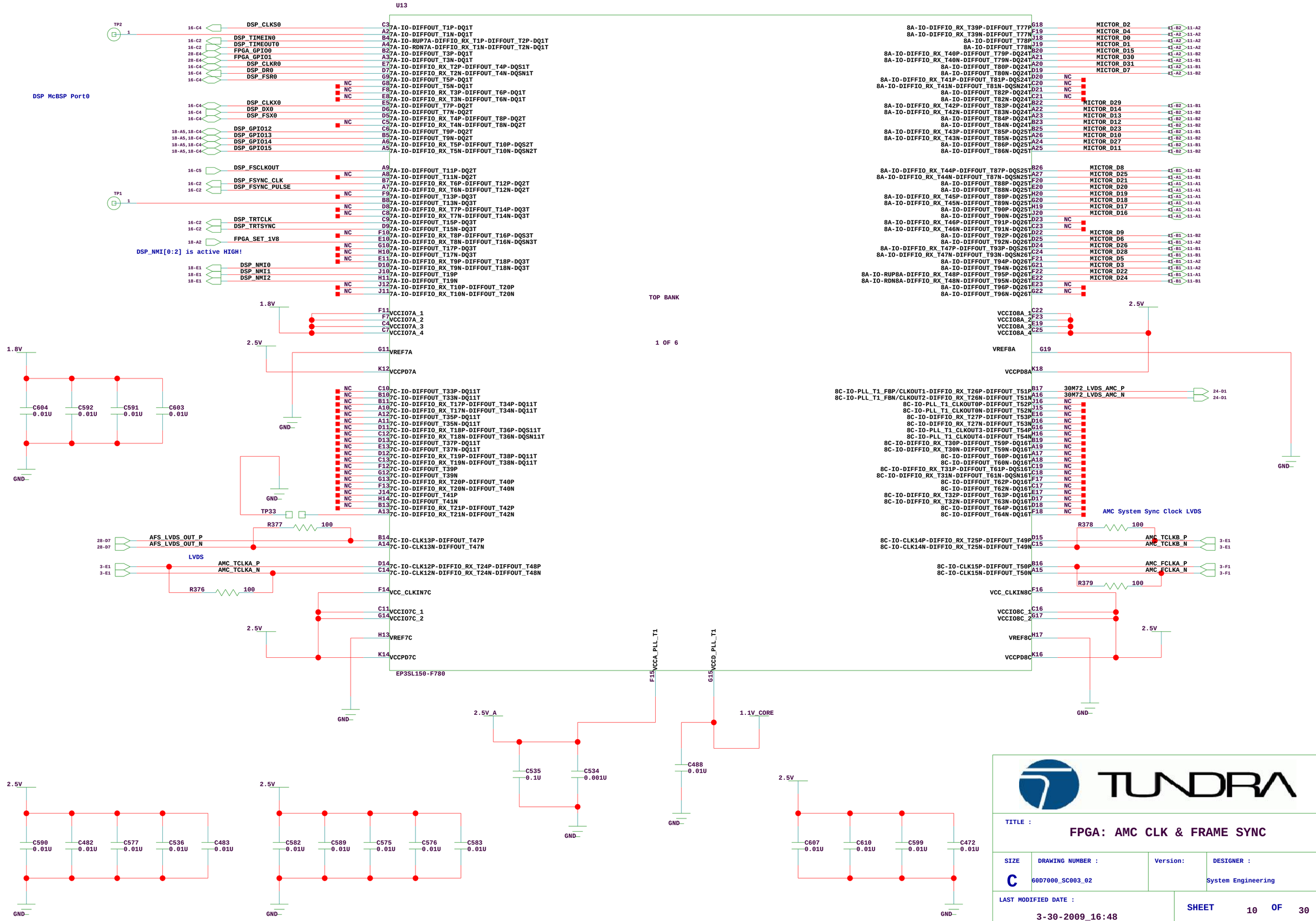
Tsi620 - Decoupling



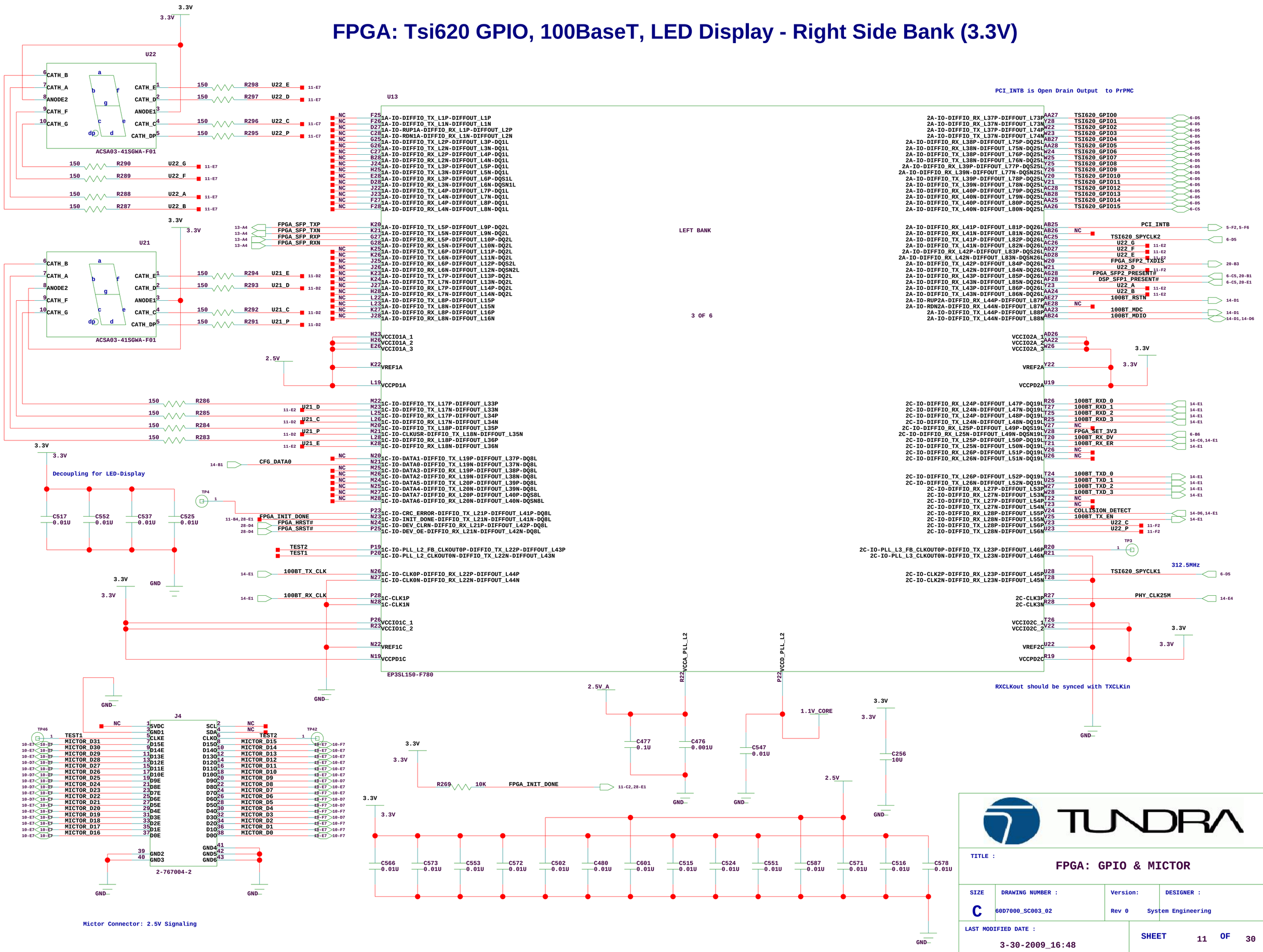
TUNDRA

TITLE :			
TSI620 DECOUPLING			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02	Rev 0	System Engineering
LAST MODIFIED DATE :		SHEET 9 OF 30	
3-30-2009_16:48			

FPGA: DSP GPIO, AMC Clock, DSP Frame Sync - Top Bank (1.8V, 2.5V, 3.3V)



FPGA: Tsi620 GPIO, 100BaseT, LED Display - Right Side Bank (3.3V)

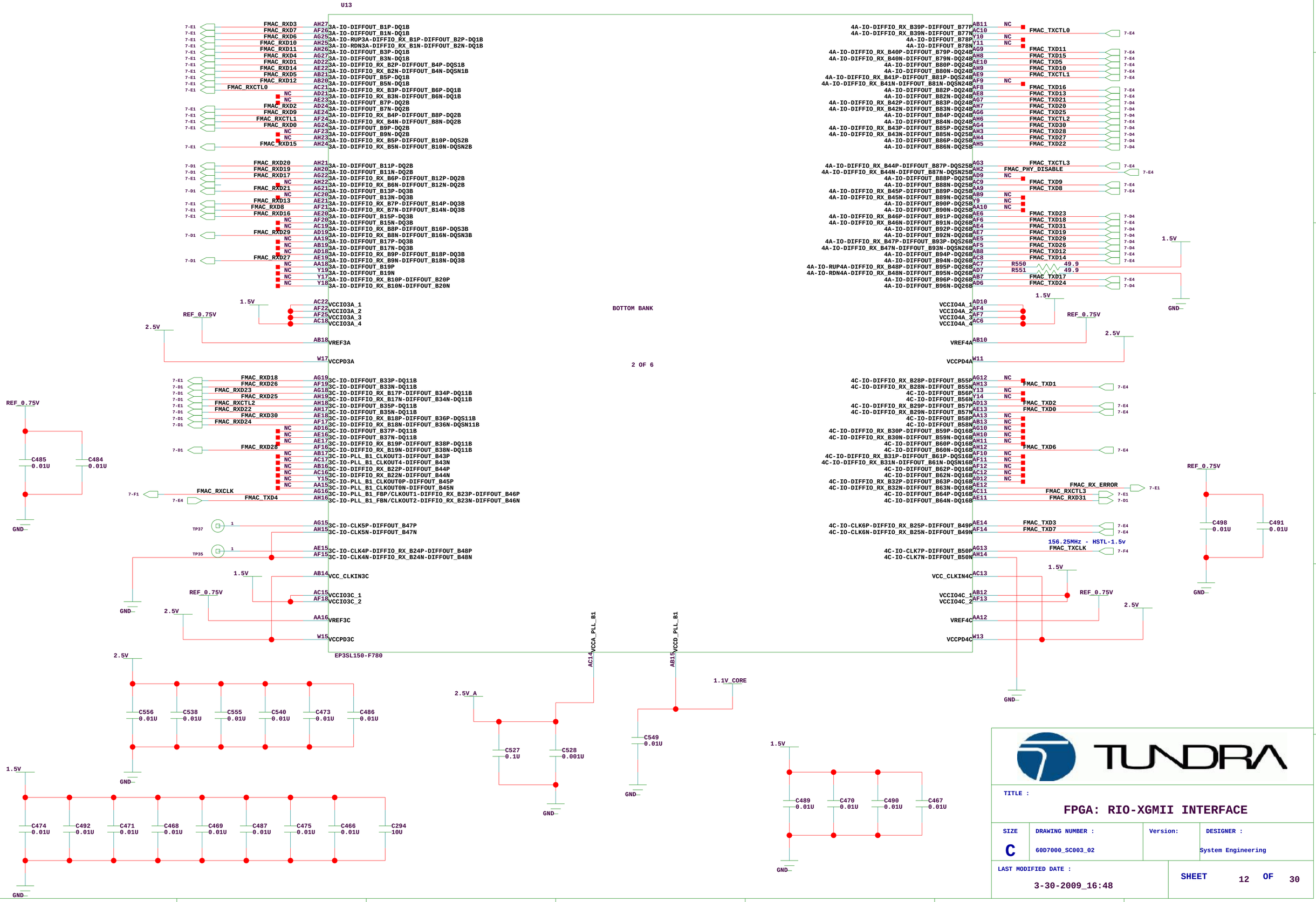


TUNDRA

TITLE :			
FPGA: GPIO & MICTOR			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02	Rev 0	System Engineering
LAST MODIFIED DATE :		SHEET 11 OF 30	
3-30-2009_16:48			

FPGA: RIO-XGMII Interface - Bottom Bank (1.5V HSTL)

FPGA driving RX as HSTL-15 Class-II with 25ohm source serial termination



TUNDRA

TITLE :

FPGA: RIO-XGMII INTERFACE

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE : 3-30-2009_16:48

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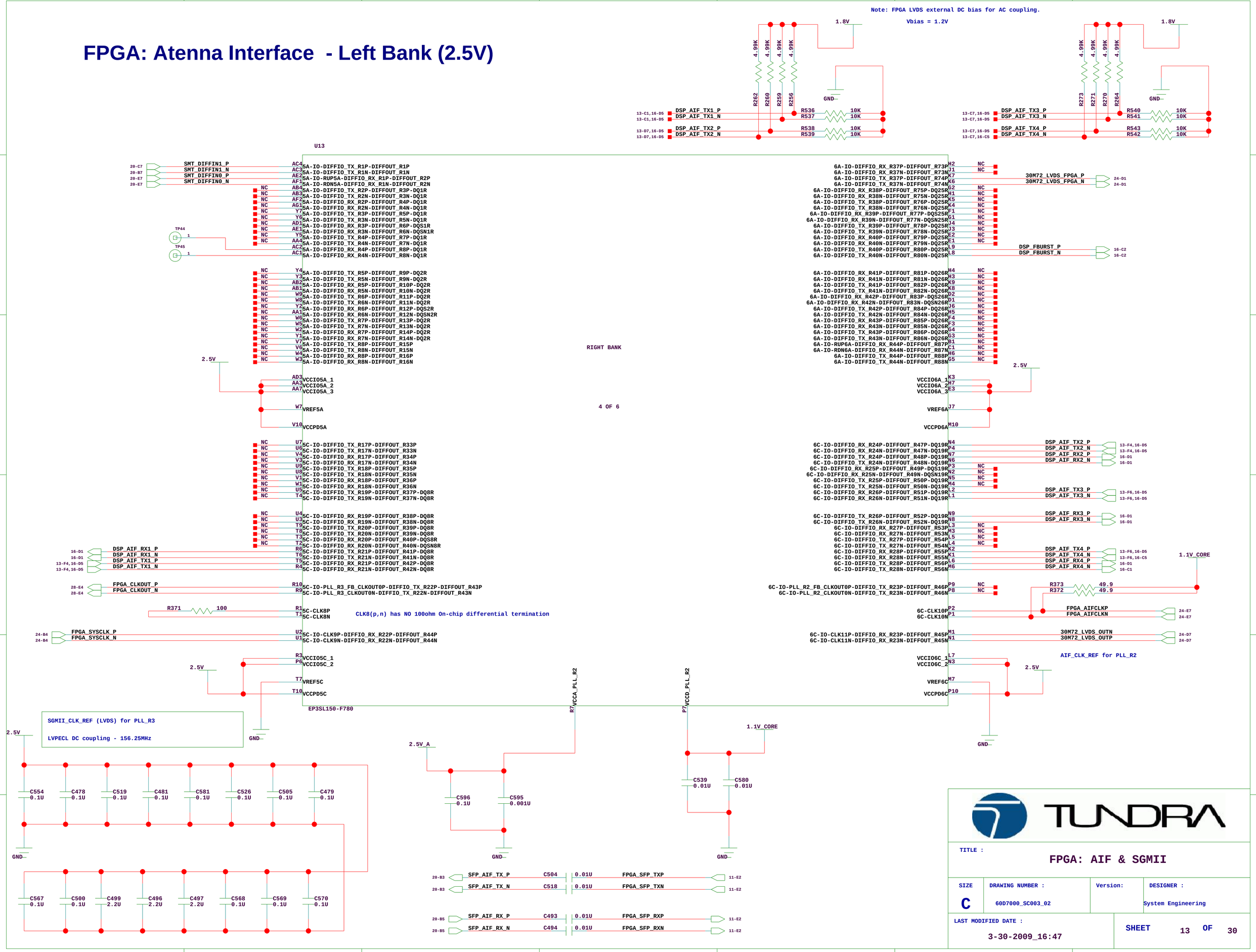
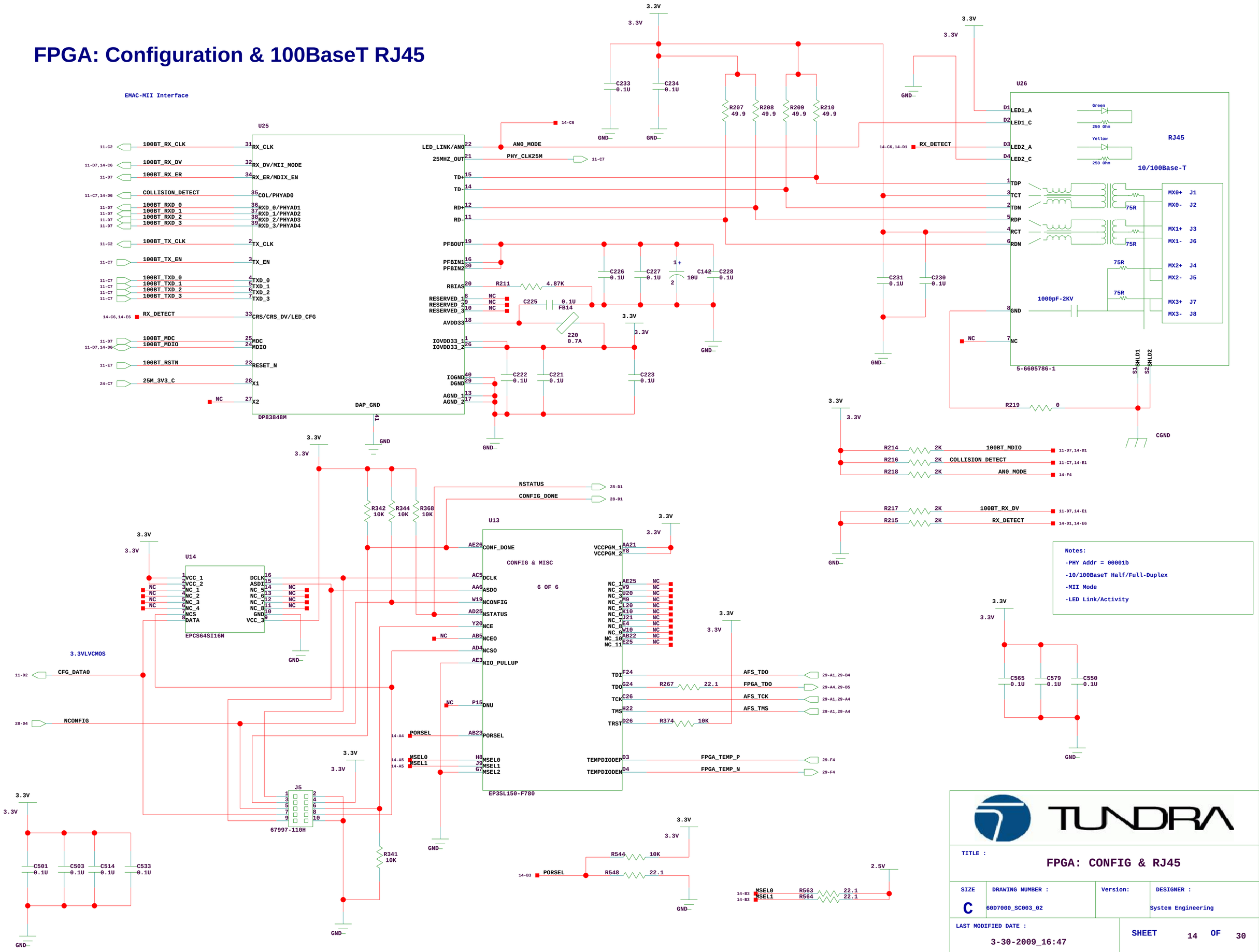
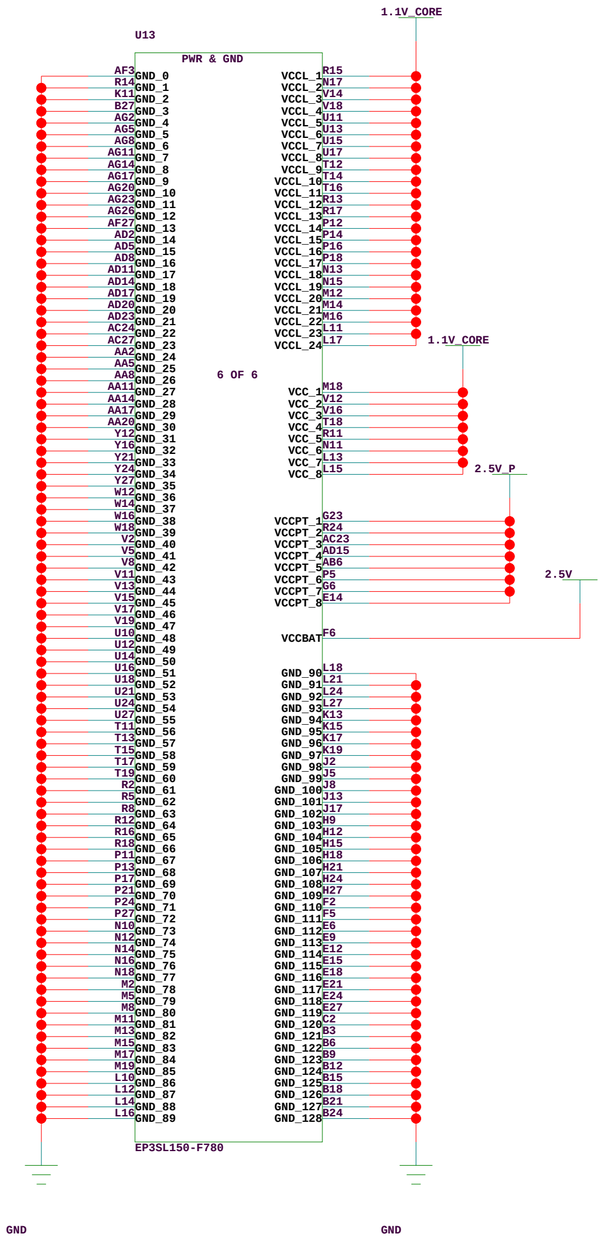
FPGA: Atenna Interface - Left Bank (2.5V)

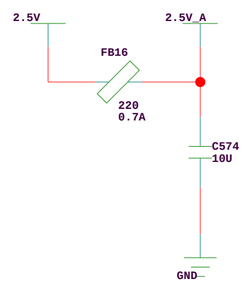


FPGA: Configuration & 100BaseT RJ45



FPGA: Power, Ground, and Decoupling

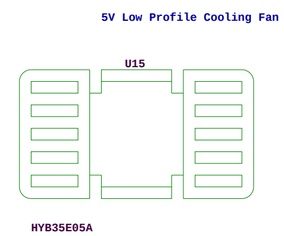


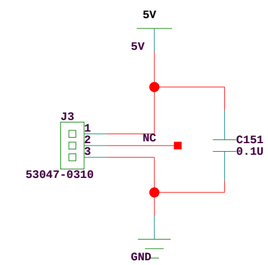


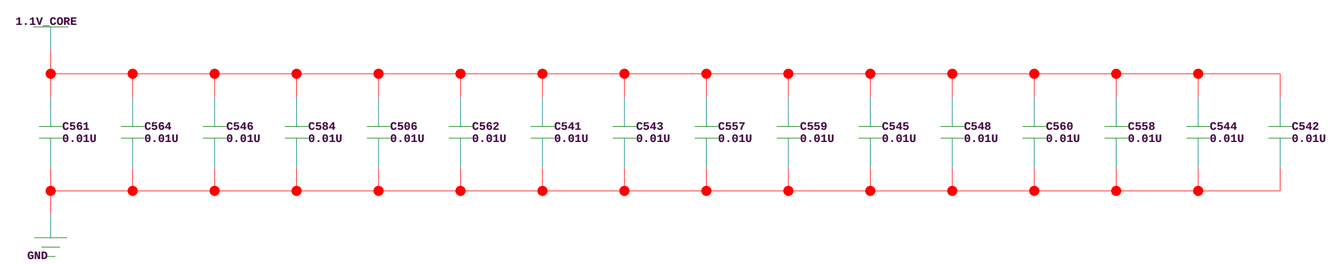
Notes:

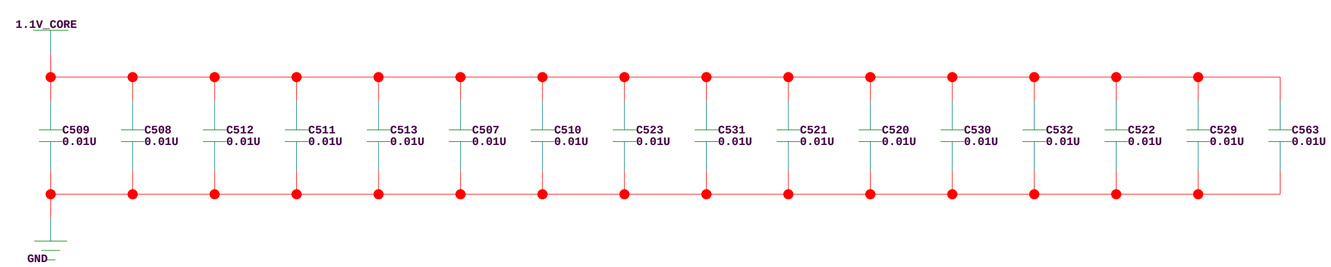
2.5V_A is the filtered 2.5V supply to VCCA_PLL of FPGA

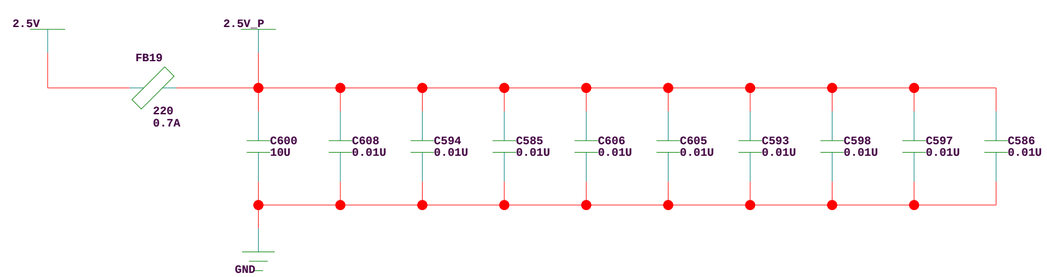
2.5V_P is the filtered 2.5V supply to VCCPT of FPGA











TUNDRA

TITLE : FPGA: POWER & GROUND

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE : 3-30-2009_16:47

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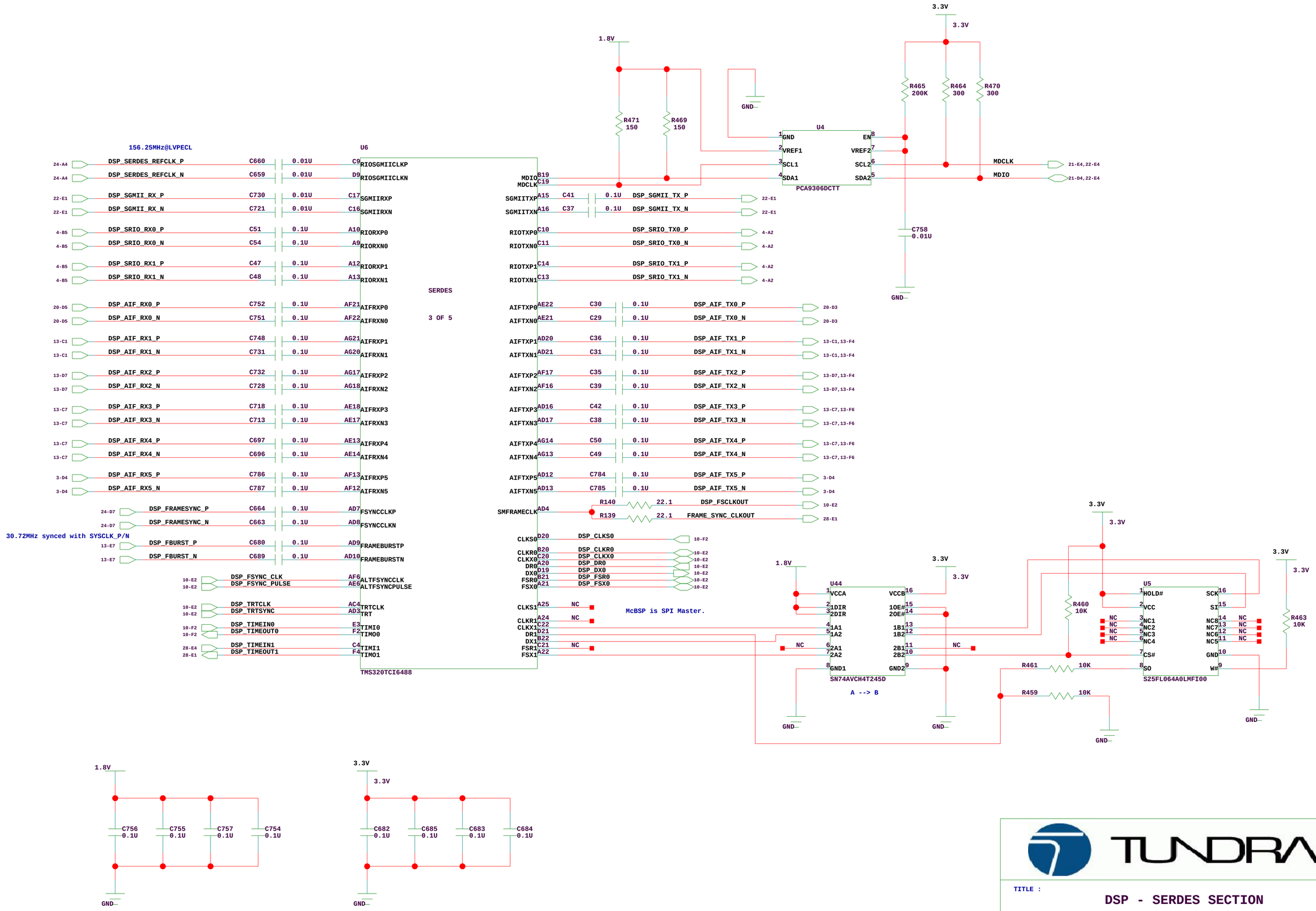
DSP - SERDES Section: AIF, SGMII, sRIO, and S-Flash



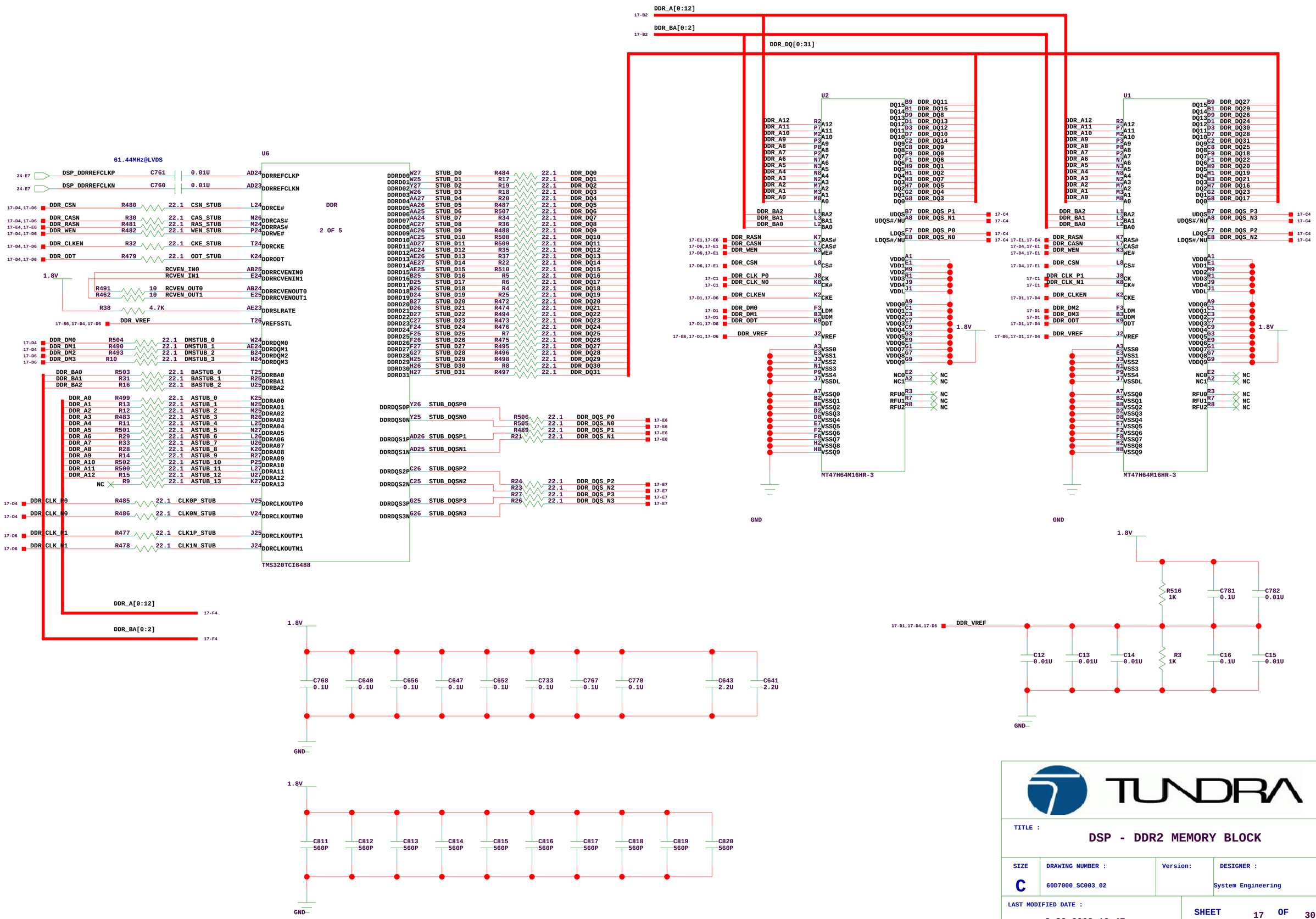
TUNDRA

TITLE : DSP - SERDES SECTION

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE : 3-30-2009_16:47

DSP - DDR2 Memory Block



TUNDRA

TITLE : DSP - DDR2 MEMORY BLOCK

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE : 3-30-2009_16:47

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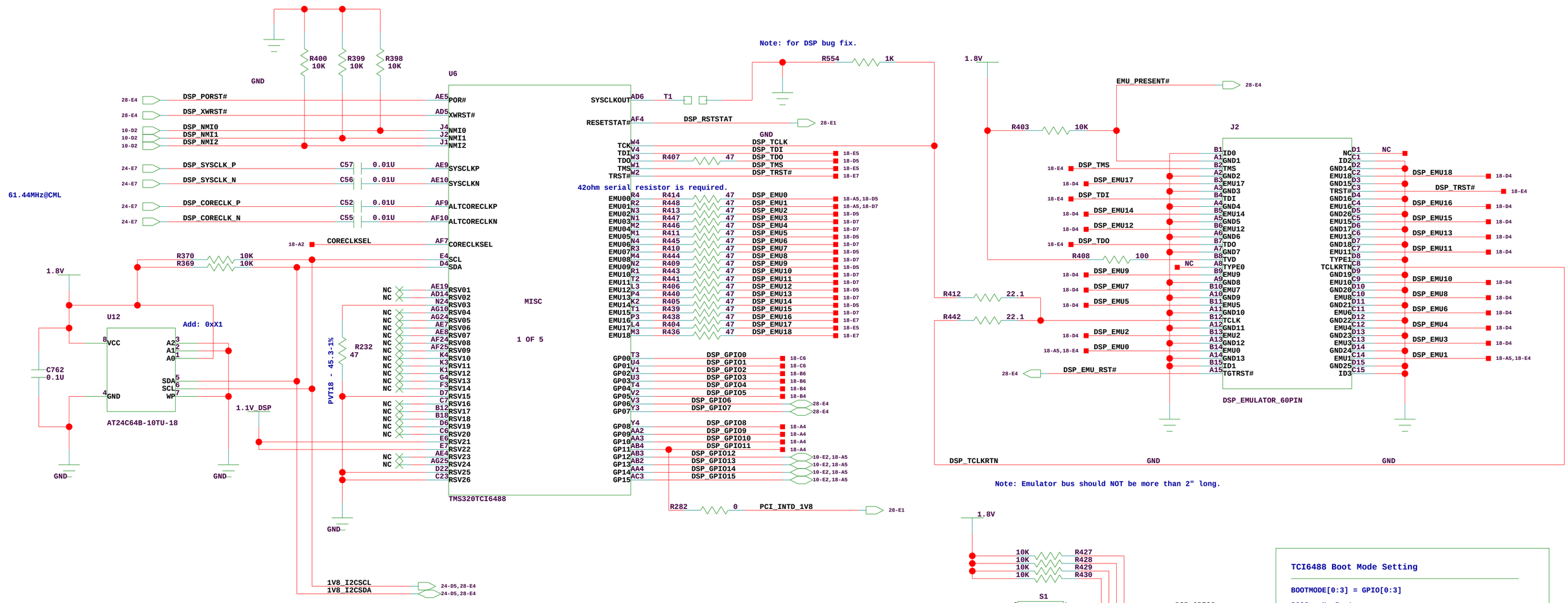
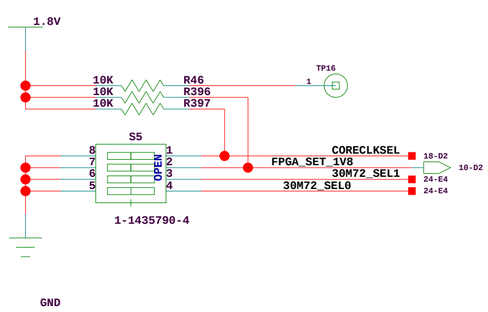
DSP - Emulator, GPIO, and Configuration

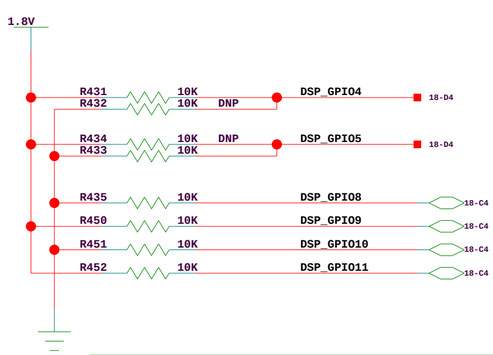


Notes:

-DSP_GPIO11 is Interrupt to PrPMC after Reset

-DSP_GPIO8 is TX_Disable to SFP1 via AFS600

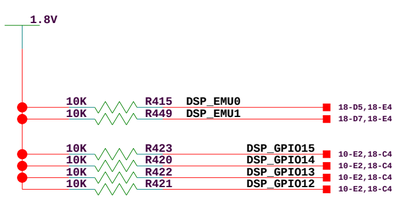


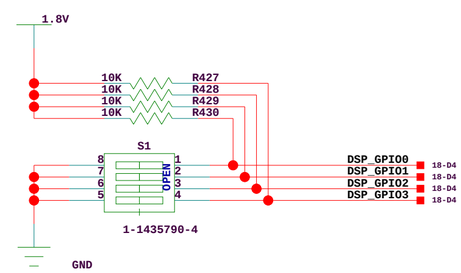


GPIO[11:8] = DEVNUM[3:0] = 1010 (0xA)

GPIO[4] = 1: Little Endian

GPIO[5] = 0: Asymmetric L2 Configuration





TCI6488 Boot Mode Setting

BOOTMODE[0:3] = GPIO[0:3]

0000 - No Boot
1000 - I2C Master Boot A (N/A)
0100 - I2C Master Boot B (0x51)
1100 - I2C Slave Boot

0010 - EMAC Master Boot
1010 - EMAC Slave Boot
0110 - EMAC Forced-Mode Boot
1110 - Reserved

0001 - sRIO Boot (N/A)
1001 - sRIO Boot (N/A))
0101 - sRIO Boot (CFG2 - 1.25G)
1101 - sRIO Boot (CFG3 - 3.125G)

TUNDRA

TITLE : DSP - CONFIGURATION

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE : 3-30-2009_16:47

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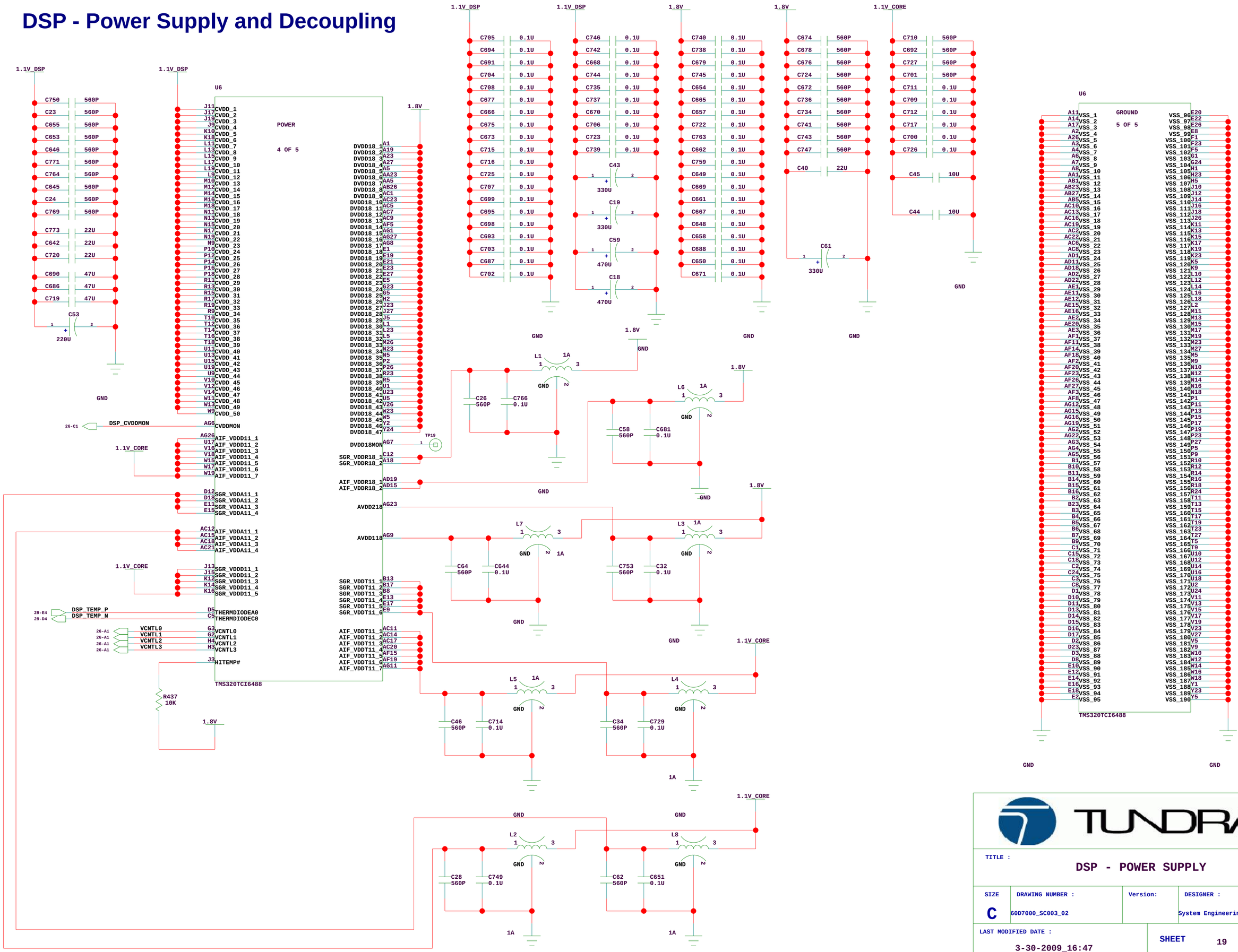
DSP - Power Supply and Decoupling



TITLE :

DSP - POWER SUPPLY

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE :

3-30-2009_16:47

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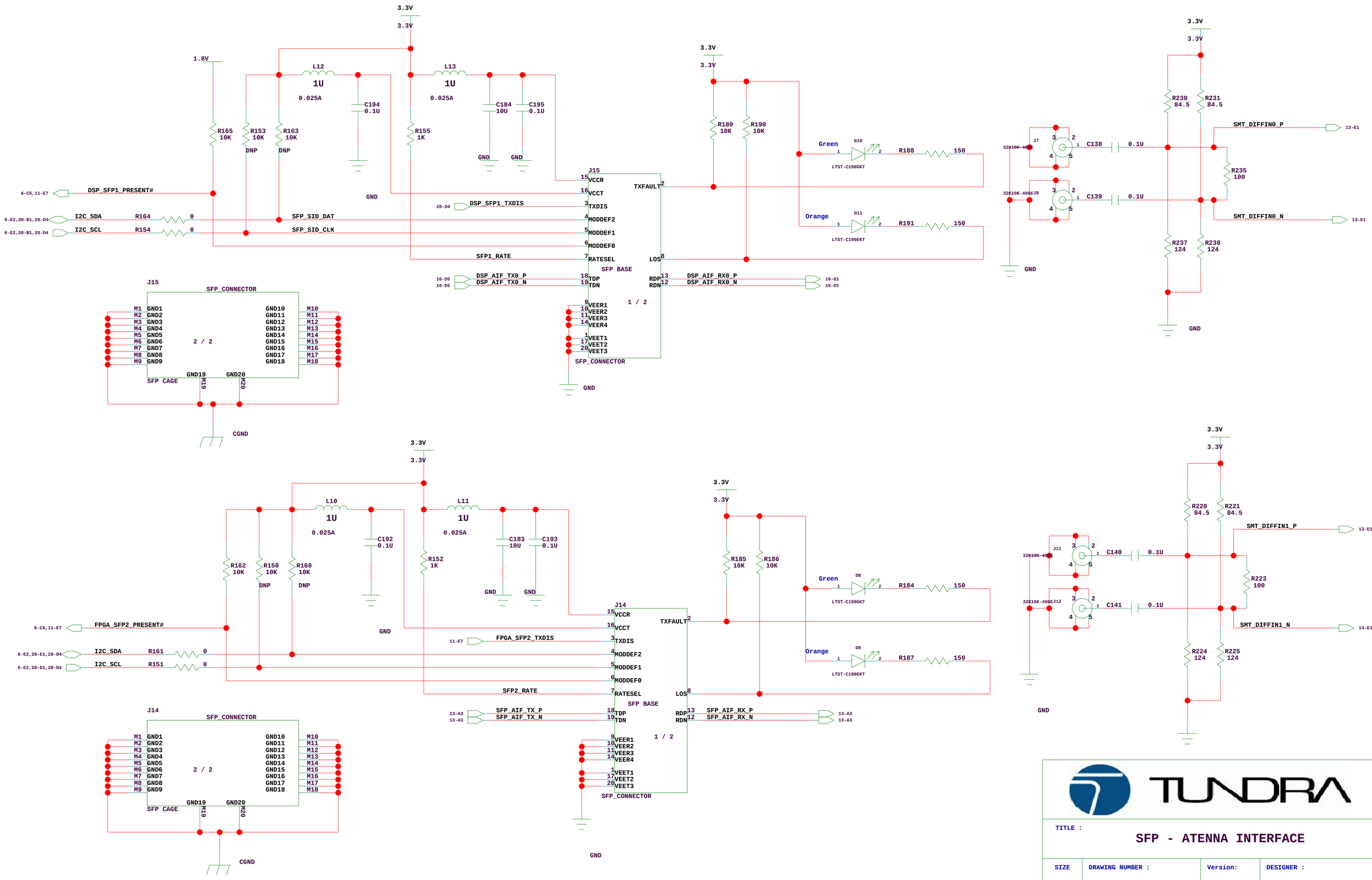
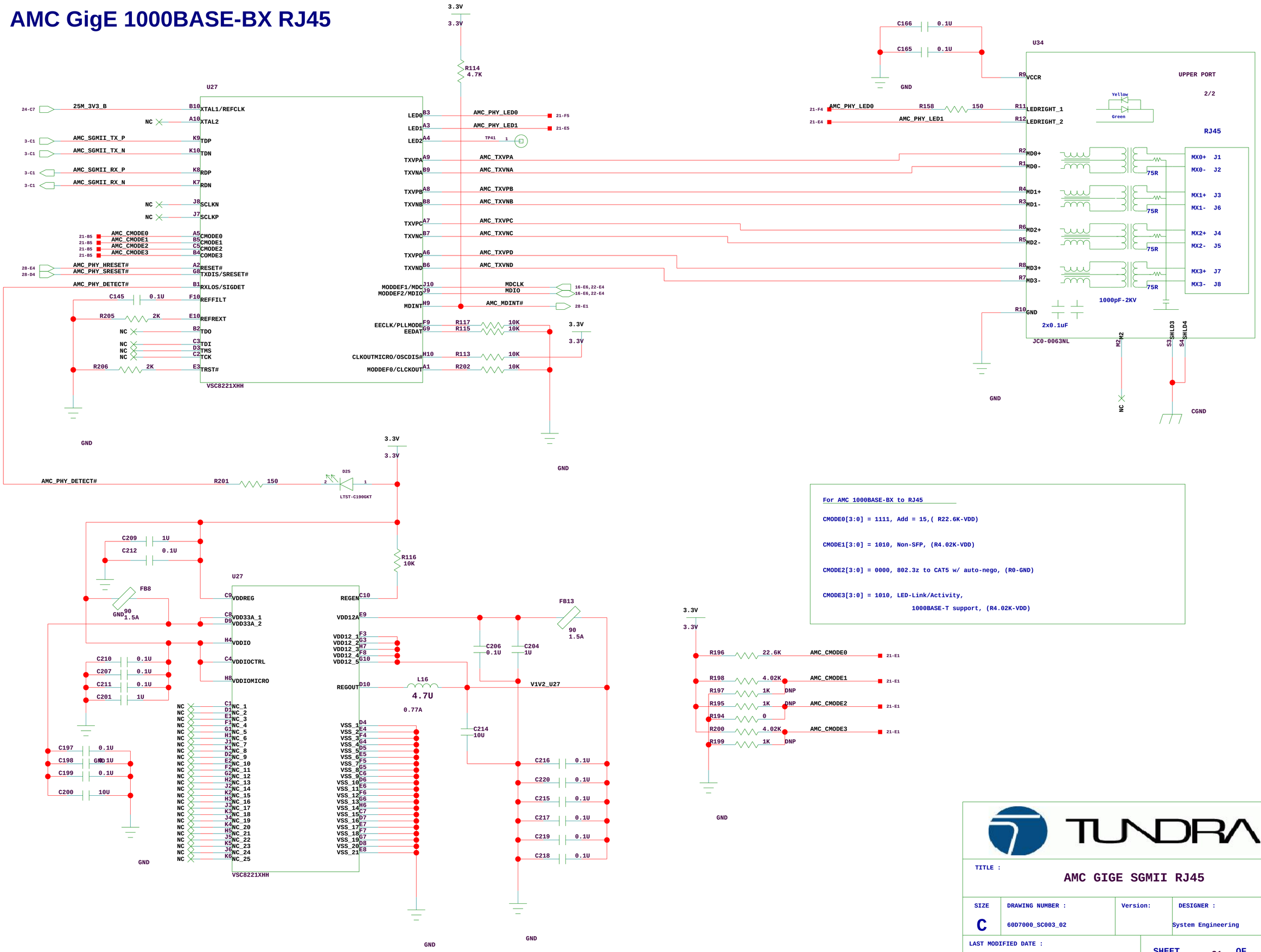
SFP Antenna Interface Connectors



TUNDRA

TITLE :			
SFP - ATENNA INTERFACE			
SIZE: C	DRAWING NUMBER : 60D7000_SC003_02	Version:	DESIGNER : System Engineering
LAST MODIFIED DATE : 3-30-2009_16:47		SHEET 20 OF 30	

AMC GigE 1000BASE-BX RJ45



For AMC 1000BASE-BX to RJ45

CMODE0[3:0] = 1111, Add = 15,(R22.6K-VDD)

CMODE1[3:0] = 1010, Non-SFP, (R4.02K-VDD)

CMODE2[3:0] = 0000, 802.3z to CAT5 w/ auto-nego, (R0-GND)

CMODE3[3:0] = 1010, LED-Link/Activity,
1000BASE-T support, (R4.02K-VDD)

TUNDRA

TITLE : AMC GIGE SGMII RJ45

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE : 3-30-2009_16:47

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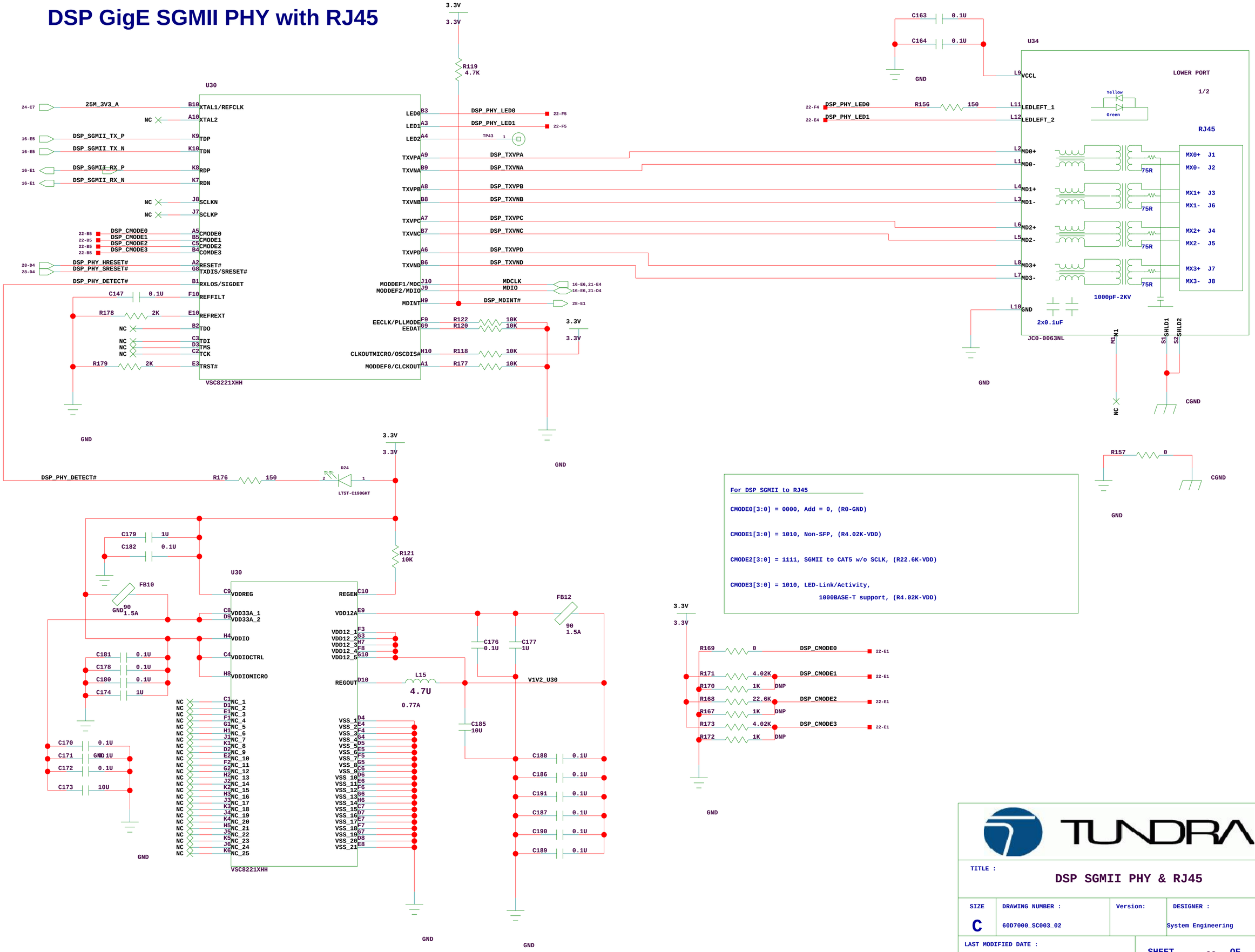
DSP GigE SGMII PHY with RJ45



For DSP SGMII to RJ45

CMODE0[3:0] = 0000, Add = 0, (R0-GND)

CMODE1[3:0] = 1010, Non-SFP, (R4.02K-VDD)

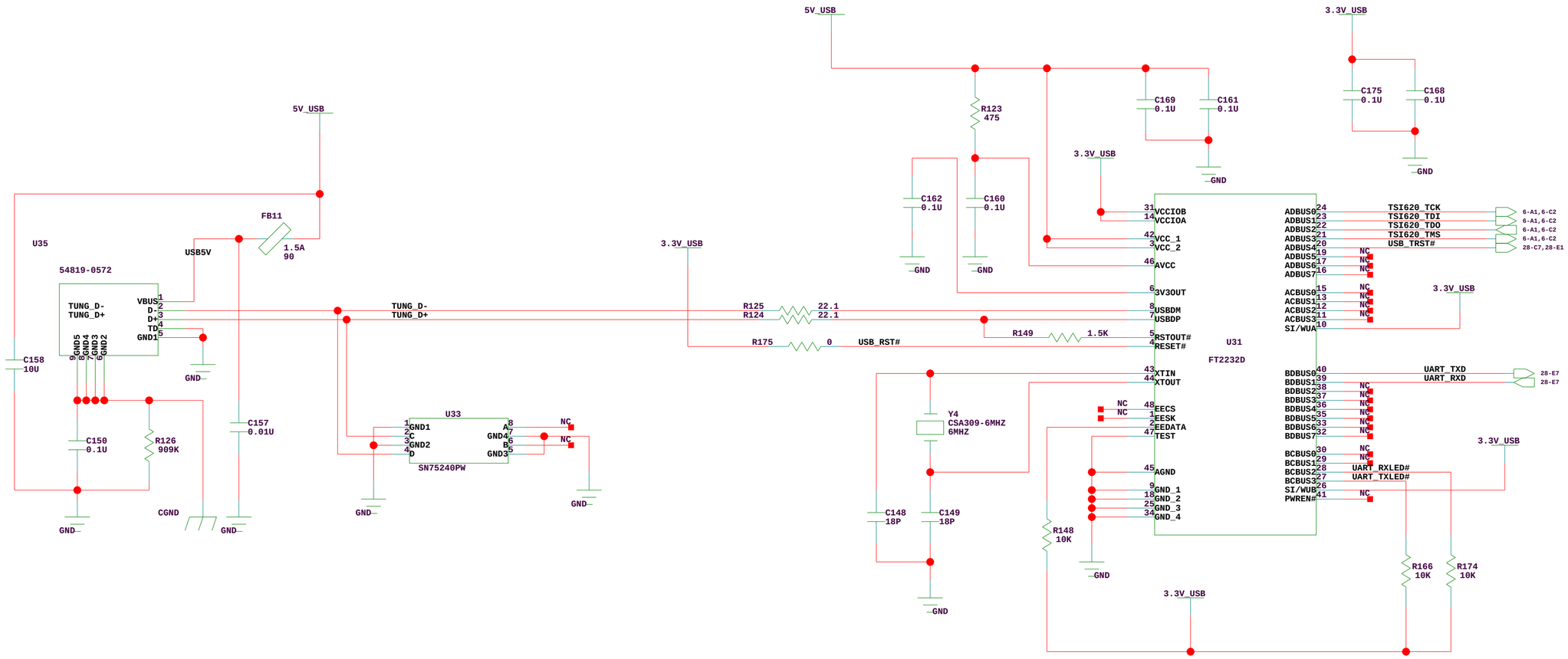
CMODE2[3:0] = 1111, SGMII to CAT5 w/o SCLK, (R22.6K-VDD)

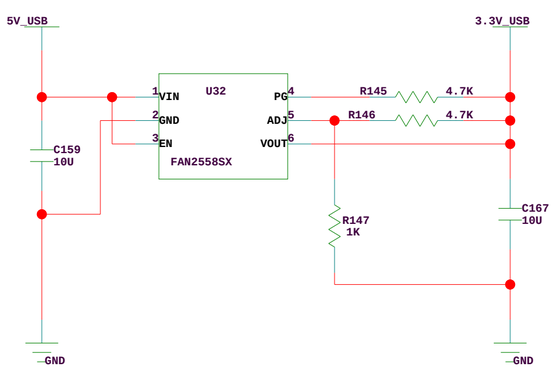
CMODE3[3:0] = 1010, LED-Link/Activity,
1000BASE-T support, (R4.02K-VDD)

TUNDRA

TITLE : DSP SGMII PHY & RJ45			
SIZE C	DRAWING NUMBER : 60D7000_SC003_02	Version:	DESIGNER : System Engineering
LAST MODIFIED DATE : 3-30-2009_16:47	SHEET 22 OF 30		

Tsi620 JTAG to USB





TUNDRA

TITLE :

USB TO TSI620 JTAG

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02	Rev 0	System Engineering

LAST MODIFIED DATE :

3-30-2009_16:47

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Clocking Distribution Block

NOTES:

1) 61.44MHz is Default Output

2) Y[0:4] Output is 61.44MHz

3) Y[5:9] Output is 30.72MHz

4) Y[5:9] Output Divider is 2 Changed by I2C

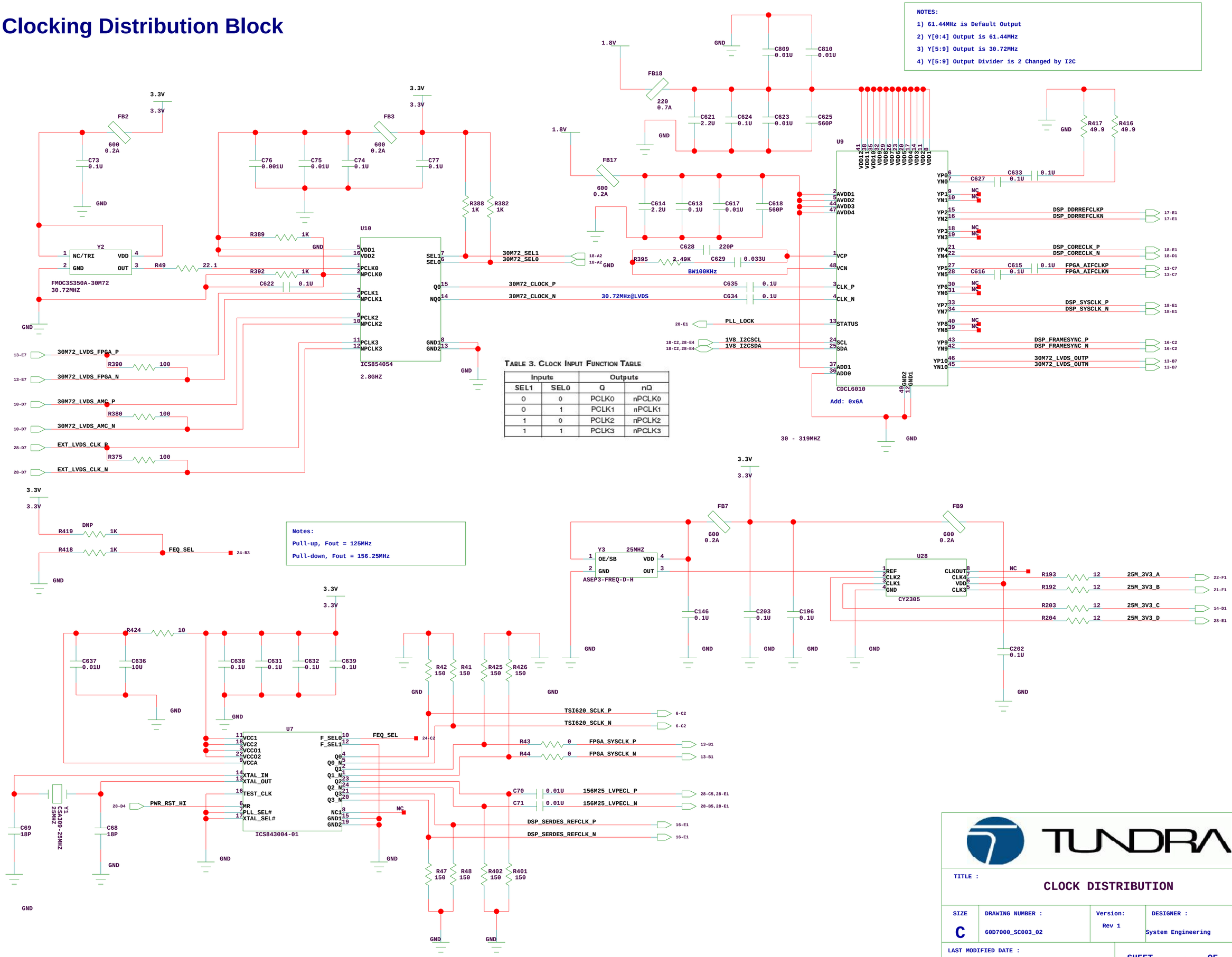

Table 3. Clock Input Function Table

Inputs		Outputs	
SEL1	SEL0	Q	nQ
0	0	PCLK0	nPCLK0
0	1	PCLK1	nPCLK1
1	0	PCLK2	nPCLK2
1	1	PCLK3	nPCLK3

Notes:

Pull-up, Fout = 125MHz

Pull-down, Fout = 156.25MHz

TUNDRA

TITLE : CLOCK DISTRIBUTION

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02	Rev 1	System Engineering

LAST MODIFIED DATE : 3-30-2009_16:47

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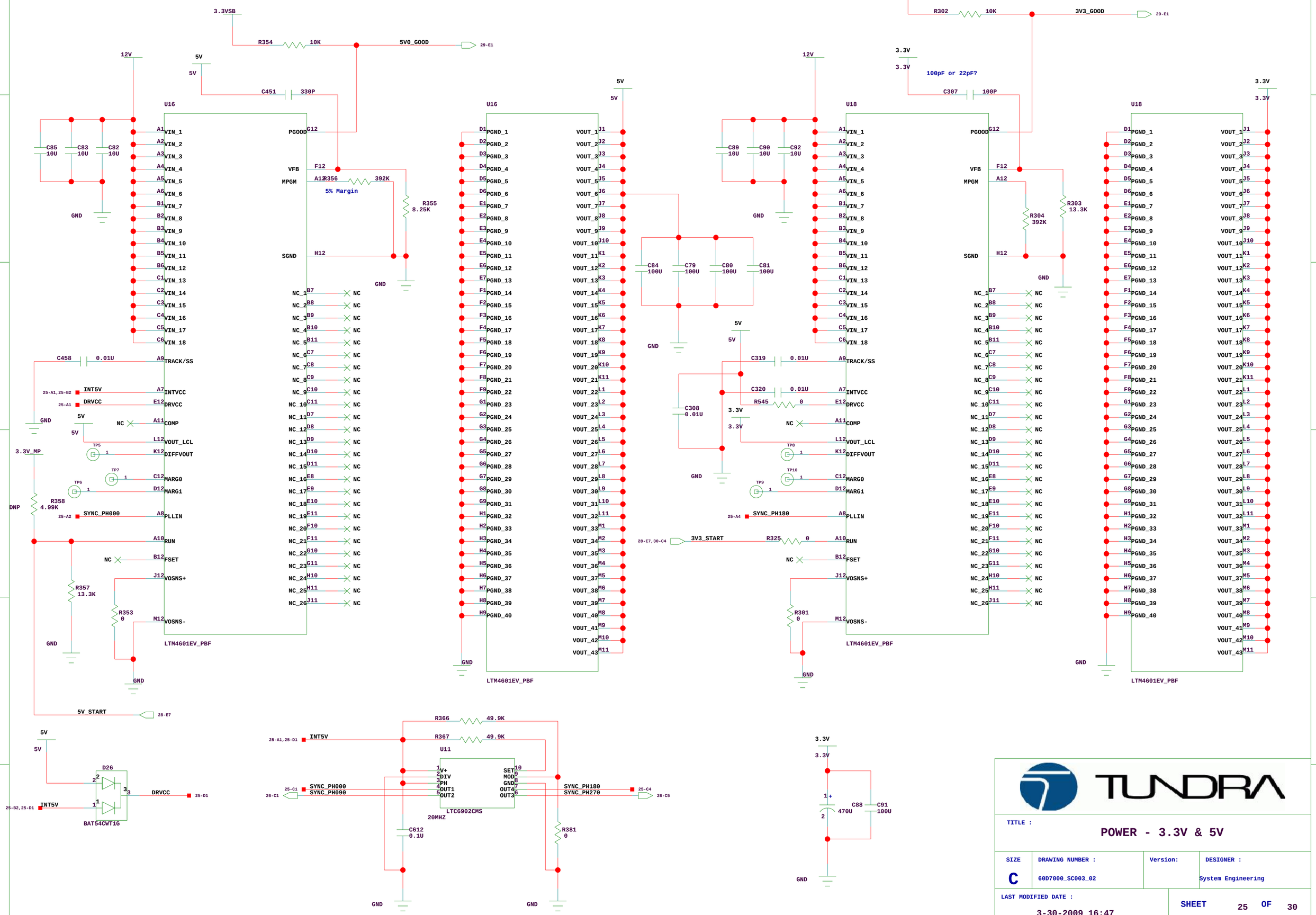
Power - 5V and 3.3V



TUNDRA

TITLE :

POWER - 3.3V & 5V

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE :

3-30-2009_16:47

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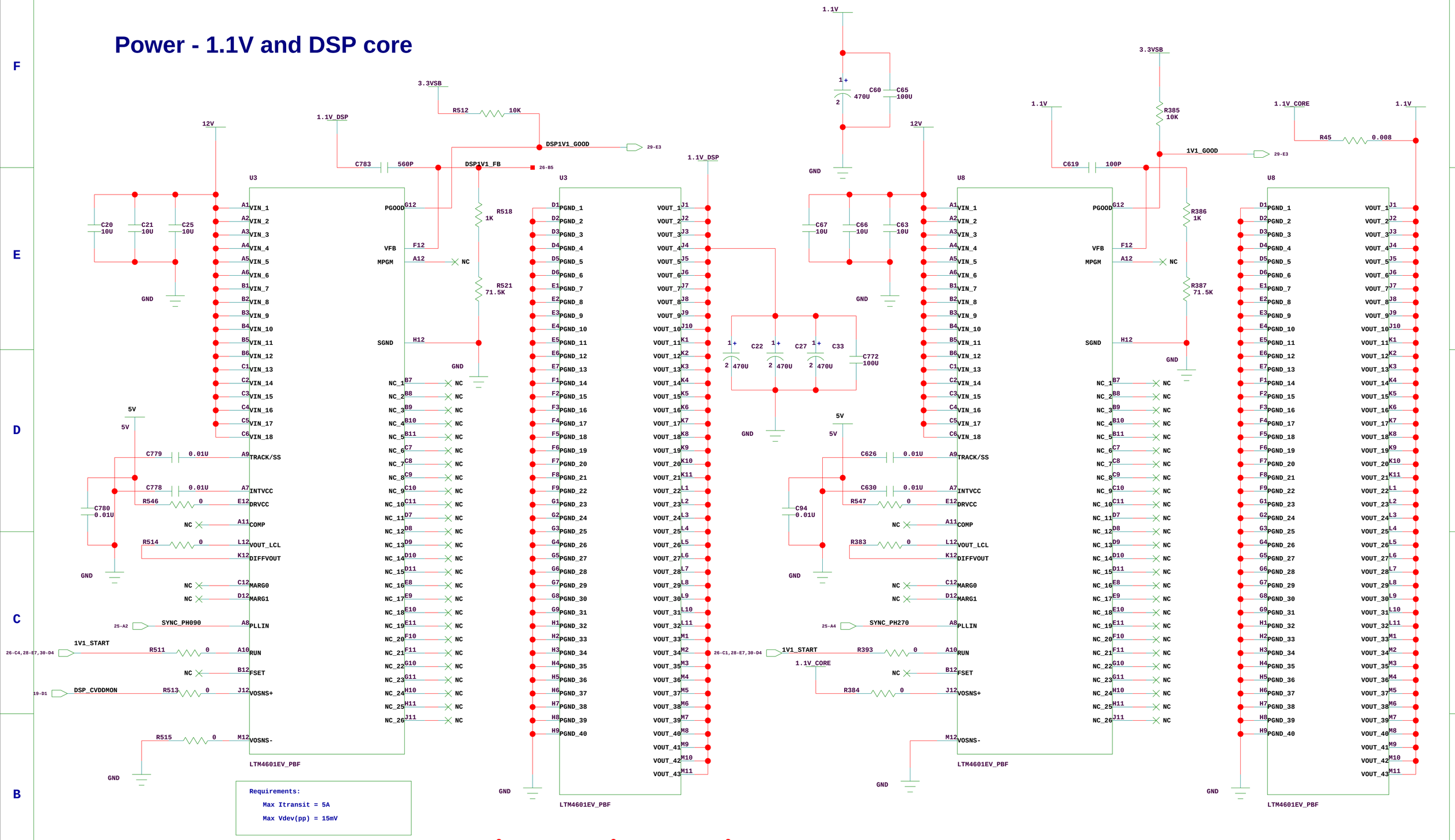
Power - 1.1V and DSP core



TUNDRA

TITLE : POWER - 1.1V & DSP_1.1V

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE : 3-30-2009_16:46

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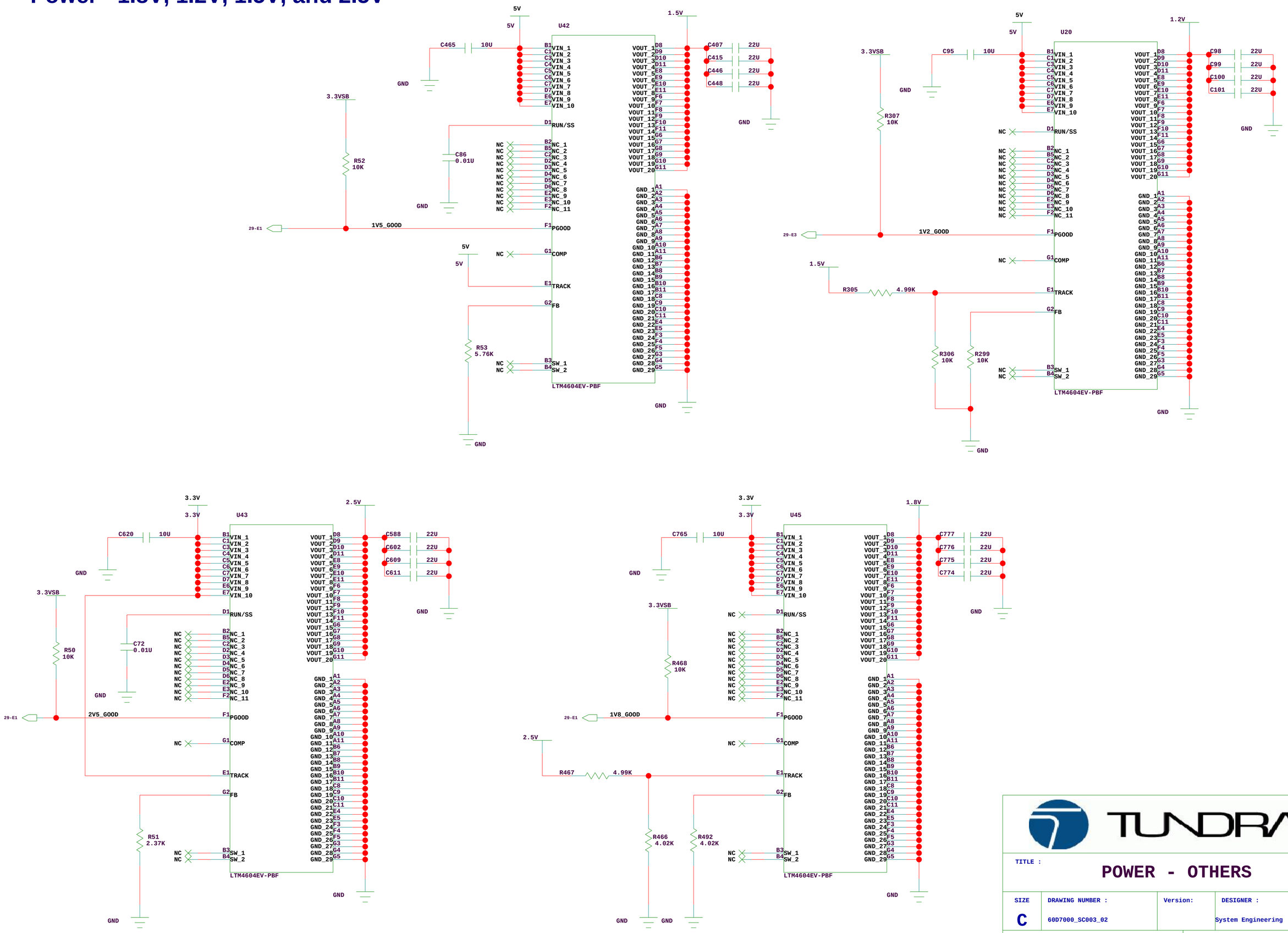
Power - 1.8V, 1.2V, 1.5V, and 2.5V



TUNDRA

TITLE : POWER - OTHERS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02		System Engineering

LAST MODIFIED DATE : 3-30-2009_16:46

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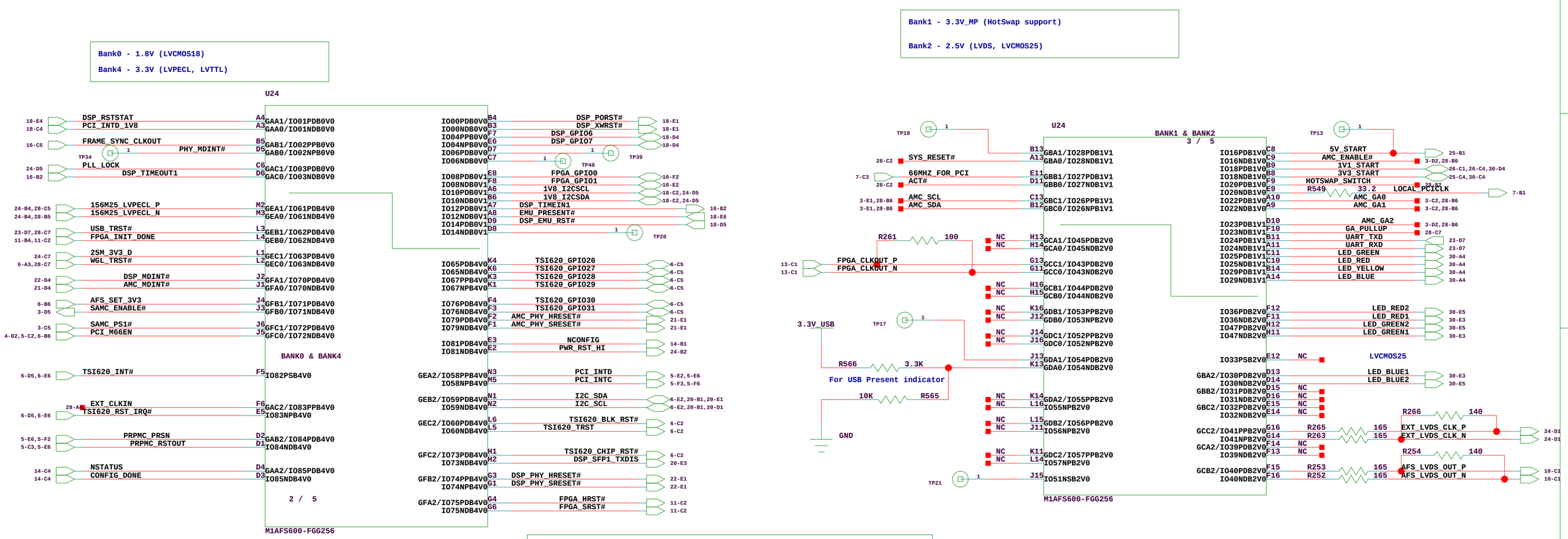
System Controller: Digital Block



TUNDRA

TITLE : AFS600 - DIGITAL BLOCK

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02	Rev 1	System Engineering

LAST MODIFIED DATE : 3-30-2009_16:46

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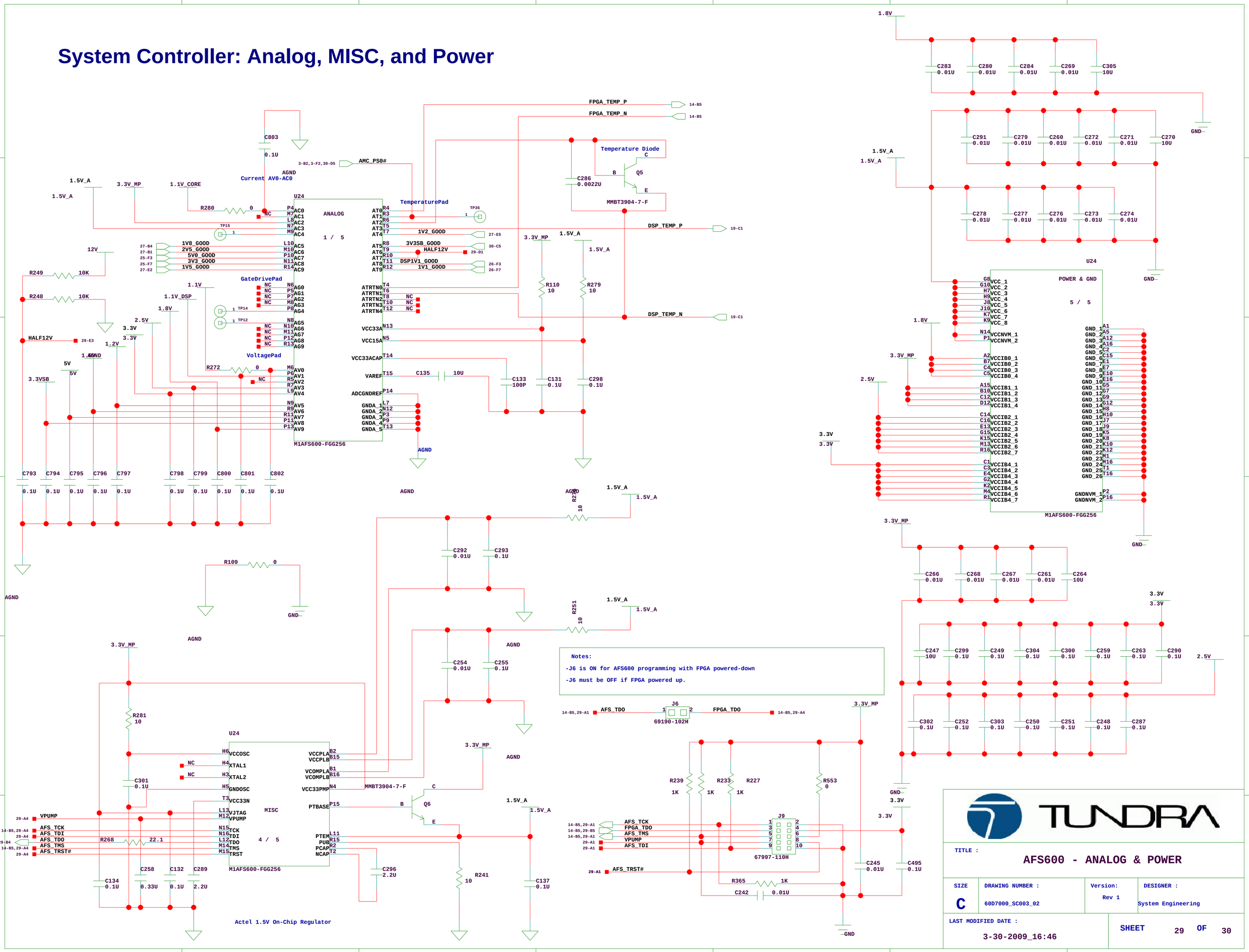
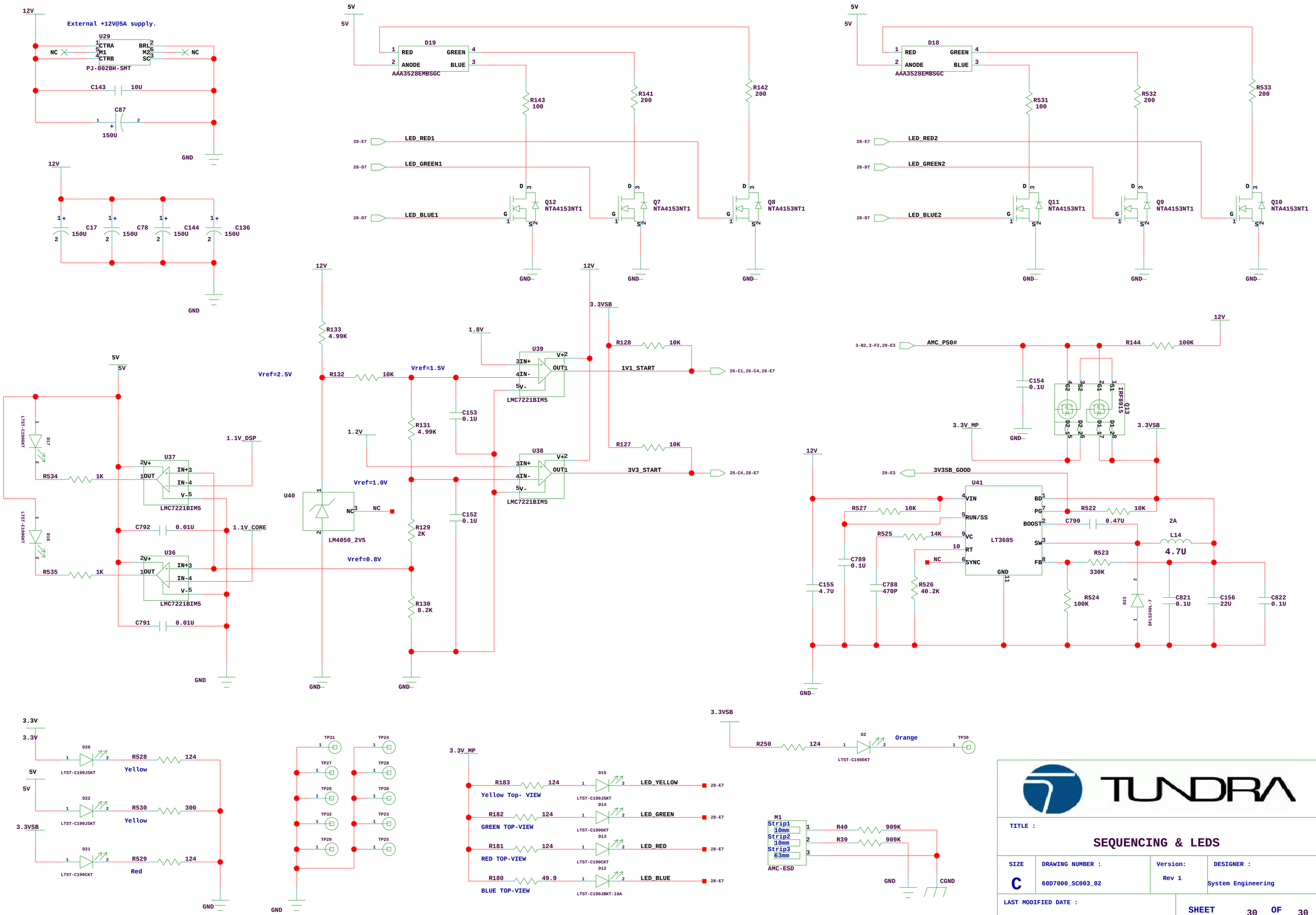
System Controller: Analog, MISC, and Power



Sequencing Control, LEDs, and Management Power



TUNDRA

TITLE :

SEQUENCING & LEDS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60D7000_SC003_02	Rev 1	System Engineering

LAST MODIFIED DATE : 3-30-2009_16:46

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