Engineering Change Notice

The following table contains a list of engineering changes that are not reflected in the Tsi381 Evaluation Board Schematics.

Table 1: ECN for E2000_AS001_05 (Board order number Tsi381-RDK1 V2.0)

No.	Item(s)	Original	Change To
1	Tsi381 Device	Tsi381-66ILZ1	Tsi381-66ILZ2
2	3.3Vaux on J1, J2, J36, J37[a]	No connection	Short pin A14 (3.3Vaux) to pin A16 (VIO_PCI) with 0-Ohm (0603) resistor

a. 3.3Vaux does not provide power to plug-in cards when the system is powered down.

Table 2: ECN for E2000_AS001_04 (Board order number Tsi381-RDK1 V2.1)

No.	Item(s)	Original	Change To
1	Tsi381 Device	Tsi381-66ILZ1	Tsi381-66ILZ2[a]
2	3.3Vaux on J1, J2, J36, J37[b]	No connection	Short pin A14 (3.3Vaux) to pin A16 (VIO_PCI) with 0-Ohm (0603) resistor

a. Ball K1 was removed from the Tsi381 device to allow the TEST_SPARE[2] signal to be detected as logic high. This version of the evaluation board is intended to support applications that require PCI bus parking on the Tsi381.

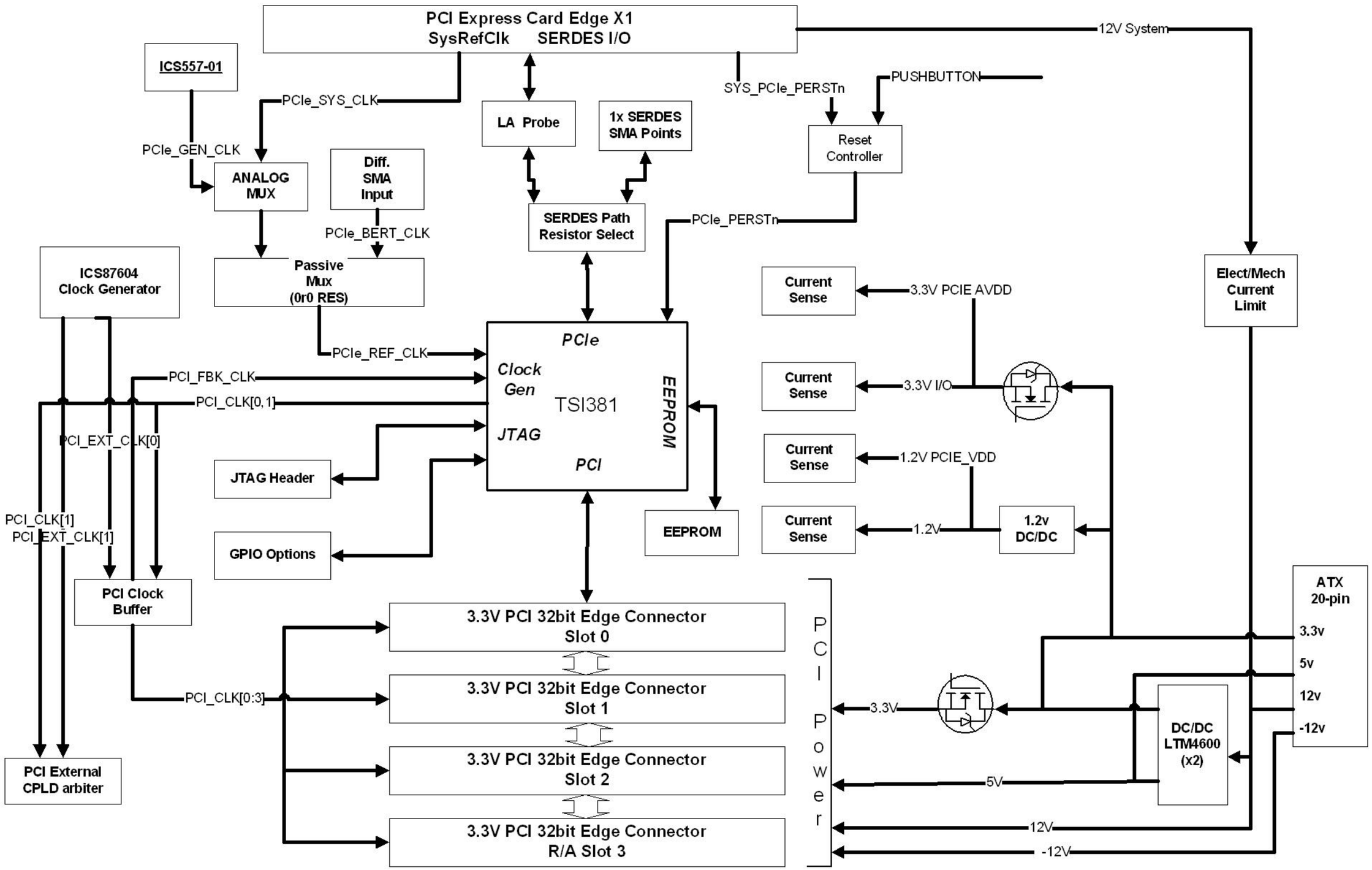
b. 3.3Vaux does not provide power to plug-in cards when the system is powered down.

Tsi381 Evaluation Board Schematic

TABLE OF CONTENTS

TITLE : TABLE OF CONTENTS				
SIZE C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :	
LAST MODIFIED DATE : 7-24-2007_17:10	SHEET 1 OF 15			

BLOCK DIAGRAM



TITLE : BLOCK DIAGRAM			
SIZE C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 5-3-2007_11:54	SHEET 2 OF 15		

TSI381 PCIE/MISC INTERFACE

TSI381 STRAPS

S1 Default Configuration

Signal	(1=High,0=Low)
N/C	
PWRUP_EN_ARB	0
N/C	
PLL_BYPASS	0

3.3V
R137 8.2K
R157 8.2K
1-1435790-4
S6
PWRUP_EN_ARB
PWRUP_PLL_BYPASS
3-E3,15-C3
3-D3

TSI381

PCIE_RXD_P0 / PCIE_RXD_N0 (4-D7, 4-D7) → A8 PCIE_RXD_P / B7 PCIE_RXD_N
PCIE_REFCLK_P / PCIE_REFCLK_N (10-C7, 10-C7) → A6 / B6
TSI381_PERST# (3-B7,3-C4) → B12 PCIE_PERSTN
PWRUP_EN_ARB (3-F2,15-C3) → K11
PWRUP_PLL_BYPASS (3-F2) → M1
TSI381_SR_CLK → B2 SR_CLK
TSI381_SR_CSN → C4 SR_CSN
TSI381_SR_DIN → A2 SR_DIN
TSI381_SR_DOUT → A1 SR_DOUT
TSI381_TCK (3-B5) → M2 JTAG_TCK
TSI381_TDI (3-B5) → L3 JTAG_TDI
TSI381_TDO (3-B4) → L1 JTAG_TDO
TSI381_TMS (3-B5) → M12 JTAG_TMS
TSI381_TRST# (3-B5) → L10 JTAG_TRSTN
TSI381_TEST_BCE (3-D6) → C8 TEST_BCE
TSI381_TEST_BIDR_CTRL (3-D6) → B1 TEST_BIDR_CTL
TSI381_TEST_ON (3-D6) → A3 TEST_ON

U11
1 OF 3
PCIE, MISC

PCIE_TXD_P → B5
PCIE_TXD_N → A4

NC_4 → B9 NC
NC_3 → K9 NC
NC_2 → E8 NC
NC_1 → A9 NC

TEST_SPARE[0] → M11
TEST_SPARE[1] → D8
TEST_SPARE[2] → K1

TX Compliance Testing

PCIE_TXD_TSI_P0 (4-D1) / PCIE_TXD_TSI_N0 (4-D1)
0.1U C112, 0.1U C111
R162 DNP 49.9, R159 DNP 49.9

AT25640A-10PU-2 DNP

3.3V
R207 8.2K
R198 8.2K, R187 8.2K
C233 0.1U
U23
SCK, CS#, SI, SO, HOLD#, VCC, GND, WP#

AP_U1
115-13-308-41-001

TI381 JTAG

Test for IDT Only
3.3V
2K R150 DNP, 2K R148 DNP, 2K R158
TSI381_TEST_BCE (3-D2)
TSI381_TEST_ON (3-D2)
TSI381_TEST_BIDR_CTRL (3-D2)
2K R156, 2K R153
J21 69190-102H

RESET CONTROLLER

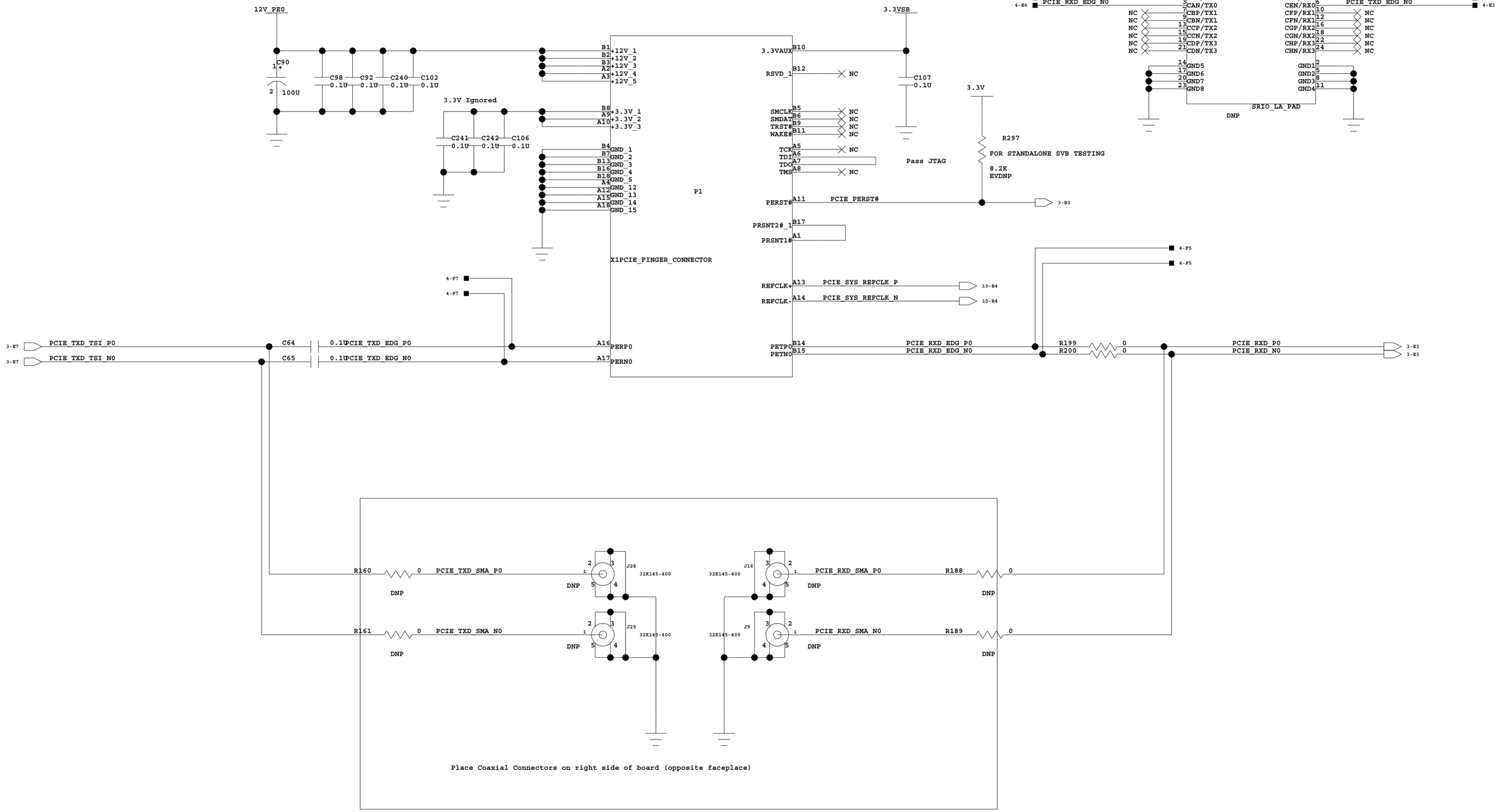
5V
R172 1K
B1, B2
SW2 EVQPAC07K
A1, A2
3.3V 5V
2.6V Threshold on SENSE
U15
VCC, SENSE, RESIN#, CT, RESET#, RESET, REF, GND
TL7702BCD
R173 1K
C231 1U
0.1U C73
3.3V
R136 1K
U16
5VCC
TSI381_PERST# → 3-B7,3-E3
NC7SZ08
PCIE_PERST# (4-E5)

TSI381_TDO (3-D2) → R296 33.2 → TSI381_TDI (3-D2)
TSI381_TCK (3-D2)
TSI381_TMS (3-D2)
TSI381_TRST# (3-D2)

2K R295, 2K R293, 2K R288, 2K R294
J22
5103309-3
C228 0.1U
U18
VCC5
TSI381_PERST# → 3-C4,3-E3
NC7SZ08

TITLE : Tsi381 PCIE/MISC			
SIZE: C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 7-24-2007_17:09		SHEET 3 OF 15	

PCIE CONNECTORS



TITLE : PCIE CONNECTORS			
SIZE C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 6-15-2007_14:56	SHEET 4 OF 15		

TSI381 PCI INTERFACE

VIO_PCI

R12 2.4K
R11 2.4K
R10 2.4K
R9 2.4K
R13 1K
R283 8.2K
R16 8.2K
R25 8.2K
R23 8.2K
R24 8.2K
R22 8.2K
R21 8.2K
R20 8.2K
R19 8.2K
R18 8.2K
R120 8.2K
R15 8.2K
R256 8.2K
R14 8.2K
R118 8.2K
R242 8.2K
R241 8.2K
R17 8.2K

6-C5,7-C5,8-C5,9-C5
6-C3,7-D3,8-C2,9-C2
6-D3,7-D3,8-D2,9-D2
6-D3,7-D3,8-D2,9-D2

PCI_CBE0 F1 PCI_CBEN[0]
PCI_CBE1 H3 PCI_CBEN[1]
PCI_CBE2 K5 PCI_CBEN[2]
PCI_CBE3 M8 PCI_CBEN[3]

9-D2,15-C2
6-D3,15-C2
7-B3,15-C2
8-D2,15-C2

PCI_REQ0# G11 PCI_REQN[0]
PCI_REQ1# H9 PCI_REQN[1]
PCI_REQ2# G12 PCI_REQN[2]
PCI_REQ3# H11 PCI_REQN[3]

9-D5,15-C2
6-D5,15-C2
7-B5,15-C2
8-D5,15-C2

PCI_GNT0# G10 PCI_GNTN[0]
PCI_GNT1# G9 PCI_GNTN[1]
PCI_GNT2# F11 PCI_GNTN[2]
PCI_GNT3# E11 PCI_GNTN[3]

6-D5,7-D5,8-D5,9-D5,15-C2
6-D3,7-D3,8-D2,9-D2,15-B2
6-D5,7-D5,8-D5,9-D5
6-D3,7-D3,8-D2,9-D2
6-D5,7-D5,8-D5,9-D5
6-D3,7-C2,9-D2
6-D3,7-D3,8-D2,9-D2
6-D5,7-D5,8-C5,9-D5

PCI_FRAME# M5 PCI_FRAMEN
PCI_IRDY# L5 PCI_IRDYN
PCI_TRDY# M4 PCI_TRDYN
PCI_DEVSEL# K4 PCI_DEVSELN
PCI_STOP# L4 PCI_STOPN
PCI_SERR# J2 PCI_SERRN
PCI_PERR# J3 PCI_PERRN
PCI_PAR J1 PCI_PAR

6-D5,7-E5,8-D5,9-D5
6-D3,7-D3,8-D2,9-D2

PCI_PME# H12 PCI_PMEN
PCI_LOCK# M3 PCI_LOCKN

PCI_M66EN D10 PCI_M66EN

6-E5,7-E5,8-D5,9-E5,15-D3

PCI_RST# F10 PCI_RSTN

6-E5,7-E3,8-E5,9-E2
6-E3,7-E5,8-E2,9-E5
6-E5,7-E3,8-E5,9-E2
6-E3,7-E5,8-E2,9-E5

PCI_INTA# E12 PCI_INTAN
PCI_INTB# E9 PCI_INTBN
PCI_INTC# D11 PCI_INTCN
PCI_INTD# E10 PCI_INTDN

10-B3 PCI_FBK_CLK D12 PCI_CLK

10-B1 PCI_INT_CLK0 R285 33.2 PCI_INT_CLK_STUB0 H10 PCI_CLKO[0]
10-A1 PCI_INT_CLK1 R284 33.2 PCI_INT_CLK_STUB1 C2 PCI_CLKO[1]

L11 NC_5
NC L12 NC_6
NC C12 NC_7

15-B5 GPIO0 C9 GPIO[0]
15-B5 GPIO1 A10 GPIO[1]
15-B5 GPIO2 B10 GPIO[2]
15-B5 GPIO3 A11 GPIO[3]

PLX has L11 PU to indicate forward bridge

TSI381
U11
PCI
2 OF 3

PCI_AD[0] D3 PCI_AD0
PCI_AD[1] C1 PCI_AD1
PCI_AD[2] D1 PCI_AD2
PCI_AD[3] D2 PCI_AD3
PCI_AD[4] E1 PCI_AD4
PCI_AD[5] E2 PCI_AD5
PCI_AD[6] E3 PCI_AD6
PCI_AD[7] E4 PCI_AD7
PCI_AD[8] F2 PCI_AD8
PCI_AD[9] F3 PCI_AD9
PCI_AD[10] F4 PCI_AD10
PCI_AD[11] G1 PCI_AD11
PCI_AD[12] G2 PCI_AD12
PCI_AD[13] G3 PCI_AD13
PCI_AD[14] H1 PCI_AD14
PCI_AD[15] H2 PCI_AD15
PCI_AD[16] J5 PCI_AD16
PCI_AD[17] L6 PCI_AD17
PCI_AD[18] M6 PCI_AD18
PCI_AD[19] K6 PCI_AD19
PCI_AD[20] J6 PCI_AD20
PCI_AD[21] M7 PCI_AD21
PCI_AD[22] L7 PCI_AD22
PCI_AD[23] K7 PCI_AD23
PCI_AD[24] L8 PCI_AD24
PCI_AD[25] K8 PCI_AD25
PCI_AD[26] M9 PCI_AD26
PCI_AD[27] L9 PCI_AD27
PCI_AD[28] K12 PCI_AD28
PCI_AD[29] J11 PCI_AD29
PCI_AD[30] J12 PCI_AD30
PCI_AD[31] J10 PCI_AD31

PCI_AD[0:31] 6-D2,6-D6,6-D7,7-D2,7-D6,8-D2,8-D6,9-D2 9-D6

3.3V_384
R53 8.2K

3.3V_PCI
R282 392
REDMO-C150 D18

VIO_PCI
R85 8.2K

1-1435790-4
S1
6-C2,7-C2,8-C2,9-C2 SLOT_M66EN
NC NC NC NC

PCI_M66EN

U3
3.3V
5VCC
GND
NC7SZ08

VIO_PCI
5.1K R50 PCI_REQ64# 6-C5,7-C5,8-C5,9-C5
5.1K R51 PCI_ACK64# 6-C3,7-C3,8-C2,9-C2

TITLE : Tsi381 PCI INTERFACE

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2000_SC001_03	1.0	

LAST MODIFIED DATE : 7-24-2007_17:06

SHEET 5 OF 15

PCI SLOT 0 (R/A)

IDSEL AD16

- Required Interrupt Routing

  SLOT : BRIDGE

  INTA -> INTA

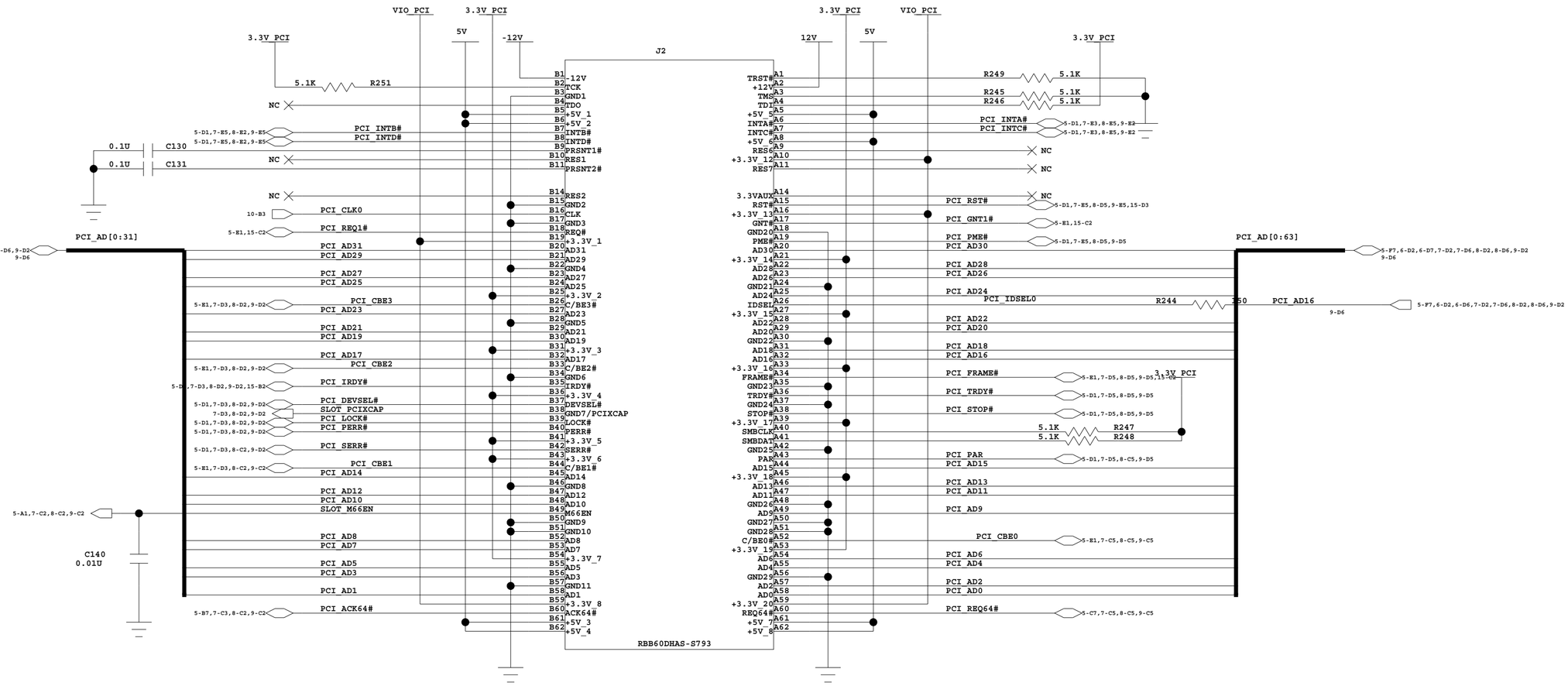
  INTB -> INTB

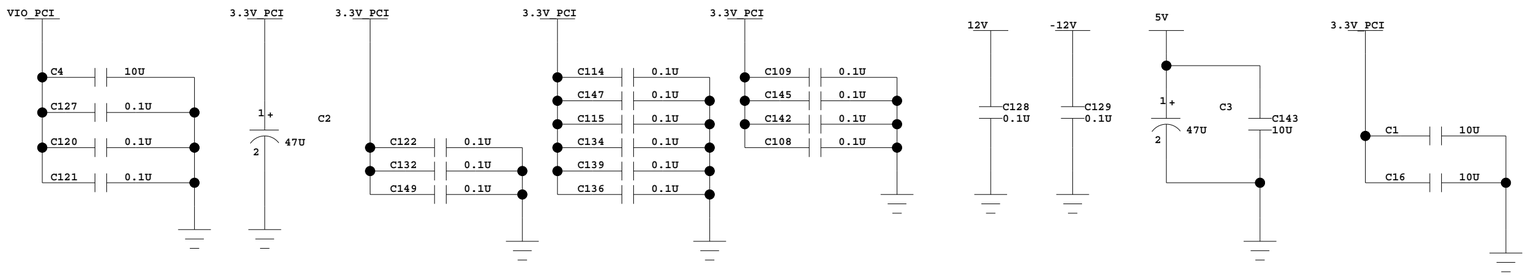
  INTC -> INTC

  INTD -> INTD

- PCI Clock PCI_CLK0

- PCI Arbitration PCI_GNT#1/PCI_REQ#1





TITLE : PCI SLOT 0

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2000_SC001_03	1.0	

LAST MODIFIED DATE : 7-25-2007_15:13

SHEET 6 OF 15

PCI SLOT 1 (Vertical)

IDSEL AD17

- Required Interrupt Routing

  SLOT : BRIDGE

  INTA -> INTB

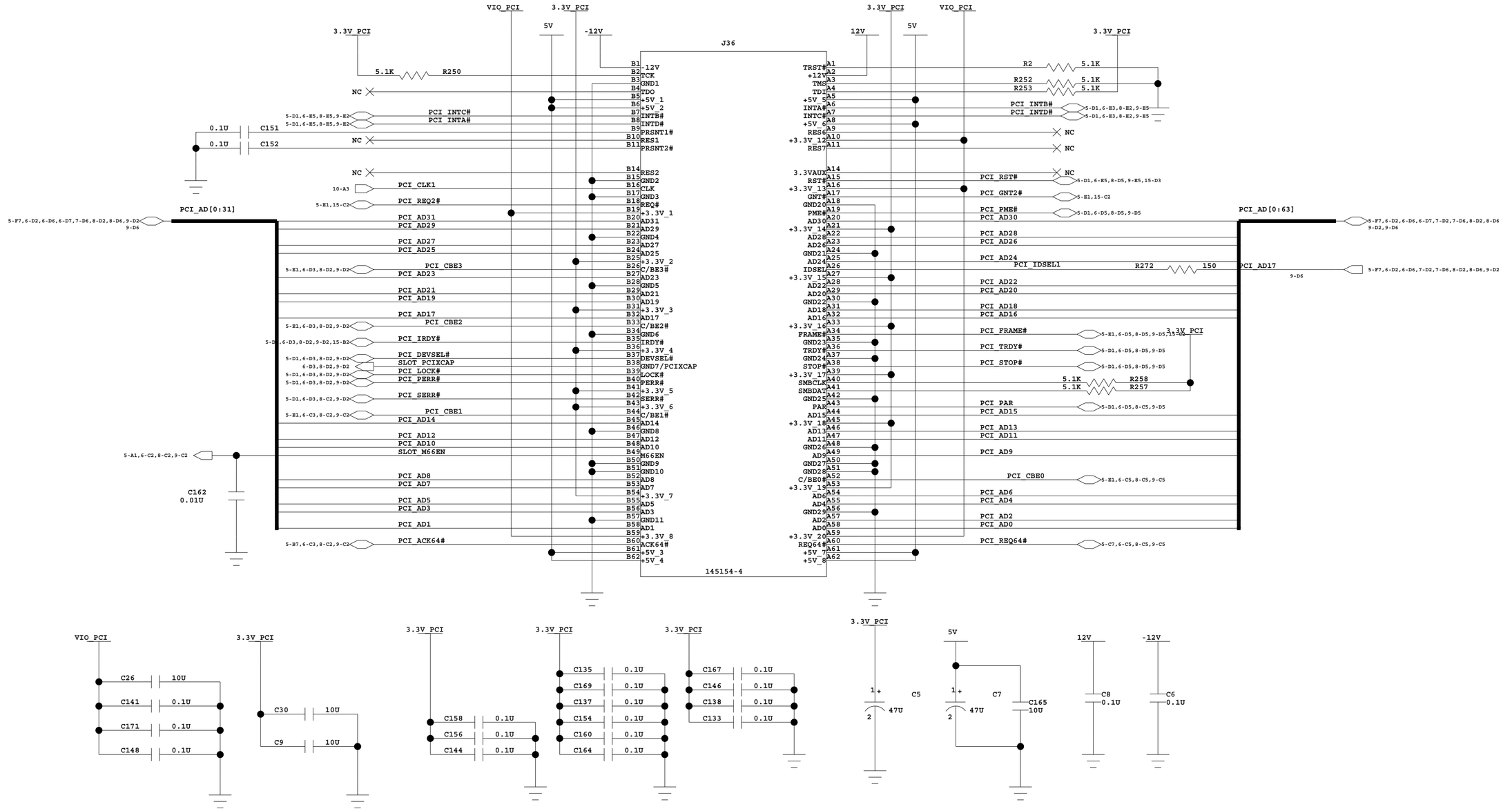
  INTB -> INTC

  INTC -> INTD

  INTD -> INTA

- PCI Clock PCI_CLK1

- PCI Arbitration PCI_GNT#2/PCI_REQ#2



TITLE : PCI SLOT 1			
SIZE: C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 7-25-2007_15:13	SHEET 7 OF 15		

PCI SLOT 3 (Vertical)

IDSEL AD18

- Required Interrupt Routing

  SLOT : BRIDGE

  INTA -> INTC

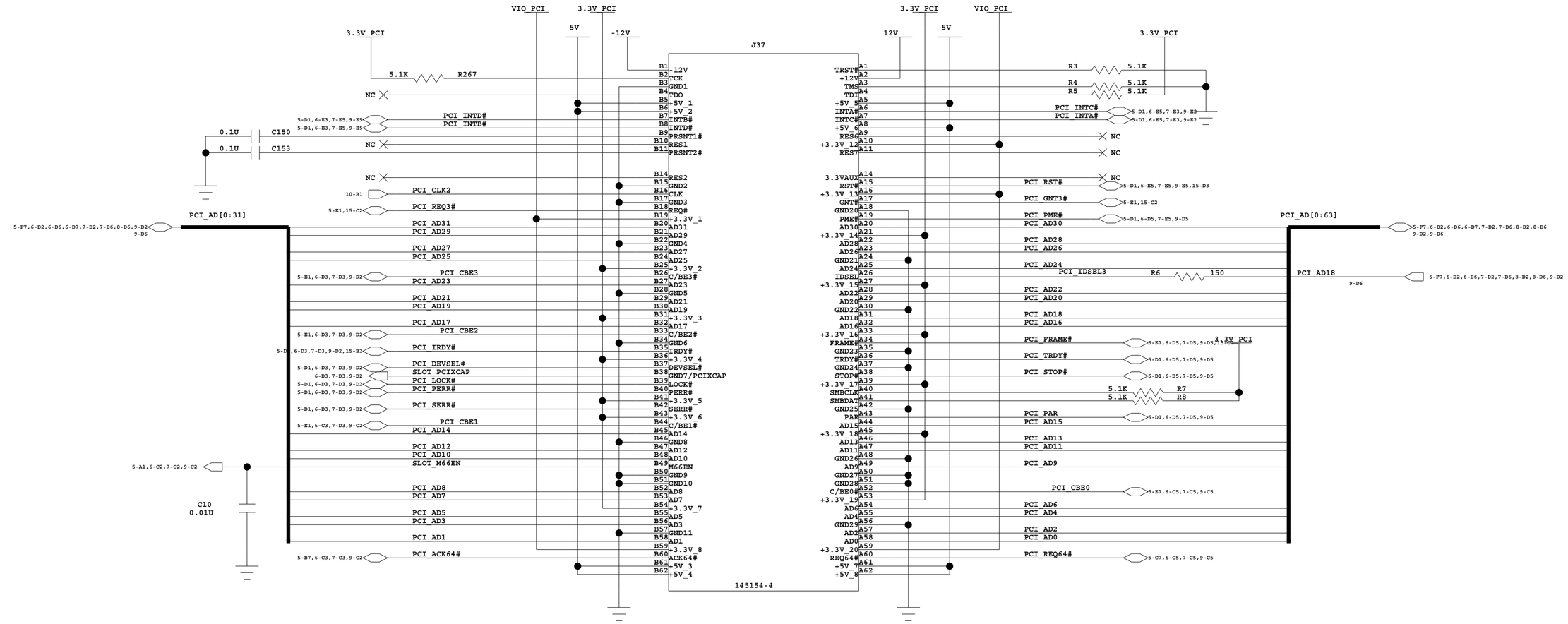
  INTB -> INTD

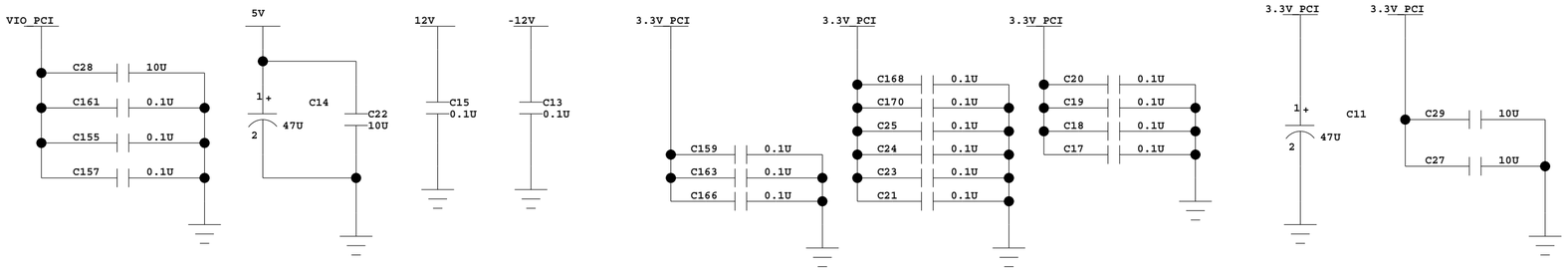
  INTC -> INTA

  INTD -> INTB

- PCI Clock PCI_CLK2

- PCI Arbitration PCI_GNT#3/PCI_REQ#3





TITLE : PCI SLOT 3			
SIZE: C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 7-25-2007_15:14	SHEET 8 OF 15		

PCI SLOT 2 (Vertical)

IDSEL AD19

- Required Interrupt Routing

  SLOT : BRIDGE

  INTA -> INTD

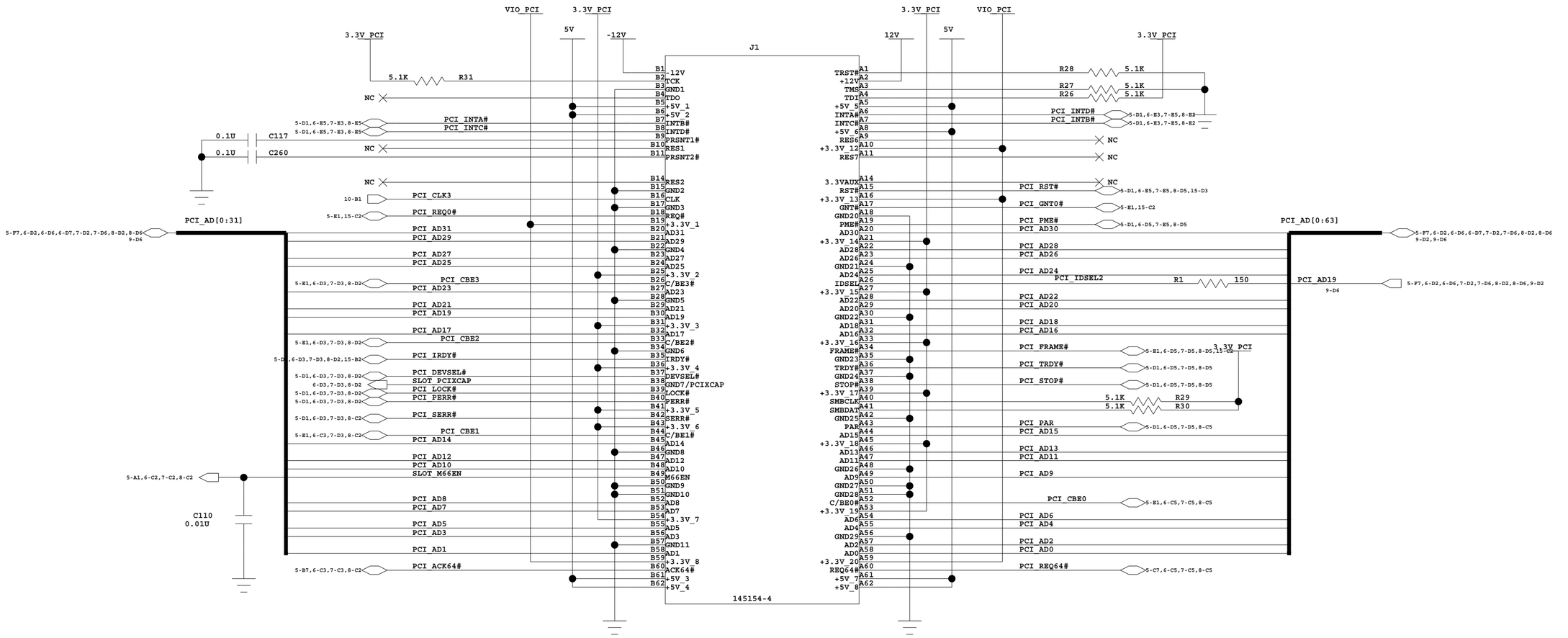
  INTB -> INTA

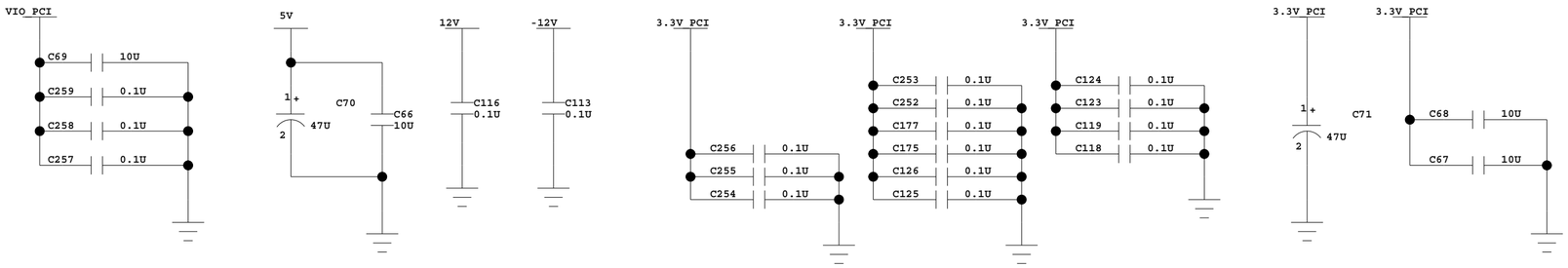
  INTC -> INTB

  INTD -> INTC

- PCI Clock PCI_CLK3

- PCI Arbitration PCI_GNT#0/PCI_REQ#0

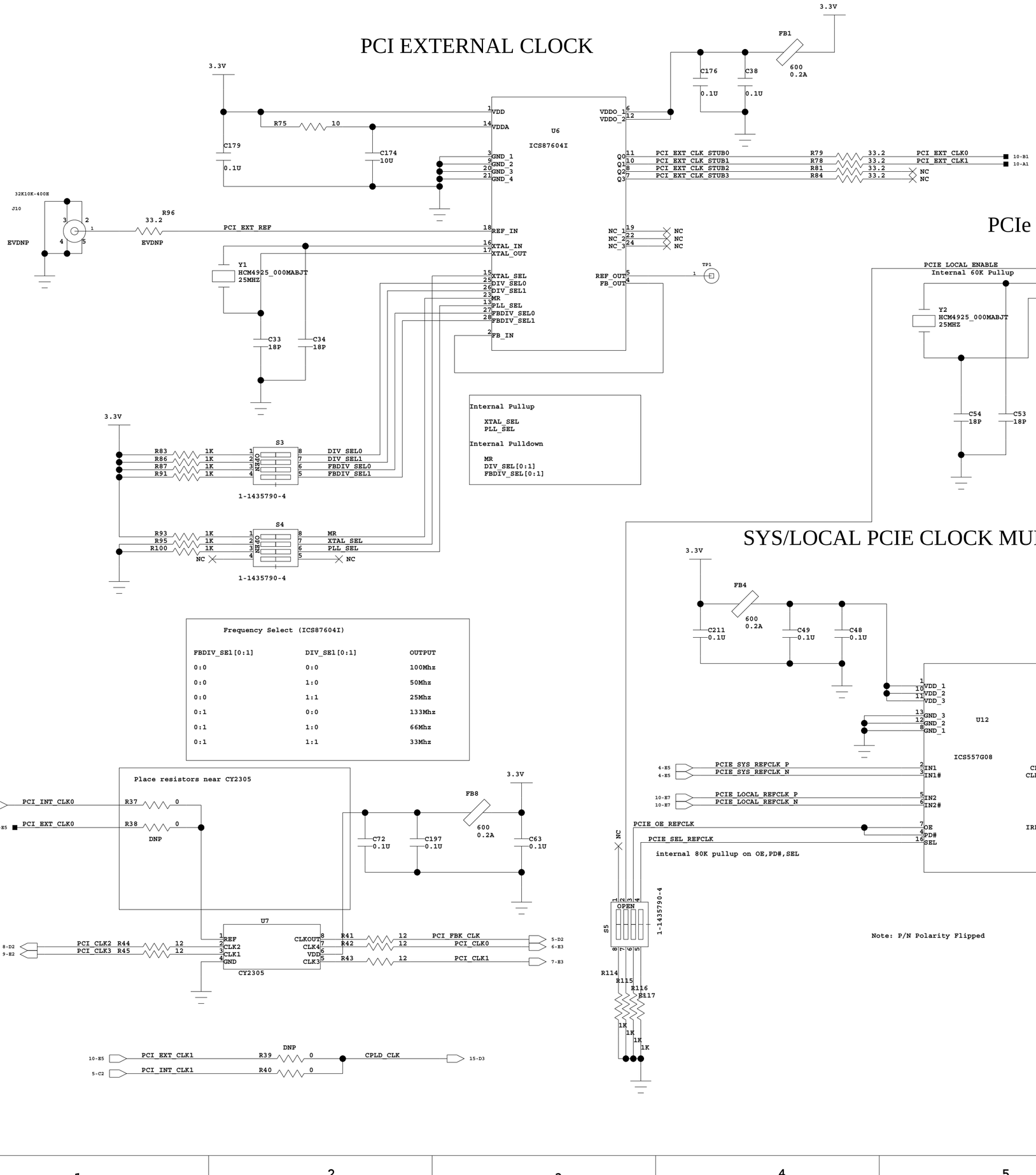




TITLE : PCI SLOT 2			
SIZE C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 7-25-2007_15:14	SHEET 9 OF 15		

CLOCK DISTRIBUTION

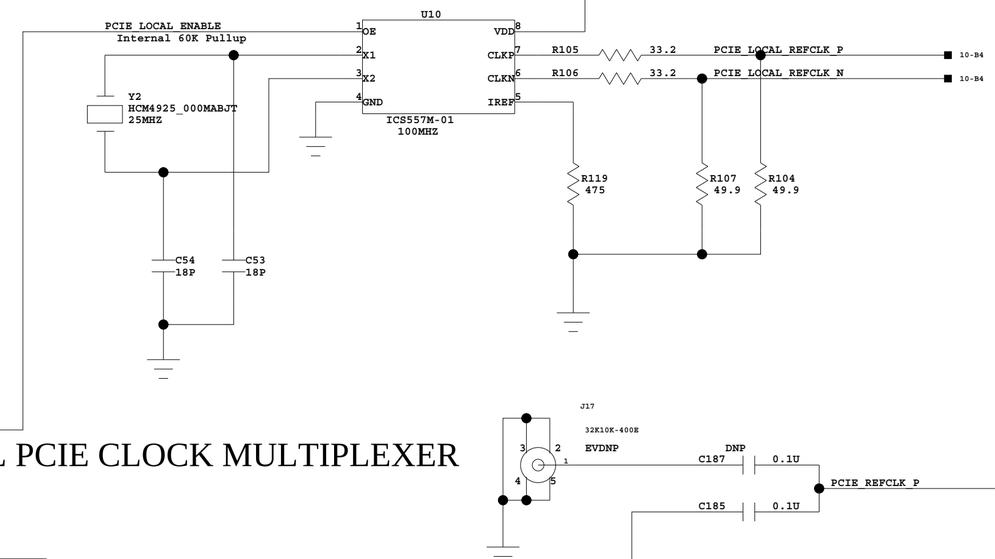
PCI EXTERNAL CLOCK



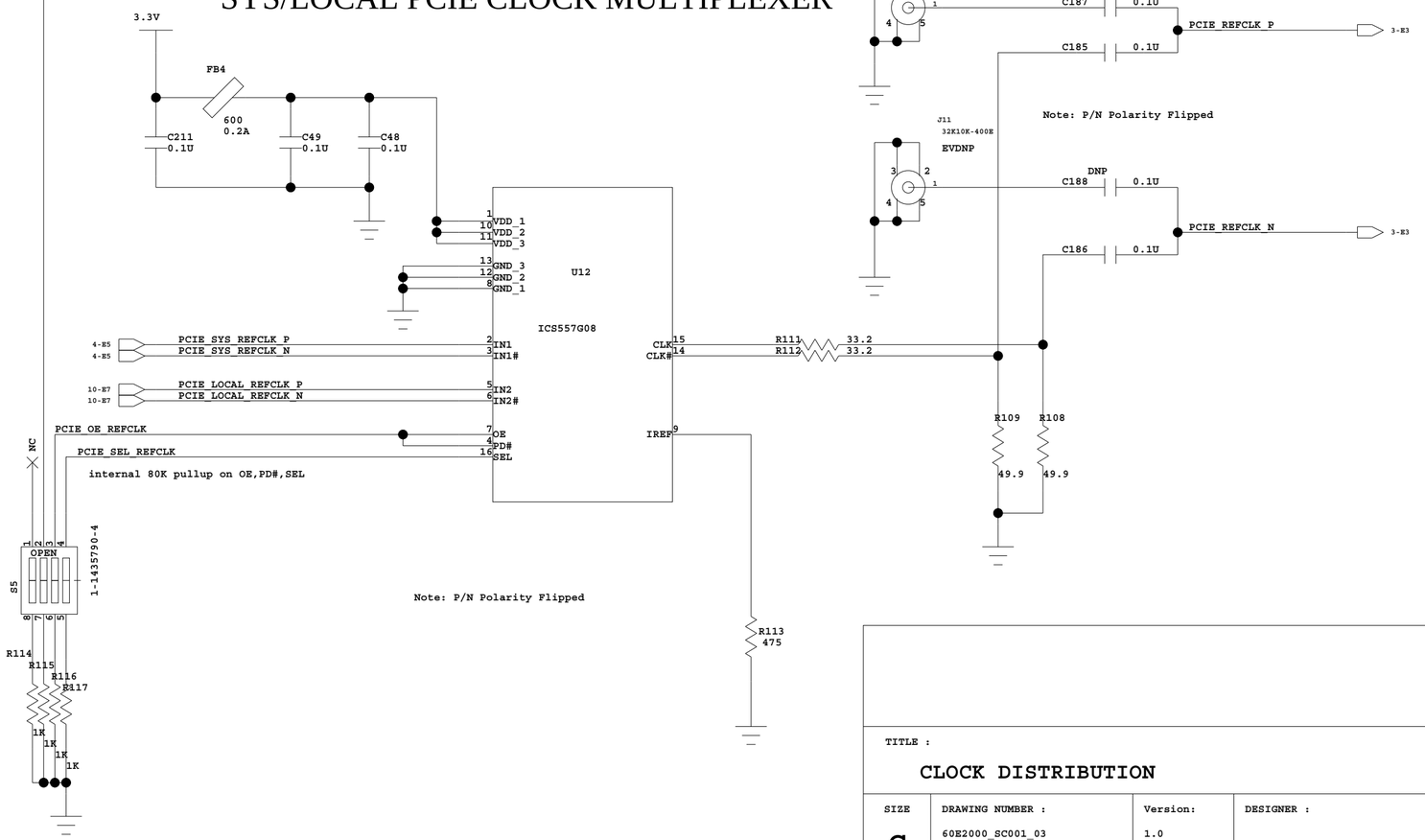
Frequency Select (ICS87604I)

FBDIV_SEl[0:1]	DIV_SEl[0:1]	OUTPUT
0:0	0:0	100Mhz
0:0	1:0	50Mhz
0:0	1:1	25Mhz
0:1	0:0	133Mhz
0:1	1:0	66Mhz
0:1	1:1	33Mhz

PCIe LOCAL CLOCKGEN



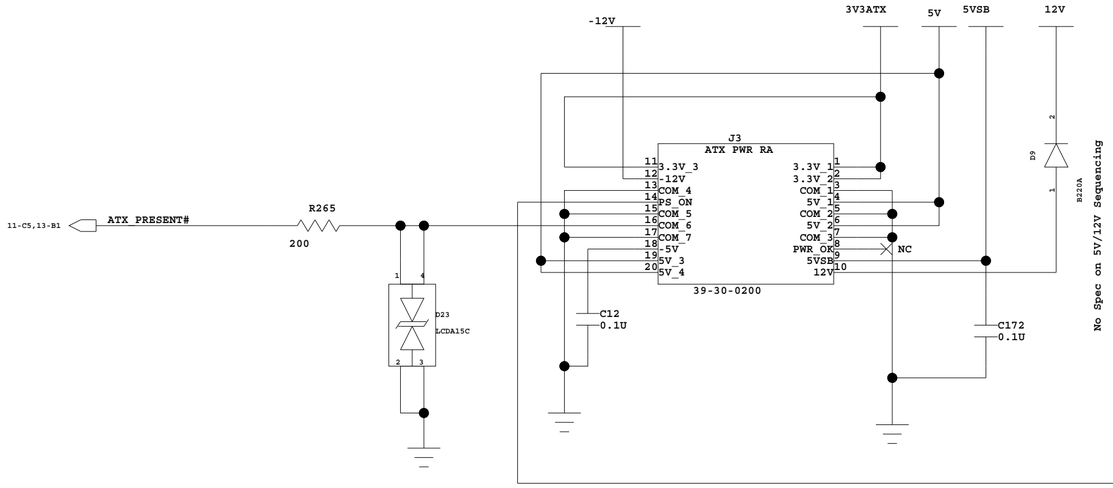
SYS/LOCAL PCIE CLOCK MULTIPLEXER



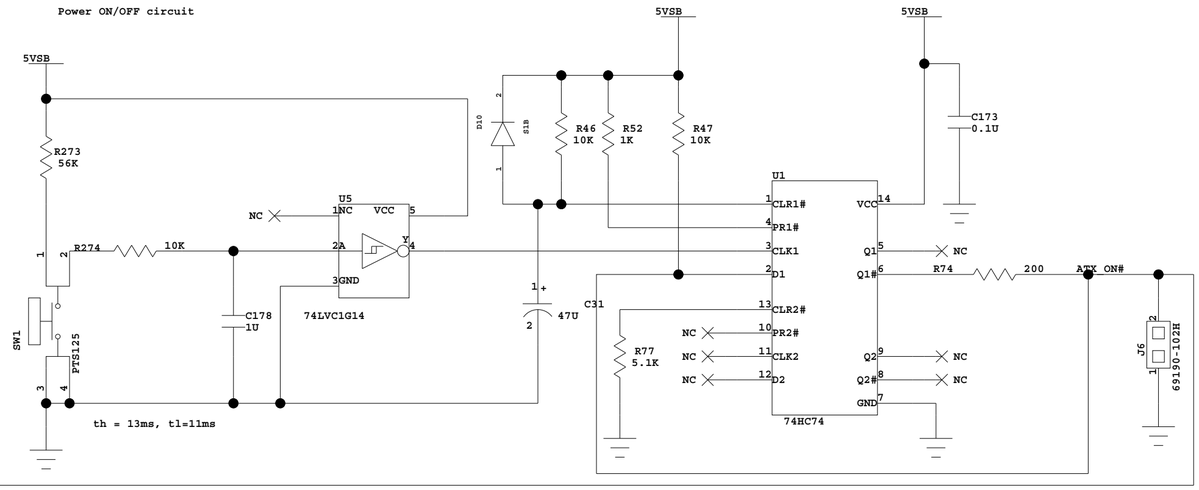
TITLE : CLOCK DISTRIBUTION			
SIZE: C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 7-16-2007_16:25	SHEET 10 OF 15		

POWER SOURCES

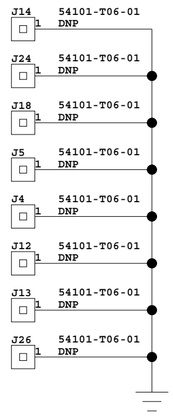
ATX

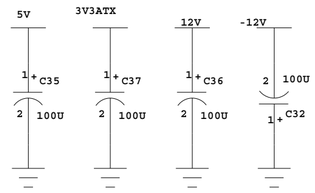


ATX SUPPLY TOGGLE

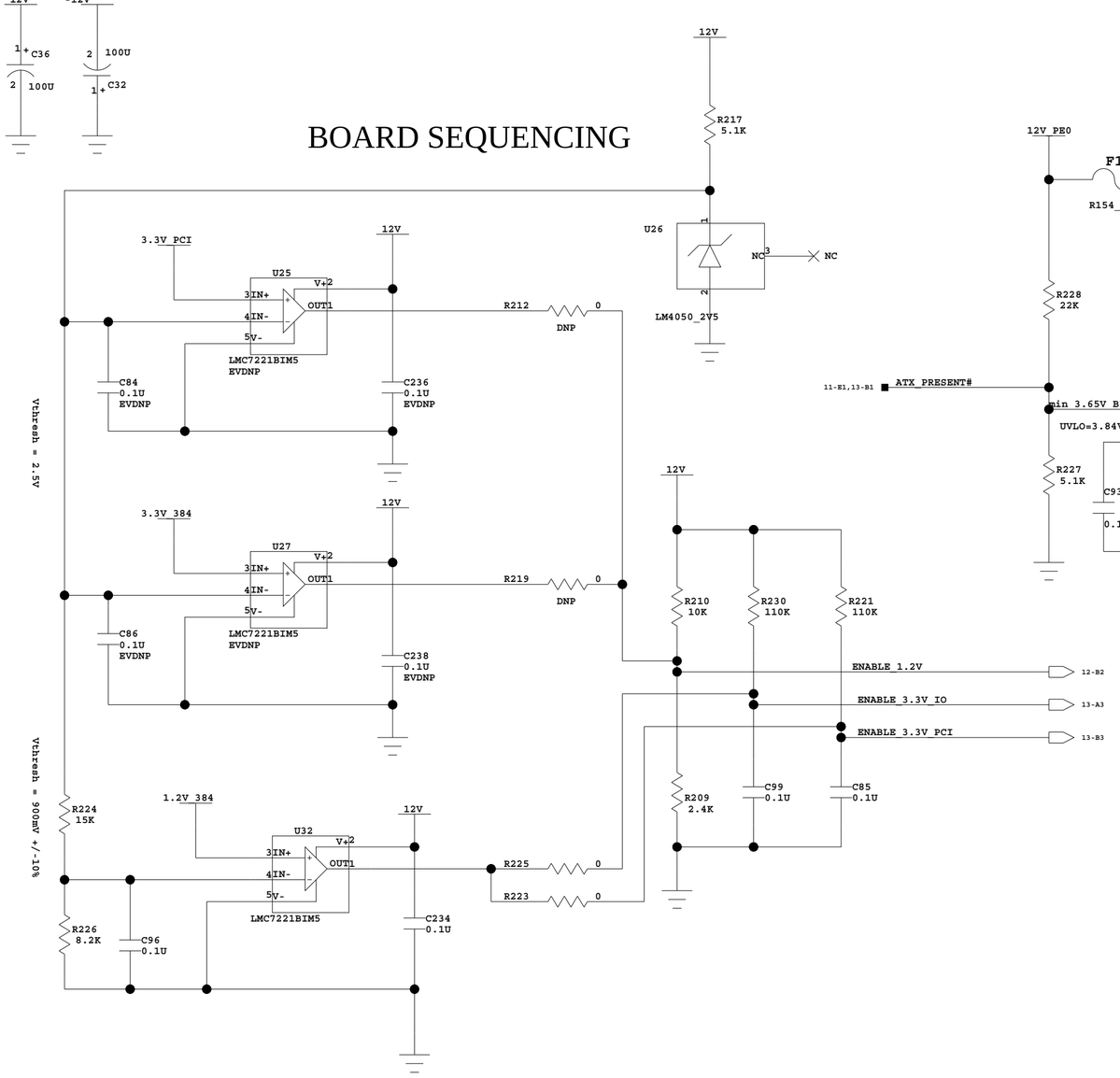


GND TESTPOINTS

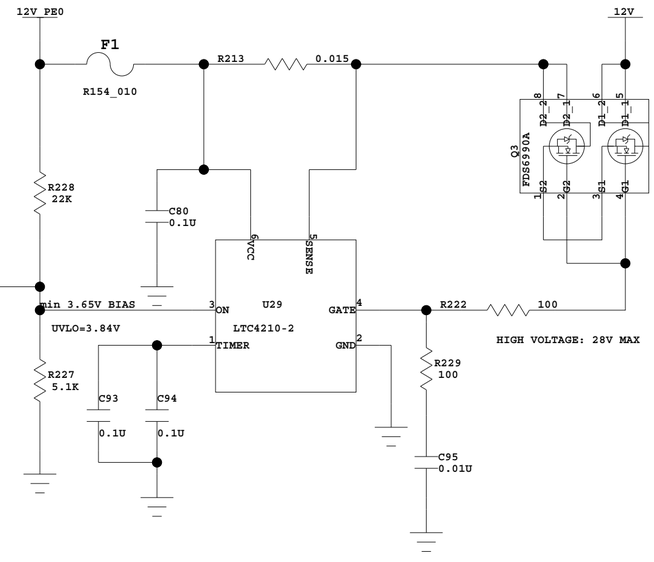




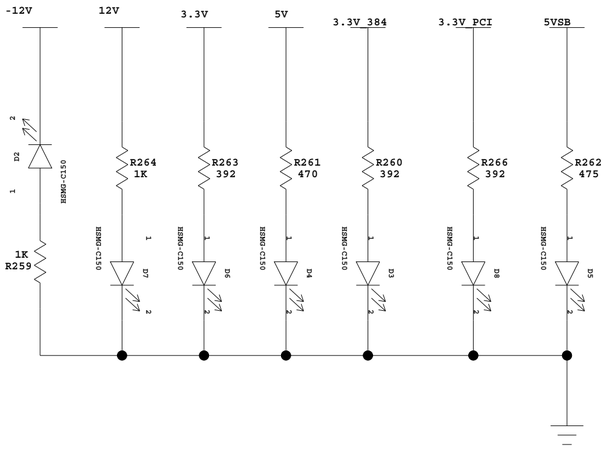
BOARD SEQUENCING



SYS SUPPLY SWITCH

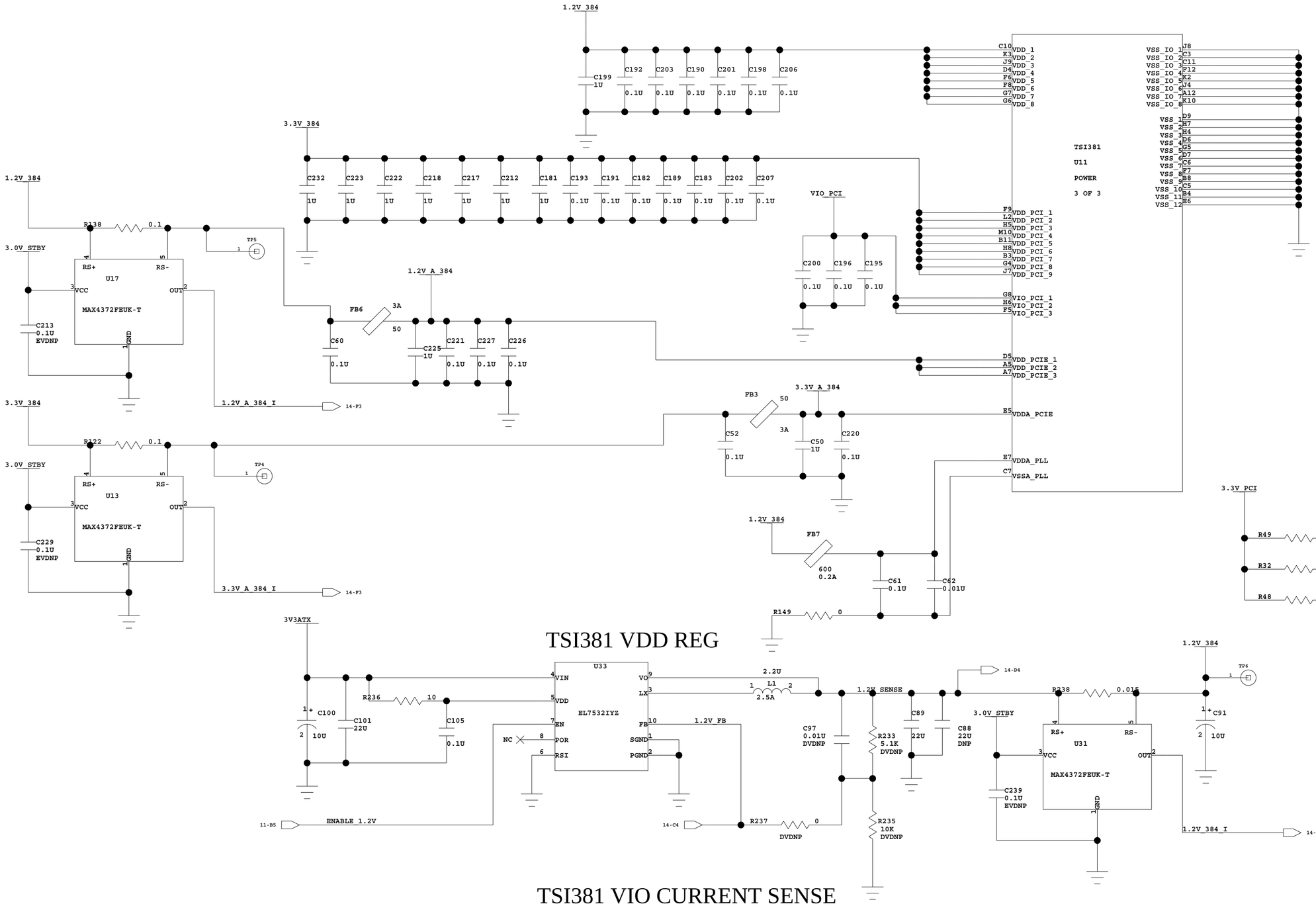


POWER STATUS



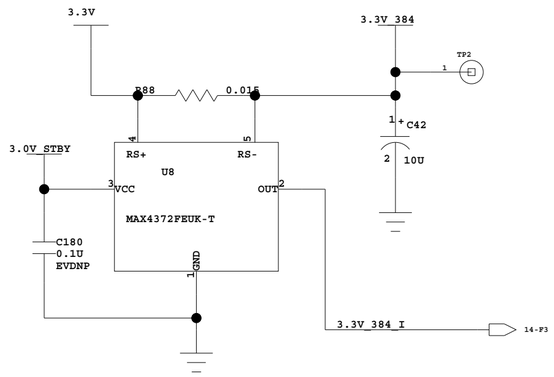
TITLE : POWER SOURCES			
SIZE C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 6-15-2007_14:56		SHEET 11 OF 15	

TSI381 POWER/REGULATORS



TSI381 VDD REG

TSI381 VIO CURRENT SENSE



TITLE :

Tsi381 POWER/REGULATORS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2000_SC001_03	1.0	

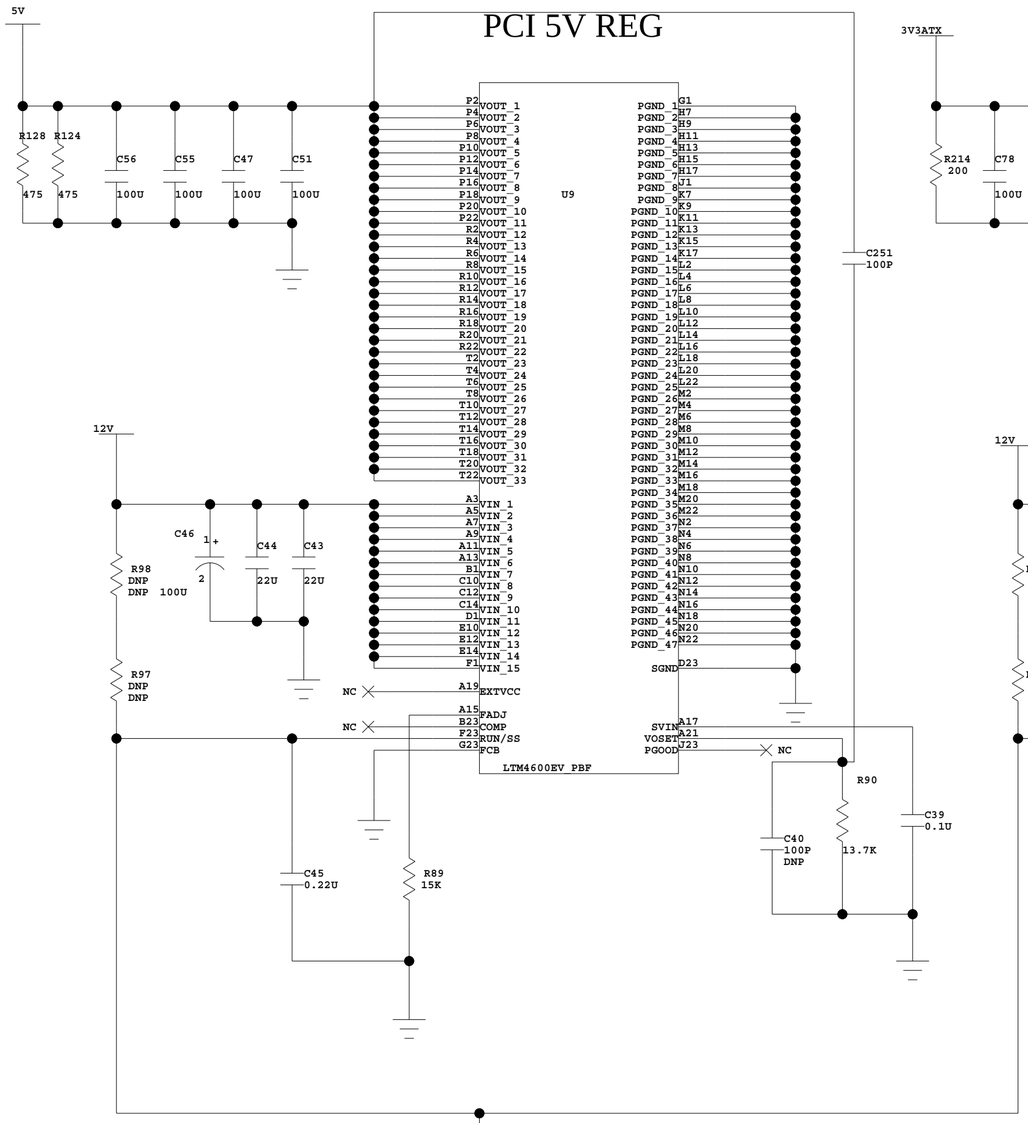
LAST MODIFIED DATE :

6-15-2007_14:56

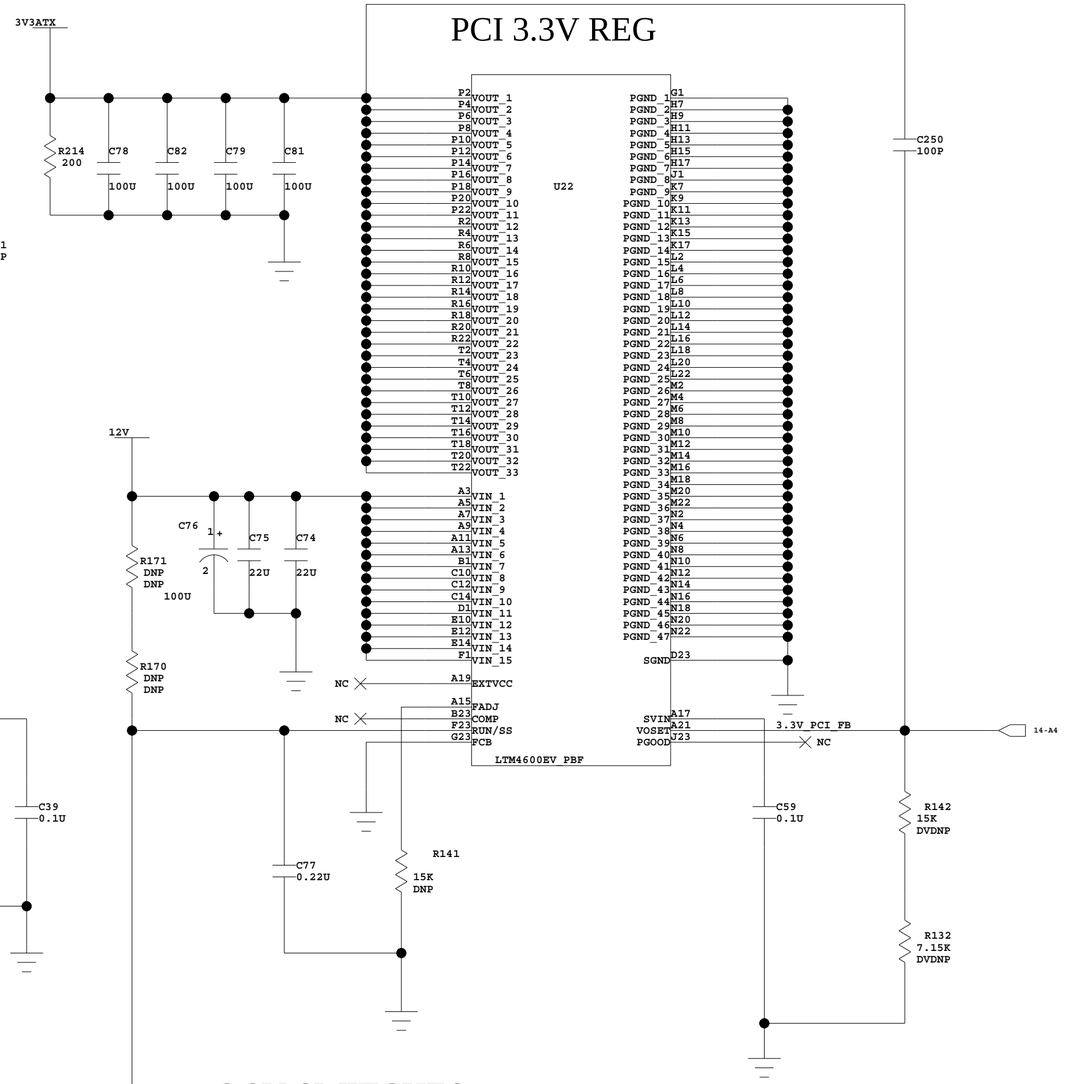
SHEET 12 OF 15

PCI POWER REGULATORS

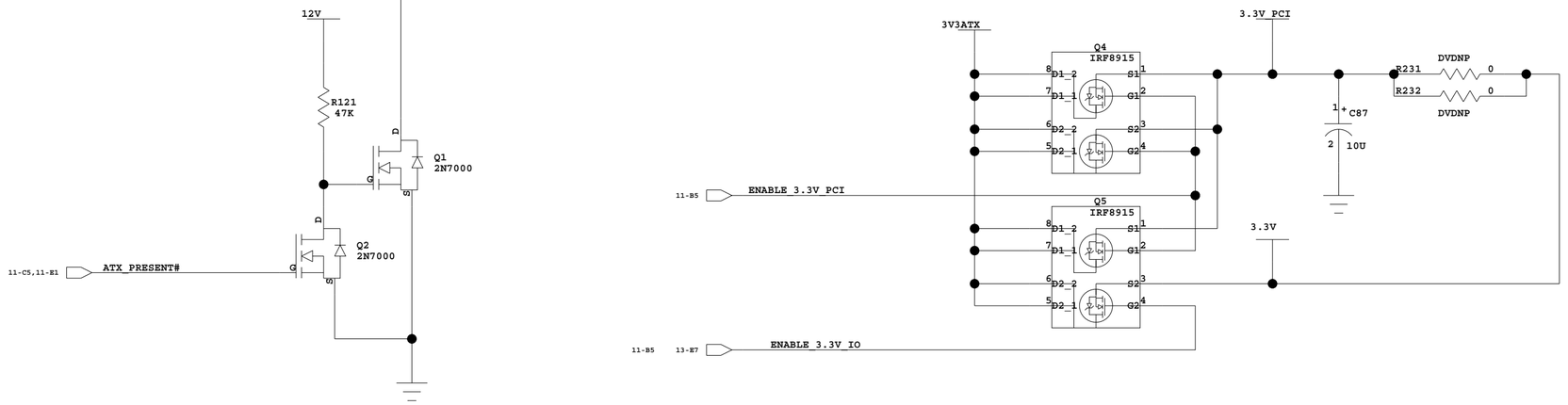
PCI 5V REG



PCI 3.3V REG



3.3V SWITCHES



TITLE :

PCI POWER REGULATORS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C	60E2000_SC001_03	1.0	

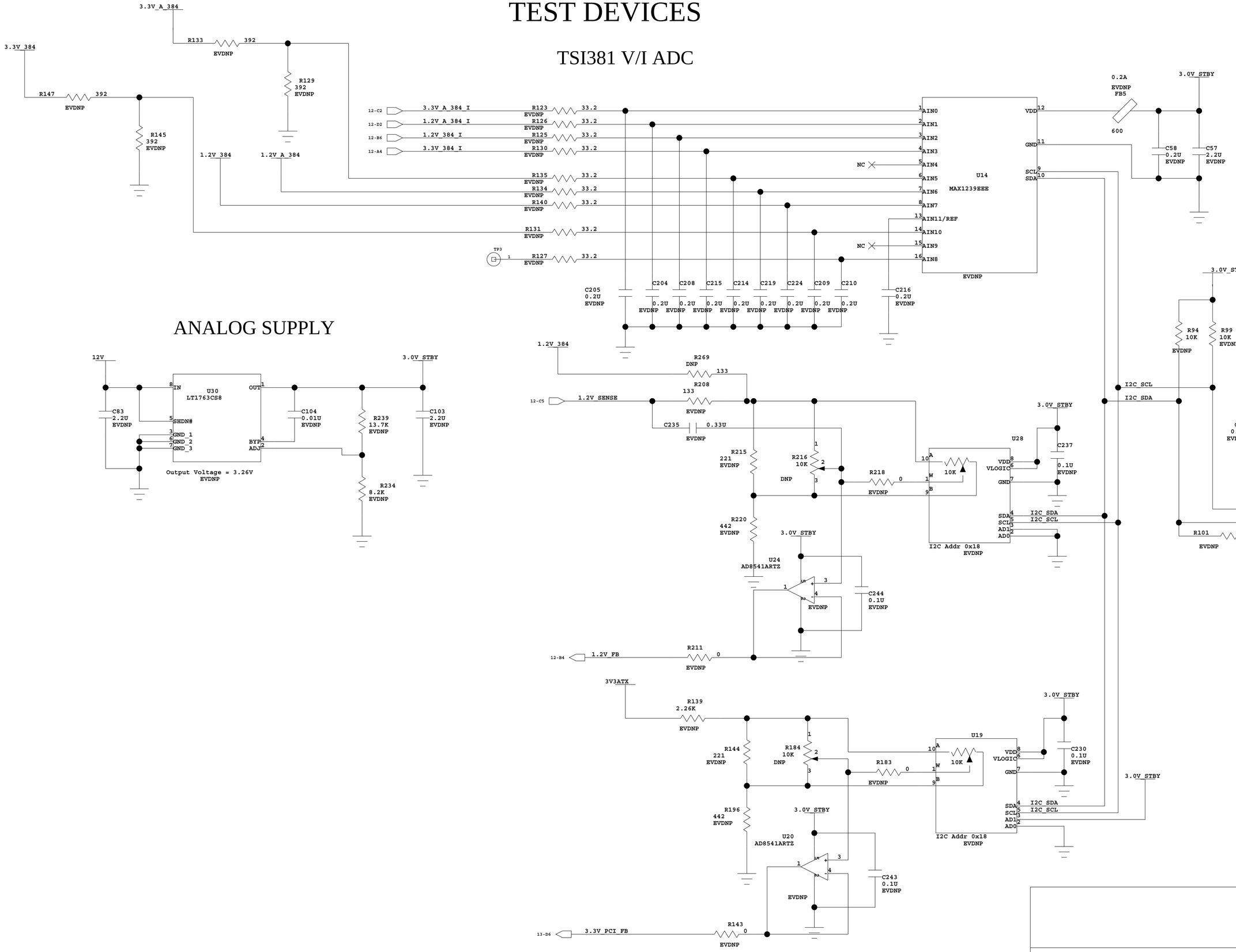
LAST MODIFIED DATE :

6-15-2007_14:48

SHEET 13 OF 15

TEST DEVICES

TSI381 V/I ADC

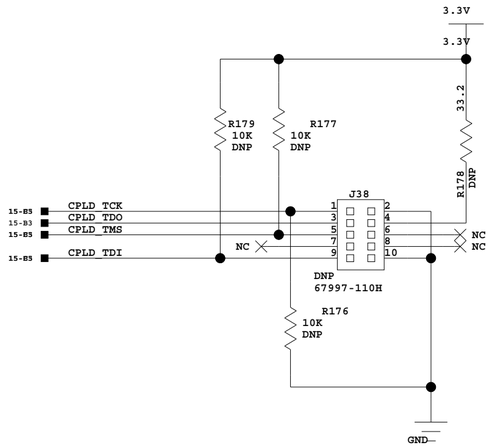


ANALOG SUPPLY

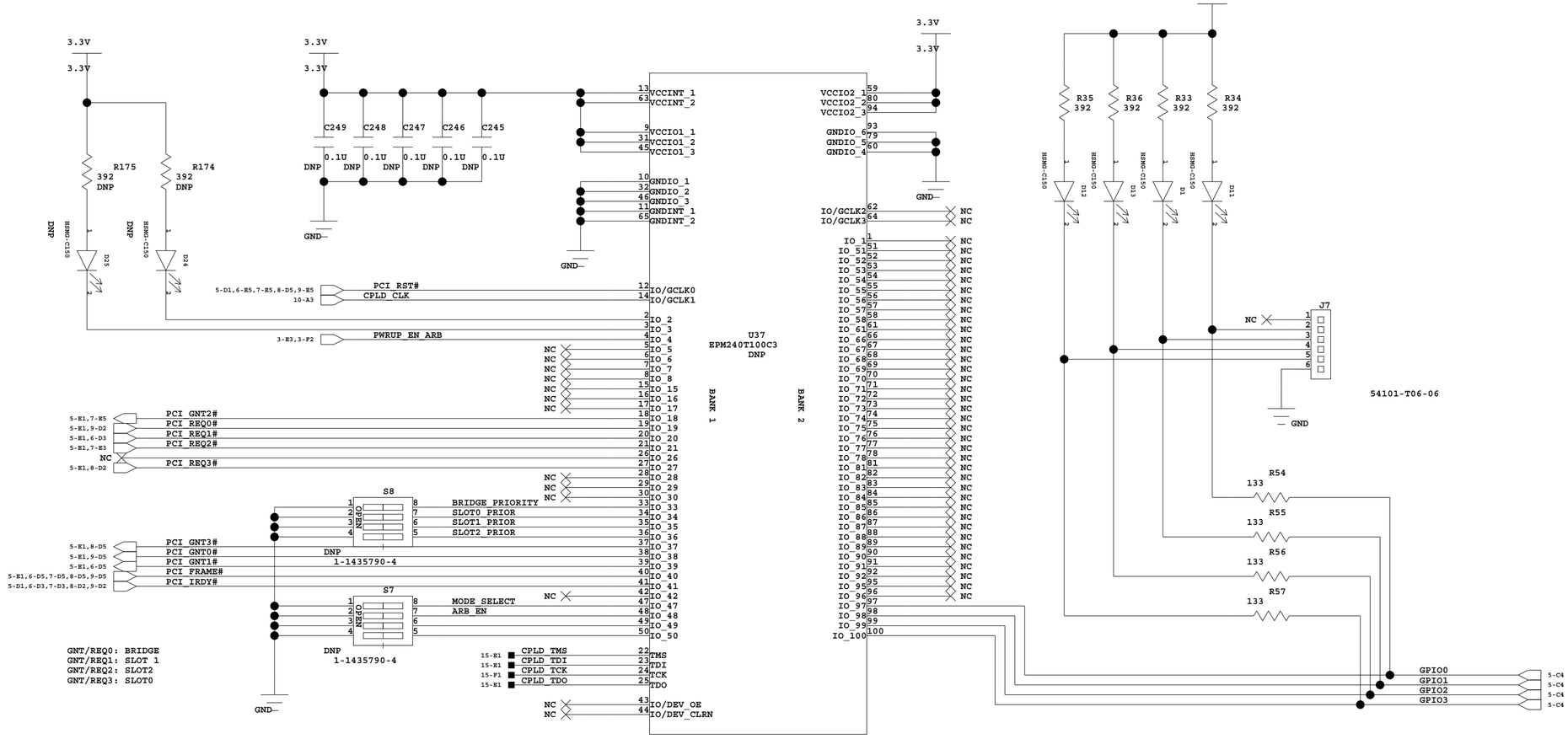
I2C

TITLE : TEST DEVICES			
SIZE C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 6-15-2007_14:56		SHEET 14 OF 15	

TEST DEVICES CONT'D



PCIARBITER/GPIO CONTROL



TITLE : TEST DEVICES CONT'D			
SIZE: C	DRAWING NUMBER : 60E2000_SC001_03	Version: 1.0	DESIGNER :
LAST MODIFIED DATE : 6-15-2007_16:00	SHEET 15 OF 15		