IDT®
Tsi310 Schematic Review Checklist

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1. Tsi310 Schematic Review Checklist

This checklist discusses the following schematic review topics for the Tsi310:

1.1 Overview

The *Schematic Review Checklist* offers design and termination recommendations for Tsi310 applications. This document is intended for designers that are in the process of completing their Tsi310 board schematics.

For this reason, it is beneficial to review the contents of the checklist before routing your Tsi310-based board.

For more information about Tsi310 hardware and software, please see the following:

- *Tsi310 User Manual*
- *Tsi310 Evaluation Board User Manual*

1.1.1 Signals

Table 1 describes the signal types found in the Tsi310.

Table 1: Signal Types

Signal Type	Definition
Input	Standard input only signal
Output	Standard output only signal
Tri-state Output	Standard tri-state output only signal
Open Drain	Open drain output — allows multiple devices to share as a wire-OR
Tri-state Bi-directional	Tri-state input/output signal
Bi-directional Open Drain	Open drain input/output — allows multiple devices to share as a wired-OR when used as output

Table 2 shows the I/O level conventions used for signal descriptions.

Table 2: Signal Conventions - I/O Level

Symbol	Type
3.3V TTL	3.3V I/O cell, TTL compatible
3.3V PCI/X	3.3V I/O cell, PCI/PCI-X compatible

Table 3 describes the driver impedance of the I/O cell.

Table 3: Signal Conventions - I/O Drive

Symbol	Type
50 ohm	Nominal impedance 50 ohms
PCI/X	For a 3.3V PCI/X I/O cell, the driver impedance for a point-to-point application is 40 ohms. For a 3.3V PCI/X I/O cell, the driver impedance for a multi-point application is 20 ohms. Driver impedance is controlled by the P_DRVR_MODE and S_DRVR_MODE pins as defined in the tables below.

1.1.2 Design Recommendation

It is advantageous to pull power up option signals high and have a jumper option to ground so the option can be changed after board production. Alternatively these can be controlled with a CPLD.

IDT experience has shown that designers who have implemented either jumpers or a CPLD into their designs have been able to significantly reduce the time it takes to bring their design up.

Pull-up is suggested to be 8.2K. Pulldown is suggested to be 1K.

1.1.3 Recommended Terminations

The purpose of this section is to identify any external circuitry required for PCI/X compliance when designing in the Tsi310. It is important to note that there are required Pull-up terminations for some of the control signals on the Primary PCI/X interface. These Pull-ups must exist somewhere in the complete system. The central resource on the primary bus segment is usually responsible to ensure proper termination of these signals.

In the following sections, when IDT recommends a central resource, it assumes that the Tsi310 is acting as a central resource on the secondary side of the bridge.

All of these recommendations are contained in the PCI 2.2 specification. If you have any questions about signal termination, it is recommended you review the appropriate sections of the latest PCI specification, available at www.pcisig.com.

1.1.4 Checkpoint

A Checkpoint section is included at the end of every signal. This is for the user to track the results of each signal recommendation in the Schematic Review.

- Pass — correct action taken
- Fail — no action or incorrect action taken
- Caution — problem with recommendation
- Help — user requires assistance or additional information

1.2 Primary PCI/X Signals

This section gives recommended terminations for Tsi310 signals that connect to the primary PCI/X bus.

This section includes two recommendations for each signal: the first is for the Tsi310, the second is for the Central Resource on the primary bus the Tsi310 is connecting to.

1.2.1 P_ACK64#

Primary PCI/X Acknowledge 64-bit Transfer: 3.3V PCI/X, Tri-state bi-directional

An active low signal. This signal is asserted by a target to indicate the target's willingness to participate in a 64-bit transaction. Driven by the target; sampled by the master. Rescinded by the target at the end of the transaction.

Recommended Termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.2 P_AD[63:0]

Primary PCI/X Multiplexed Address/Data Bus: 3.3V PCI/X, Tri-state bi-directional

64-bit multiplexed address and data bus, shared by other devices on the primary bus. During a transaction, this bus contains the physical address bus, attributes, or data, or it may be reserved.

Recommended Termination:

- None

(Central Resource on the Primary Bus must provide:

P_AD[63:32] upper 32-bits — Pull-up

P_AD[31:0] lower 32-bits — None)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.3 P_C/BE[7:0]#

Primary PCI/X Multiplexed Bus Command and Byte Enable Lines: 3.3V PCI/X, Tri-state bi-directional

During a transaction, these eight bits define the bus command, attributes, or byte enables for the transfer. These signals are shared with other agents on the primary bus and at times may be reserved.

Recommended Termination:

- None

(Central Resource on the Primary Bus must provide:

P_CBE[7:4]_ — Pull-up

P_CBE[3:0]_ — None)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.4 P_CLK

Primary PCI/X Clock Input: 3.3V PCI/X, Input

Received by the bridge and provides timing for all operations on the primary interface. P_CLK frequencies can range from 0 to 133 MHz.

Recommended termination:

- None

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.5 P_DEVSEL#

Primary PCI/X Device Select: 3.3V PCI/X, Tri-state bi-directional

Asserted by the target on the primary bus that decoded the address of the current transaction as being within one of its address ranges. P_DEVSEL# is monitored by the bridge when performing a primary bus transaction on behalf of the secondary bus master. P_DEVSEL# is driven by the bridge when a primary bus master is performing a transaction on the primary bus intended for a secondary bus slave or the bridge’s configuration registers.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.6 P_FRAME#

Primary Cycle Frame for PCI/X Bus: 3.3V PCI/X, Tri-state bi-directional

Defines the beginning and duration of each primary bus transaction and is controlled by the initiator of the operation. P_FRAME# is driven by the bridge when performing a primary bus transaction on behalf of a secondary bus master. P_FRAME# is monitored by the bridge when a primary bus master is performing a transaction on the primary bus.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.7 P_GNT#

Primary PCI/X Grant: 3.3V PCI/X, Input

Indicates that the bridge has been granted access to the primary bus.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.8 P_IDSEL

Primary PCI/X Initialization Device Select: 3.3V PCI/X, Input

Used as a chip select during Configuration Type0 read and write transactions on the primary bus.

Recommended termination:

- For the access to the Tsi310 registers the central resource should connect to only one unique AD line via a 2K series resistor. Choose from AD[31:16].

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.9 P_IRDY#

Primary PCI/X Initiator Ready: 3.3V PCI/X, Tri-state bi-directional

Indicates the ability of the initiator on the primary bus to complete the current data phase of the transaction. It is used in conjunction with P_TRDY#. P_IRDY# is driven by the bridge when performing a primary bus transaction on behalf of a secondary bus master. P_IRDY# is monitored by the bridge when a primary bus master is performing a transaction on the primary bus or through the bridge.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.10 P_LOCK#

Primary PCI/X Lock: 3.3V PCI/X, Input

Indicates that an atomic (unbroken) operation is required that may need multiple primary bus transactions to complete. P_LOCK# is monitored by the bridge when serving as the selected primary bus target in order to detect exclusive access.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.11 P_PAR

Primary PCI/X Parity: 3.3V PCI/X, Tri-state bi-directional

Parity protection bit for the lower half of the address/data and command/byte enable buses on the primary interface. It provides even parity across P_AD[31:0] and P_C/BE[3:0]#.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: None)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.12 P_PAR64

Primary PCI/X Parity Upper DWORD: 3.3V PCI/X, Tri-state bi-directional

Parity protection bit for the upper half of the address/data and command/byte enable buses on the primary interface. It provides even parity across P_AD[63:32] and P_CBE[7:4]#.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.13 P_PERR#

Primary PCI/X Parity Error: 3.3V PCI/X, Tri-state bi-directional

Used to report data parity errors on the primary interface. P_PERR# is monitored by the bridge when performing a primary bus write transaction on behalf of a secondary bus master or when serving as the selected slave for a primary bus read transaction. P_PERR# is driven by the bridge when performing a primary bus read transaction on behalf of a secondary bus master or when serving as the selected slave during a primary bus write transaction.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.14 P_REQ#

Primary PCI/X Bus Request: 3.3V PCI/X, Tri-state Output

Driven by the Tsi310 to request use of the primary bus.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.15 P_REQ64#

Primary PCI/X Request 64-bit Transfer: 3.3V PCI/X, Tri-state bi-directional

When asserted by the current master on the primary bus, this signal indicates a desire to transfer data using 64 bits.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.16 P_RST#

PCI/X Primary Bus Reset: 3.3V PCI/X, Input

This signal is used to initialize the bridge to a known state, drive the Secondary Bus Reset signal (S_RST#), and drive all primary bus and secondary bus output signals to their benign state.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.17 P_SERR#

Primary PCI/X System Error: 3.3V PCI/X, Tri-state Output

This signal is used to report address parity errors and other system errors where the results will be catastrophic. P_SERR# is driven by the bridge when detecting such errors on the primary bus or in the case of an error in which the initiator of the transaction cannot be otherwise notified. It is also driven as the result of S_SERR# being asserted on the secondary bus.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.18 P_STOP#

Primary PCI/X Stop: 3.3V PCI/X, Tri-state bi-directional

Indicates that the current target is requesting that the initiator stop the current transaction on the primary bus. P_STOP# is monitored by the bridge when performing a primary bus transaction on behalf of a secondary bus master. P_STOP# is driven by the bridge when addressed as a target and is asserted low to indicate target termination.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.2.19 P_TRDY#

Primary PCI/X Target Ready: 3.3V PCI/X, Tri-state bi-directional

Indicates the ability of the target on the primary bus to complete the current data phase of the transaction. It is used in conjunction with the P_IRDY# signal. P_TRDY# is monitored by the bridge when performing a primary bus transaction on behalf of a secondary bus master. P_TRDY# is driven by the bridge when a primary bus master is performing a transaction in which the bridge is the selected target.

Recommended termination:

- None

(Central Resource on the Primary Bus must provide: Pull-up)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3 Secondary PCI/X Signals

This section gives recommended terminations for Tsi310 signals that connect to the secondary PCI/X bus.

When a central resource is recommended, it means that the Tsi310 is acting as a central resource on the secondary side.

1.3.1 S_ACK64#

Secondary PCI/X Acknowledge 64-bit Transaction: 3.3V PCI/X, Tri-state bi-directional

Active low signal asserted by a target to indicate its ability to participate in a 64-bit transaction. Driven by the target; sampled by the master. Rescinded by the target at the end of the transaction.

Recommended Termination: (Central Resource)

- Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.2 S_AD[63:0]

Secondary PCI/X Address/Data Bus: 3.3V PCI/X, Tri-state bi-directional

These signals are the 64-bit multiplexed address and data bus, shared by other devices on the secondary bus. During a transaction, this bus contains the physical bus address, attributes, or data, or it may be reserved.

Recommended Termination: (Central Resource)

- S_AD[63:32] upper 32-bits — Pull-up
- S_AD[31:0] — None

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.3 S_C/BE[7:0]#

Secondary PCI/X Bus Command and Byte Enable Lines: 3.3V PCI/X, Tri-state bi-directional

During a transaction, these eight bits define the bus command, attributes, or byte enables for the transfer. These signals are shared with other agents on the secondary bus and at times may be reserved.

Recommended Termination: (Central Resource)

- S_CBE[7:4]_ — Pull-up
- S_CBE[3:0]_ — None

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.4 S_CLK

Secondary PCI/X Clock: 3.3V PCI/X, Input

Used to generate fixed timing parameters for the Secondary PCI/X Interface. S_CLK can operate from 25 to 133 MHz.

Recommended Termination: (Central Resource)

- None

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.5 S_DEVSEL#

Secondary PCI/X Device Select: 3.3V PCI/X, Tri-state bi-directional

Asserted by the target on the secondary bus that decoded the address of the current transaction as being within one of its address ranges. S_DEVSEL# is monitored by the bridge when performing a secondary bus transaction on behalf of a primary bus master. S_DEVSEL# is driven by the bridge when a secondary bus master is performing a transaction on the secondary bus intended for a primary bus slave.

Recommended Termination: (Central Resource)

- Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.6 S_FRAME#

Secondary Cycle Frame for PCI/X Bus: 3.3V PCI/X, Tri-state bi-directional

Defines the beginning and duration of each secondary bus transaction and is controlled by the initiator of the operation. S_FRAME# is driven by the bridge when performing a secondary bus transaction on behalf of a primary bus master. S_FRAME# is monitored by the bridge when a secondary bus master is performing a transaction on the secondary bus.

Recommended Termination: (Central Resource)

- Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.7 S_GNT1REQ#

Secondary PCI/X Grant 1: 3.3V PCI/X, Tri-state Output

This is a dual-purpose signal. When the bridge's internal arbiter is enabled, this signal is used as a grant output. It is activated by the bridge to grant the use of the secondary bus to the master who requested access to the bus with the S_REQ1GNT# signal. When the internal arbiter is disabled, this signal is used by the bridge as its request output signal.

Recommended Termination: (Central Resource)

- Tsi310 Arbiter used — Pull-up
- External Arbiter used — Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.8 S_GNT[6:2]#

Secondary PCI/X Grant 2-6: 3.3V PCI/X, Tri-state Output

Driven by the bridge's internal arbiter to grant usage of the secondary bus to the master that activated the corresponding request signal.

Recommended Termination: (Central Resource)

- Tsi310 Arbiter used — Pull-up
- External Arbiter used — Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.9 S_IDSEL

Secondary PCI/X Initialization Device Select: Input

Used as a chip select during configuration Type 0 read and write transactions on the secondary bus.

Recommended Termination: (Central Resource)

- Applications requiring access to the bridge configuration registers from the secondary bus should connect to only one unique AD line via 2K series resistor. Choose from AD [31:16]. Applications that do not require access to the bridge configuration registers from the secondary bus should place a Pulldown on this pin.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.10 S_IRDY#

Secondary PCI/X Initiator Ready: 3.3V PCI/X, Tri-state bi-directional

This signal indicates the ability of the initiator on the secondary bus to complete the current data phase of the transaction. It is used in conjunction with S_TRDY#. S_IRDY# is driven by the bridge when performing a secondary bus transaction on behalf of a primary bus master. S_IRDY# is monitored by the bridge when a secondary bus master is performing a transaction on the secondary bus through the bridge.

Recommended Termination: (Central Resource)

- Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.11 S_LOCK#

Secondary PCI/X Lock: 3.3V PCI/X, Tri-state bi-directional

Indicates that an atomic (unbroken) operation is required that may need multiple secondary bus transactions to complete. The bridge drives S_LOCK# only to propagate an exclusive access from the primary bus to the secondary bus and monitors S_LOCK# as part of that protocol. When acting as a target on the secondary interface, the bridge ignores S_LOCK#.

Recommended Termination: (Central Resource)

- Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.12 S_PAR

Secondary PCI/X Parity: 3.3V PCI/X, Tri-state bi-directional

Parity protection bit for the lower half of the address/data and command/byte enable buses on the secondary interface. It provides even parity across S_AD[31:0] and S_C/BE[3:0]#.

Recommended Termination: (Central Resource)

- None

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.13 S_PAR64

Secondary PCI/X Parity Upper DWORD: 3.3V PCI/X, Tri-state bi-directional

Parity protection bit for the upper half of the address/data and command/byte enable buses on the secondary interface. It provides even parity across S_AD[63:32] and S_CBE[7:4]#.

Recommended Termination: (Central Resource)

- Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.14 S_PERR#

Secondary PCI/X Parity Error: 3.3V PCI/X, Tri-state bi-directional

Used to report data parity errors on the secondary interface. S_PERR# is monitored by the bridge when performing a secondary bus write transaction on behalf of a primary bus master or when serving as the selected slave for a secondary bus read transaction. S_PERR# is driven by the bridge when performing a secondary bus read transaction on behalf of a primary bus master or when serving as the selected slave during a secondary bus write transaction.

Recommended Termination: (Central Resource)

- Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.15 S_REQ1GNT#

Secondary PCI/X Bus Request 1: 3.3V PCI/X, Input

This is a dual-purpose signal: When the bridge's internal arbiter is enabled, this signal is used as a request input, to be activated by a secondary bus master requesting the use of the secondary bus. When the bridge's internal arbiter is disabled, this signal is used by the bridge as its grant input signal.

Recommended Termination: (Central Resource)

- Tsi310 Arbiter used: Pull-up
- External Arbiter used: Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.16 S_REQ[6:2]#

Secondary PCI/X Bus Request 2-6: 3.3V PCI/X, Input

Activated by the secondary bus masters to request the use of the secondary bus.

Recommended Termination: (Central Resource)

- Tsi310 Arbiter used: Pull-up
- External Arbiter used: Pull-up

When pulling up all unused S_REQ[6:2]# lines, save space by using a single resistor to pull up unused lines.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.17 S_REQ64#

Secondary PCI/X Request 64-bit Transfer: 3.3V PCI/X, Tri-state bi-directional

This signal, when asserted by the current master on the secondary bus, indicates a desire to transfer data using 64 bits.

Recommended Termination: (Central Resource)

- Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.18 S_RST#

Secondary PCI/X Secondary Bus Reset: 3.3V PCI/X, Output

S_RST#, driven by the bridge, is the secondary bus reset signal. Asserted when P_RST# is active or when the secondary bus reset bit in the bridge control register is set.

Recommended Termination: (Central Resource)

- None

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.19 S_SERR#

Secondary PCI/X System Error: 3.3V PCI/X, Input

Used to report address parity errors and other system errors where the results will be catastrophic. S_SERR# is monitored by the bridge to detect these errors on the secondary bus. When S_SERR# is asserted, it results in P_SERR# being asserted on the primary bus by the bridge.

Recommended Termination: (Central Resource)

- Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.20 S_STOP#

Secondary PCI/X Stop: 3.3V PCI/X, Tri-state bi-directional

Indicates that the current target is requesting that the initiator stop the current transaction on the secondary bus. S_STOP# is monitored by the bridge when performing a secondary bus transaction on behalf of a primary bus master. S_STOP# is driven by the bridge when addressed as a target and is asserted low to indicate target termination.

Recommended Termination: (Central Resource)

- Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.3.21 S_TRDY#

Secondary PCI/X Target Ready: 3.3V PCI/X, Tri-state bi-directional

Indicates the ability of the target on the secondary bus to complete the current data phase of the transaction. It is used in conjunction with the S_IRDY# signal. S_TRDY# is monitored by the bridge when performing a secondary bus transaction on behalf of a primary bus master. S_TRDY# is driven by the bridge when a secondary bus master is performing a transaction in which the bridge is the selected target.

Recommended Termination: (Central Resource)

- Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.4 PLL Signals

This section gives recommended terminations for Tsi310 PLL signals.

1.4.1 XCLK_OUT

Primary PLL Test Input: 3.3V TTL, Output

This signal may be used to monitor the output of the phase-locked loop circuits for the primary and secondary interfaces. During normal system operation, this output is in a high-impedance state and should be pulled down on the board.

Recommended Termination:

- Pulldown

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5 Power Supply Signals

This section gives recommended terminations for the Tsi310 power supply signals.

1.5.1 P_VDDA

Supply

Quiet 2.5V power supply connection to the PLL for the primary clock domain.

Recommended Termination:

- 2.5V plus filtering

A filtering circuit may be required to ensure a quiet supply at this pin. Please see the *Tsi310 User Manual* section 6.6.1, for a suggested filtering circuit.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.2 GND

Supply

Ground

Recommended Termination:

- Ground

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.3 S_VDDA

Supply

Quiet 2.5V power supply connection to the PLL for the secondary clock domain.

Recommended Termination:

- 2.5V plus filtering

A filtering circuit may be required to ensure a quiet supply at this pin. Please see the *Tsi310 User Manual* section 6.6.1, for a suggested filtering circuit.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.4 VDD

Supply

2.5V power supply connections for the internal logic.

Recommended Termination:

- 2.5V plus decoupling

See the schematic section on page 11 of the *Tsi310 Evaluation Board User Manual* for suggested decoupling placement.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.5.5 VDD2

Supply

3.3V power supply connections for the I/O circuits.

Recommended Termination:

- 3.3V plus decoupling

See the schematic section on page 11 of the *Tsi310 Evaluation Board User Manual* for suggested decoupling placement.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6 Strapping Pins and Other Signals

This section gives recommended terminations for Tsi310 strapping pins and other signals.

1.6.1 64_BIT_DEVICE#

Physical bus width of the PCI-X device: Input

Used only when the Tsi310 is employed as the bus interface on PCI-X. The PCI-X specification requires that such devices indicate the physical width of their bus in bit 16 of the PCI-X bridge status register. Bit 16 of the PCI-X bridge status register is set directly from the inverse of the 64_BIT_DEVICE# pin. This information is used solely by the configuration software; operation of the Tsi310 is unaffected.

Recommended Termination:

- Pulldown, bit 16 of the PCI-X bridge status register is set to 1, indicating a 64 bit bus.
- Pull-up, bit 16 of the PCI-X bridge status register is set to 0, indicating a 32 bit bus.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.2 BAR_EN

Base Address Register Enable: input

Used to enable the base address register at reset or power up. The 64 bit register located at offsets x‘10‘ and x‘14‘ is used to claim a 1 MB memory region when enabled. The register returns all zeros to read accesses and the associated memory region is not claimed when disabled.

Recommended Termination:

- Pulldown, BAR disabled, register reads return 0’s, no memory region claimed.
- Pull-up, BAR enabled, bits [63:20] can be written by software to claim a 1MB memory region.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.3 IDSEL_REROUTE_EN

IDSEL Reroute Enable: Input

Used to enable the IDSEL reroute function at reset or power up. The reset value of the secondary bus private device mask register is modified according to the tie value of the IDSEL_REROUTE_EN pin. Note that configuration software can subsequently modify the secondary bus private device mask register, regardless of how the IDSEL_REROUTE_EN pin is tied. Please see the *Tsi310 User Manual* for additional information around the functionality of this signal.

Recommended Termination:

- Pulldown, reset value of the secondary bus private device mask register is x‘00000000‘.
- Pull-up, reset value of the secondary bus private device mask register is x‘22F20000‘.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.4 OPAQUE_EN

Opaque Region Enable: Input

Used to enable the opaque memory region at reset or power up. The reset value of bit 0 of the opaque memory enable register is modified according to the tie value of the OPAQUE_EN pin. The configuration software can subsequently modify bit 0 of the opaque memory enable register, regardless of how the OPAQUE_EN pin is tied.

Recommended Termination:

- Pulldown, reset value of bit 0 of the opaque memory enable register is 0.
- Pull-up, reset value of bit 0 of the opaque memory enable register is 1.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.5 P_CFG_BUSY

Primary Configuration Busy: Input

Controls the reset and power up value of bit 2 of the miscellaneous control register. Used to sequence initialization with regard to primary and secondary buses for applications that require access to the bridge configuration registers from the secondary bus. The intended use of this pin is when pulled high, the configuration commands received on the primary bus are retried until such time as bit 2 of the miscellaneous control register is set to 0 by a configuration write initiated from the secondary bus.

Recommended Termination:

- Pulldown, due to Tsi310 Errata #1.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.6 P_DRVR_MODE

Primary Driver mode control: Input

Used to alter the output impedance of the primary bus PCI/PCI-X drivers, to account for how many drops are on the bus. This line should be pulled through a resistor to a high or a low as needed. Please see Table 4 below.

Recommended Termination:

- Pulldown, Tsi310 uses the default impedance value.
- Pull-up, Tsi310 selects the alternative impedance value.

Table 4 describes the driver impedance selection for the primary PCI/X signals.

Table 4: Primary Bus Driver Impedance Selection

Primary Bus Mode	Default Driver Mode (P_DRVR_MODE = 0)	Driver Mode if (P_DRVR_MODE = 1)
Conventional PCI	Multi-point (20 ohm)	Point-to-point (40 ohm)
PCI-X 66	Multi-point (20 ohm)	Point-to-point (40 ohm)
PCI-X 100	Multi-point (20 ohm)	Point-to-point (40 ohm)
PCI-X 133	Point-to-point (40 ohm)	Multi-point (20 ohm)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.7 S_CLK_STABLE

Secondary Clock Input Stable: Input

Indicates when the S_CLK input to the bridge is stable. It is used to determine when the S_RST# signal may be de-asserted.

Recommended Termination:

See the *Tsi310 User Manual* section 4.4 for source suggestions for this input.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.8 S_DRVR_MODE

Secondary Driver mode control: Input

Used to alter the output impedance of the secondary bus PCI/PCI-X drivers, to account for how many drops are on the bus. This line should be pulled through a resistor to a high or a low as needed. Please see Table 5 below.

Recommended Termination:

- Pulldown, Tsi310 uses the default impedance value.
- Pull-up, Tsi310 selects the alternative impedance value.

Table 5 describes the driver impedance selection for the secondary PCI/X signals.

Table 5: Secondary Bus Driver Impedance Selection

Secondary Bus Mode	Default Driver Mode (S_DRVR_MODE = 0)	Driver Mode if (S_DRVR_MODE = 1)
Conventional PCI	Multi-point (20 ohm)	Point-to-point (40 ohm)
PCI-X 66	Multi-point (20 ohm)	Point-to-point (40 ohm)
PCI-X 100	Multi-point (20 ohm)	Point-to-point (40 ohm)
PCI-X 133	Point-to-point (40 ohm)	Multi-point (20 ohm)

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.9 S_INT_ARB_EN#

Secondary Internal Arbiter Enable: Input

Used to choose between the internal arbiter and the external arbiter for the secondary bus.

Recommended Termination:

- Pulldown, uses the Tsi310 internal arbiter.
- Pull-up, disables the Tsi310 internal arbiter, use an external arbiter.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.10 S_PCIXCAP

Secondary Bus PCI-X Capable: Input

Used in conjunction with the S_PCIXCAP_PU and S_SEL100 signals to determine the operating frequency and mode of the secondary interface.

Recommended Termination:

See the *Tsi310 User Manual* section 4.3.2 for circuit suggestions for this input.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.11 S_PCIXCAP_PU

Secondary Bus S_PCIXCAP Pull-up Driver: Output

Part of a programmable Pull-up circuit used to detect the three possible states of the S_PCIXCAP input signal. A 1K ohm resistor must be placed on the board and wired between this signal and S_PCIXCAP.

Recommended Termination:

See the *Tsi310 User Manual* section 4.3.2 for circuit suggestions for this signal.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.6.12 S_SEL100

Secondary Bus 100MHz Indicator: Input

Used to choose between 100MHz and 133MHz maximum operating frequency on the secondary interface when in PCI-X mode. It has no meaning in the PCI mode, but should be tied to a stable value.

Recommended Termination:

- Pulldown, 133MHz operation.
- Pull-up, 100MHz operation.

See the *Tsi310 User Manual* section 4.3.2 for circuit suggestions for this signal.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.7 Test Signals

This section gives recommended terminations for Tsi310 Test signals. Please see section 7.3 of the *Tsi310 User Manual* for additional JTAG design considerations.

As a precaution. The board designer must do their own analysis of the devices on the bus before implementing JTAG. Some devices may have signals with pull-ups where Tsi310 has pulldowns or vise-versa. This could cause signals to be pulled to an indeterminate logic level.

1.7.1 JTG_TCK

JTAG Test Clock: 3.3V TTL, Input

Used to clock state information and data into and out of the bridge during operation of the IEEE 1149.1 test access port (TAP).

Recommended Termination:

- JTAG Used — None, this signal has a 14K ohm internal Pull-up on it.
- JTAG Unused — Pull-up or Pulldown

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.7.2 JTG_TDI

JTAG Test Data Input: 3.3V TTL, Input

Used (in conjunction with TCK) to shift data and instructions into the Test Access Port (TAP) in a serial bit stream.

Recommended Termination:

- None, this signal has a 14K ohm internal Pull-up on it.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.7.3 JTG_TDO

JTAG Test Data Output: 3.3V TTL, Tri-state output

Used (in conjunction with TCK) to shift data and instructions into the Test Access Port (TAP) in a serial bit stream.

Recommended Termination:

- None

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.7.4 JTG_TMS

JTAG Test Mode Select: 3.3V TTL, Input

Used to control the state of the Test Access Port Controller within the bridge.

Recommended Termination:

- None, this signal has an internal 14K ohm pull-up on it.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.7.5 JTG_TRST#

JTAG Test Reset: 3.3V TTL, Input

Provides an asynchronous initialization of the TAP controller within the bridge. If this pin is not used, pull low.

Recommended termination:

- If boundary scan is not implemented — Pulldown independently bussed
- If boundary scan is implemented — None, this signal has an internal 14K ohm pull-up on it.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.7.6 T_DI1#

Driver Inhibit 1: 3.3V TTL, Input

Used to tri-state the outputs of non-test drivers during manufacturing test. It must be tied high for normal system operation.

Recommended Termination:

- This signal has an internal pull-up on it, but IDT recommends a Pull-up on the board.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.7.7 T_DI2#

Driver Inhibit 2: 3.3V TTL, Input

Used to tri-state the outputs of non-test drivers during manufacturing test. It must be tied high for normal system operation.

Recommended Termination:

- This signal has an internal Pull-up on it, but IDT recommends a Pull-up on the board.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.7.8 T_MODECTL

Driver Mode Control: 3.3V TTL, Input

Used to control the PCI/PCI-X driver impedance during manufacturing test. It should be tied low for normal system operation.

Recommended Termination:

- Pulldown

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.7.9 T_RI#

Receiver Inhibit: 3.3V TTL, Input

Used to gate all receivers during manufacturing test. It must be tied high for normal system operation.

Recommended Termination:

- Pull-up

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.7.10 TEST_CEO

Test Mode Enable: 3.3V TTL, Input

Used to enable scan testing of the bridge device during manufacturing test. It must be tied low for normal system operation.

Recommended Termination:

- This signal has an internal Pulldown on it, but IDT recommends a Pulldown on the board.

Checkpoint:

Pass_____ Fail_____ Caution_____ Help_____

1.8 Interrupts

Interrupt Signal Routing Recommendation:

There are multiple standards for interrupt routing. The recommendation for interrupt routing depends upon the standard (PICMG standard, etc.). It may also be a proprietary routing.

It is recommended that you discuss interrupt routing with your BIOS resource people to determine which method is applicable to the design.

1.9 Recommended Reading

1. *PCI-X/PCI Hardware and Software Architecture and Design, 5th edition*
   (Ed Solari, George Willse) ISBN 0-92932-63-9
2. *PCI-X System Architecture*
   (Tom Shanley, Don Anderson) Mindshare Inc. ISBN 0-201-72682-3
3. *PCI System Architecture, 4th edition*
   (Tom Shanley, Don Anderson) Mindshare Inc. ISBN 0-201-30974-2
4. *PCI Local Bus Specification Rev. 2.2*
   (Available from www.pcisig.com)
5. *PCI-X Specification*
   (Available from www.pcisig.com)
6. *PCI Bridge Specification*
   (Available from www.picmg.com)

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