Serial RapidIO Gen2 Development Platform (SRDP2)

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TITLE : TITLE SHEET			
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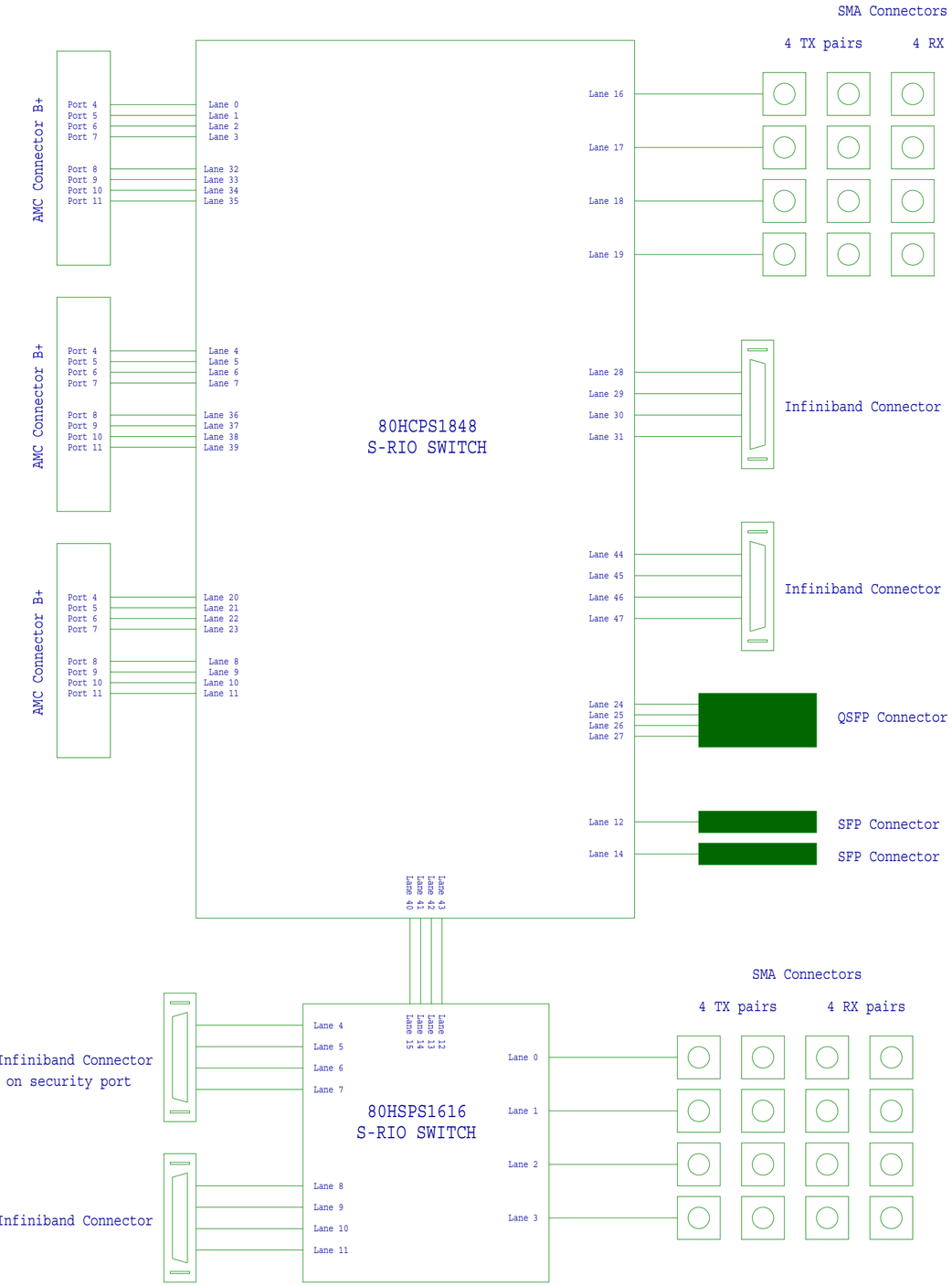
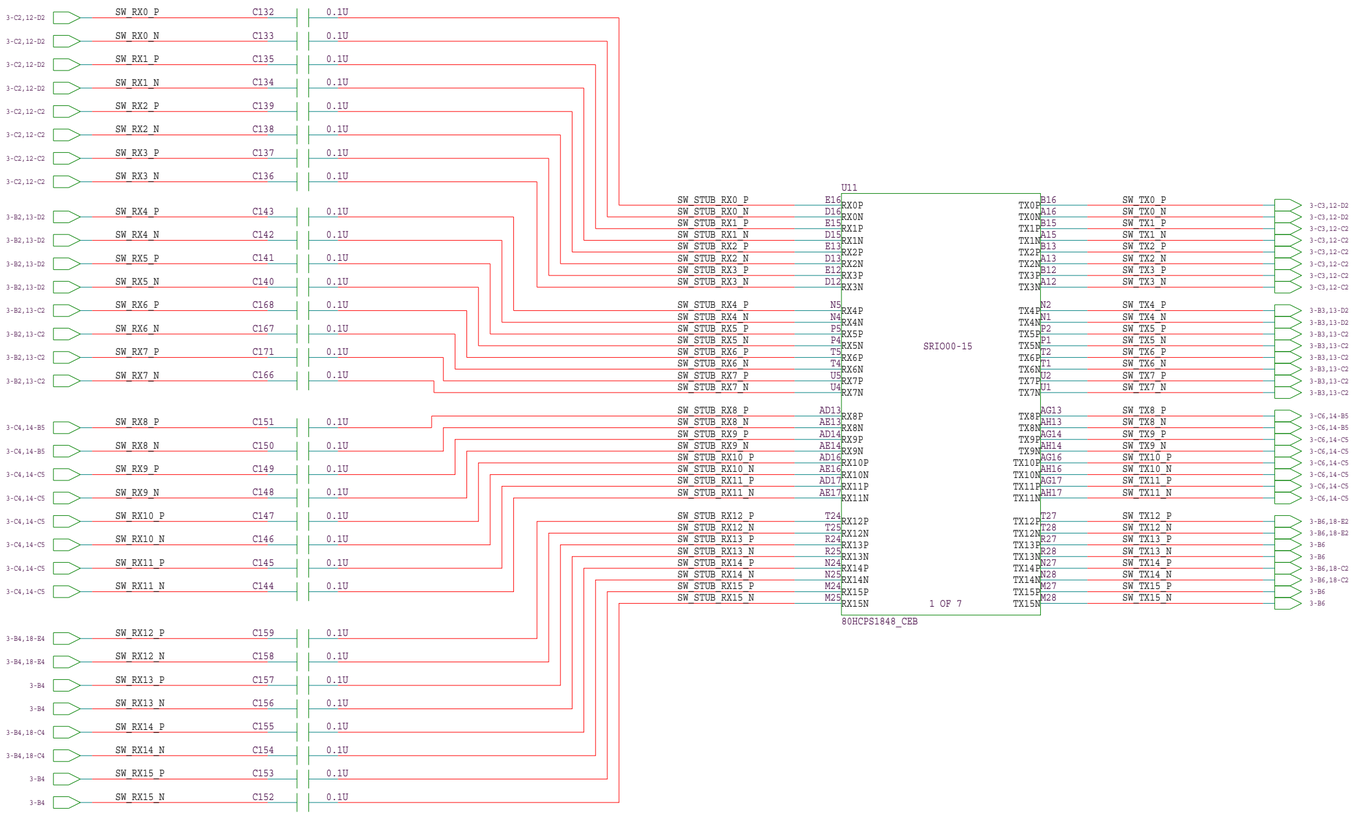
Block Diagram

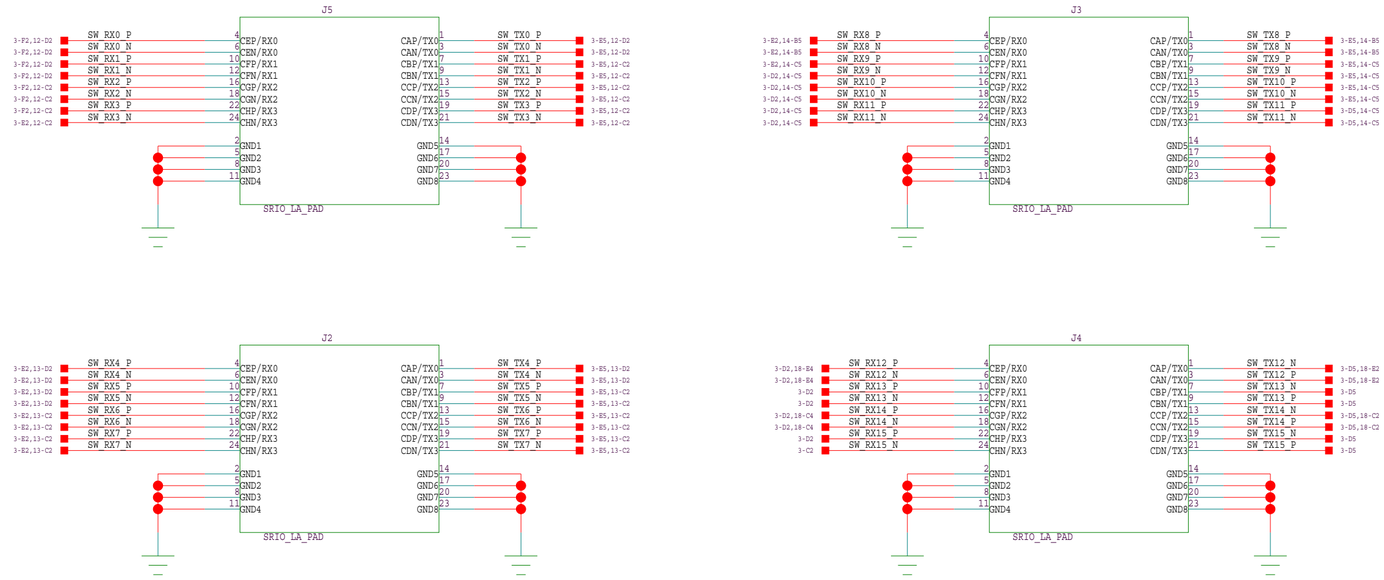


TITLE : BLOCK DIAGRAM			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:46		SHEET 2 OF 25	

80HCPS1848 Lanes 0-15

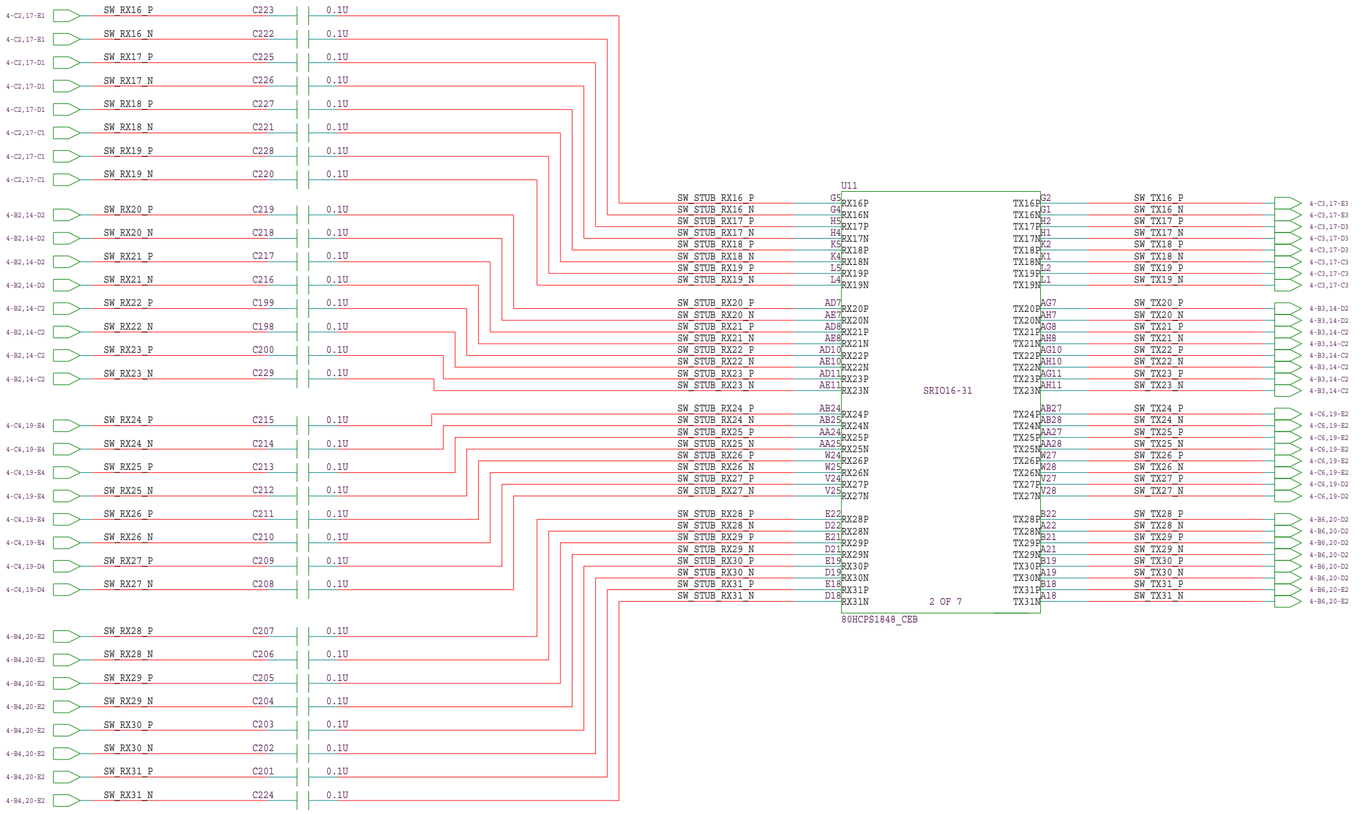


L.A. PADS



TITLE : 80HCPS1848 LANES 0-15			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:46	SHEET 3 OF 25		

80HCPS1848 Lanes 16-31



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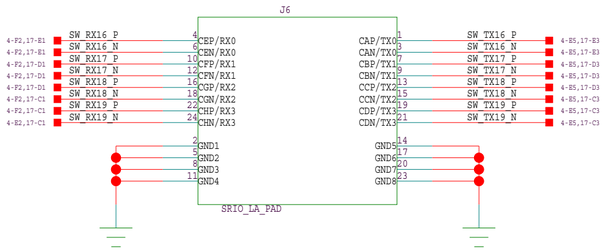

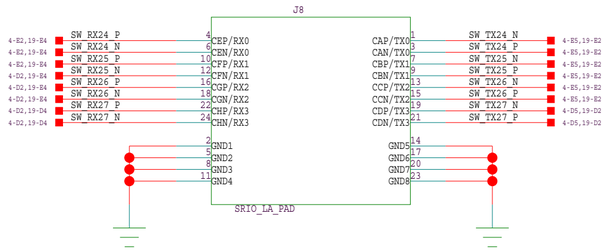

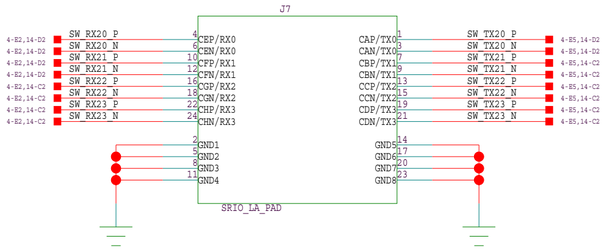

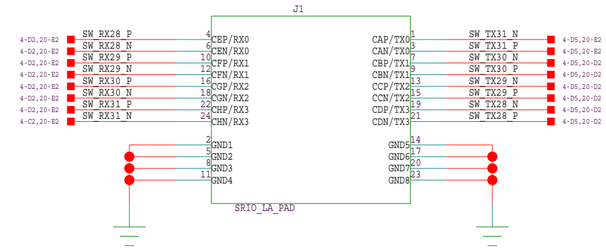

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TITLE : 80HCPS1848 LANES 16-31

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			

LAST MODIFIED DATE : 7-22-2010_16:46

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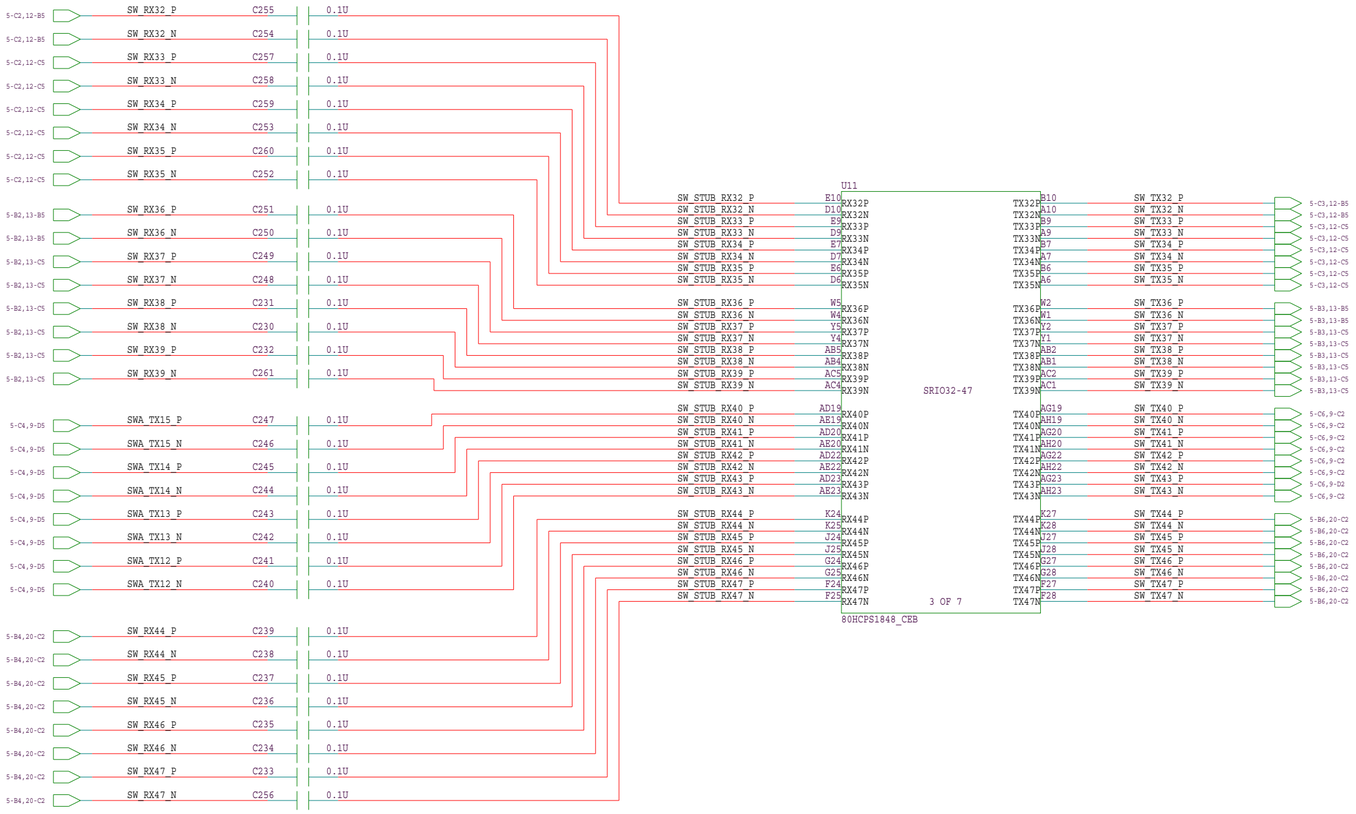
80HCPS1848 Lanes 32-47



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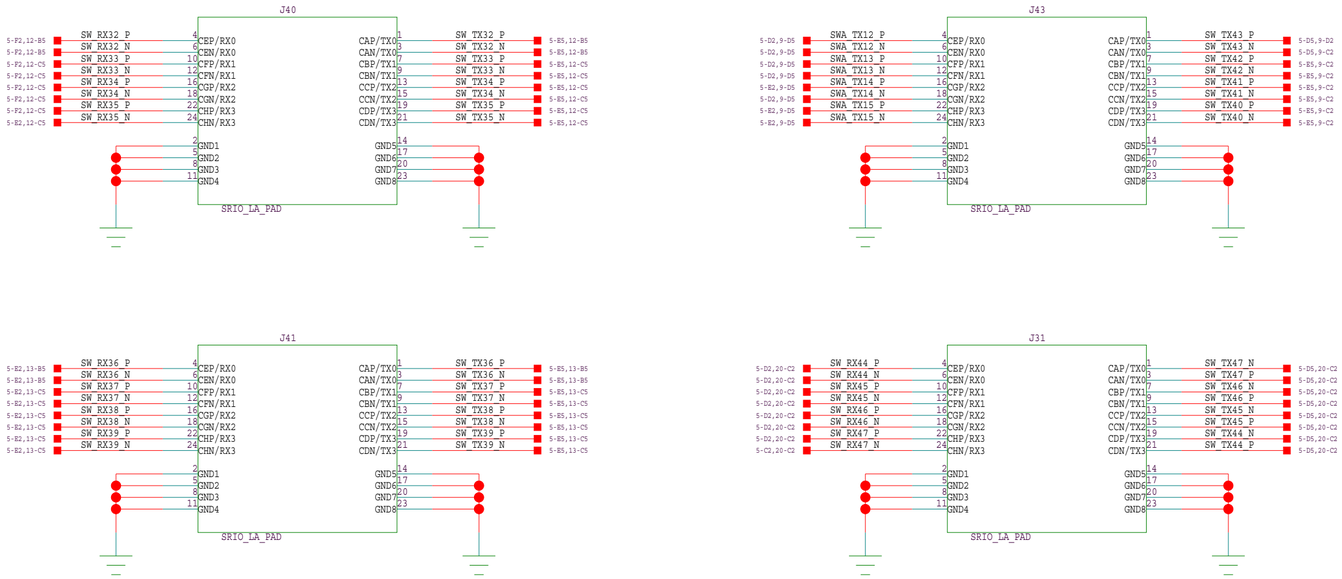

TITLE : 80HCPS1848 LANES 32-47			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
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80HCPS1848 Config

I2C address 0x60

3.3V

R41 10K, R38 10K, R40 10K, R18 10K, R30 10K, R35 10K, R37 10K, R36 10K, R39 10K, R48 10K

R66 0, R63 0, R62 0, R61 0, R58 0, R59 DNP 0, R60 DNP 0, R57 0, R56 0, R55 0, R64 0

U11

A25 SID0, B28 SID1, B27 SID2, B26 SID3, B25 SID4, B24 SID5, C28 SID6, C27 SID7, C26 SID8, C25 SID9, D24 SADS, D23 MM#

J55 69190-102H

MISC

R16 10K, R15 10K, R14 10K, R13 10K, R42 10K

AF27 SPD0, AG27 SPD1, AG28 SPD2, AH3 FSEL0, AH4 FSEL1, AH2 MCAST

R65 0

S2 97C04ST

OPEN

21-D6 SW_REFCLK_P, 21-D6 SW_REFCLK_N → AP28 REF_CLKP, AE28 REF_CLKN

12-E1,13-E1,14-E1,23-B5 BOARD_RESET → AP1 RST#

10-C3,22-A3,22-B6 SW_TCK → B2 TCK

22-A2 SW_TDI → C1 TDI

10-C3,22-A3,22-B6 SW_TMS → A2 TMS

10-C3,22-A3,22-B6 SW_TRST → C2 TRST#

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80HCPS1848_CEB

3.3V

R45 10K, R44 10K

SCL A27, SDA A26 → SW_SCL, SW_SDA

10-P6,22-B5,22-D6

10-P6,22-B5,22-D6

U36

A2, A1, A0, SDA, SCL, WP, VCC, GND

AT24C64B-10TU-18

C262 0.1U

QCFG have internal pull ups

S1

QCFG0 AE3, QCFG1 AE4, QCFG2 AE5, QCFG3 AF4, QCFG4 AG1, QCFG5 AG2, QCFG6 AG3, QCFG7 AG4

OPEN

97C08SR

REXTP AH27, REXTN AH26 — R72 9.1K

IRQ# D1

TDO B1 — SW_TDO → 22-B3

DNC_AF2 AF2 NC, DNC_AF3 AF3 NC, DNC_AE25 AE25 NC, DNC_AD25 AD25 NC

3.3V

R43 10K

J46 54101-T06-01 DNP

3.3V

U9 74LVC1G125

VCC, 1OE#, 2A, 3GND, Y4

R3 300

Orange LED

D10 LTST-C190EKT

3.3V

R68 56K

D3 S1B

R6 10K

B1, B2, A1, A2

SW1 EVQPAC07K

C362 1U

J53 69190-102H

U5 74LVC1G14

NC, 1NC, VCC, 2A, 3GND, Y4

MCAST is rising edge triggered

This header is for an external pulse generator

FANSINK_COFAN-USA KEM-202B-12
PWR CONNECTOR

12V

J95 A2543WV2-3P

NC

TITLE : 80HCPS1848 CONFIG			
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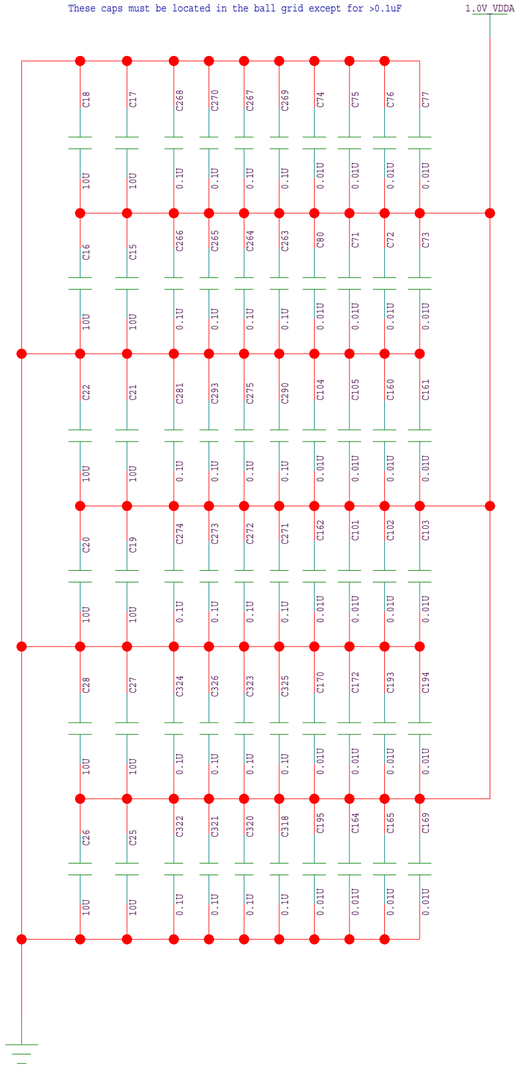
80HCPS1848 Power and Decoupling

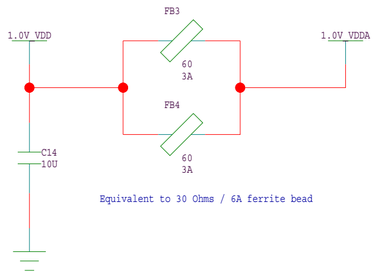
Decoupling 1.0V_VDDA

These caps must be located in the ball grid except for >0.1uF

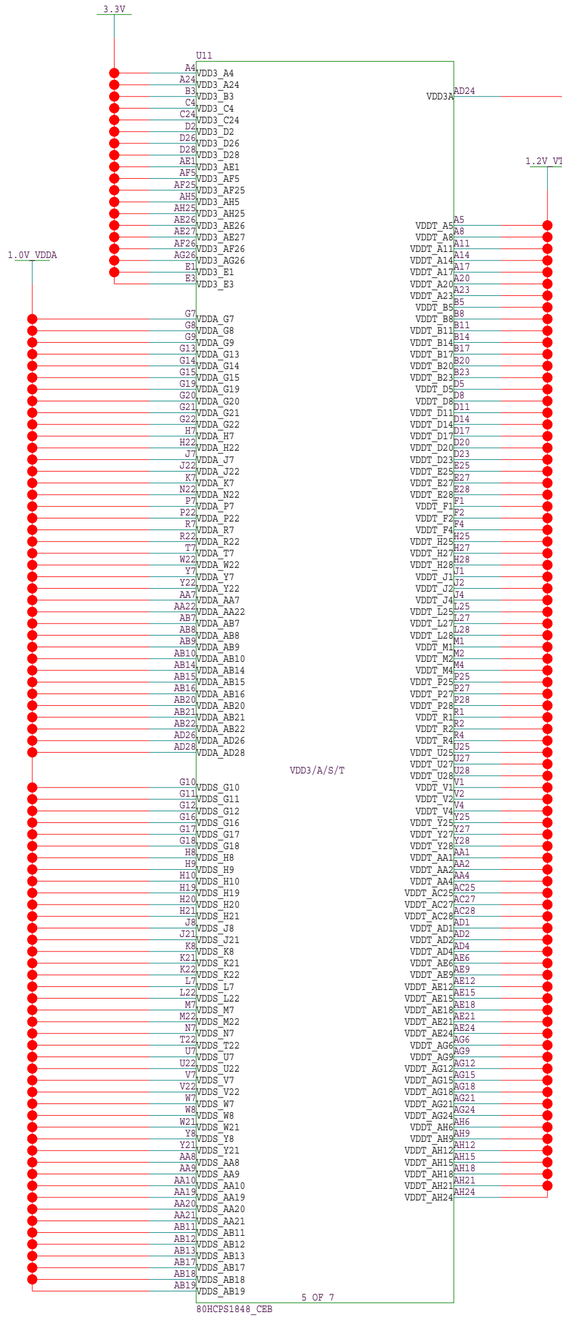


Board layout note:

Make two seperate power planes: 1.0V_VDD and 1.0V_VDDA

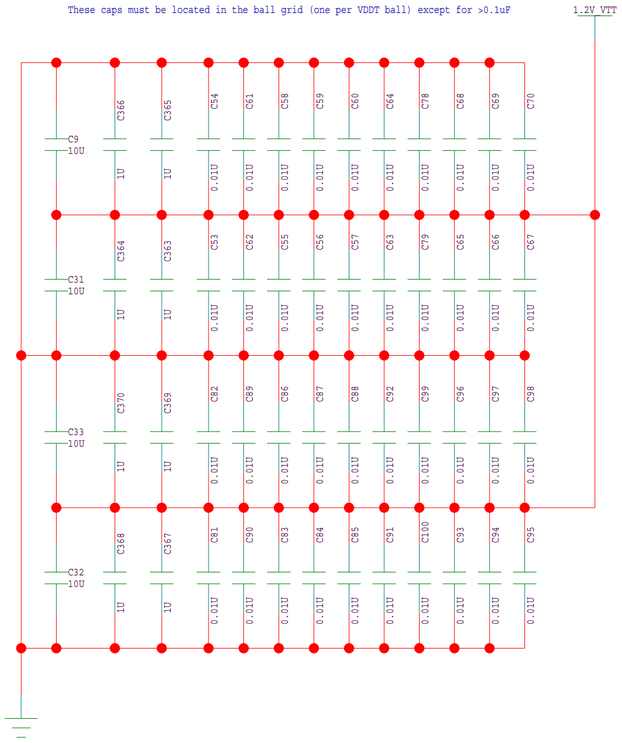


Equivalent to 30 Ohms / 6A ferrite bead



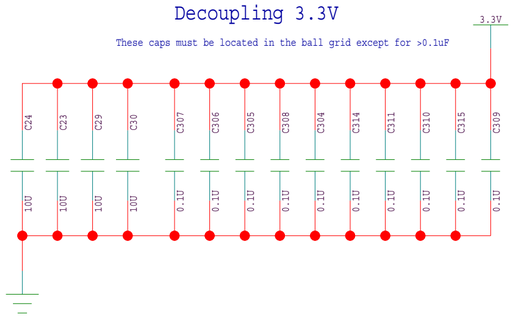
Decoupling 1.2V_VDDT

These caps must be located in the ball grid (one per VDDT ball) except for >0.1uF



Decoupling 3.3V

These caps must be located in the ball grid except for >0.1uF



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TITLE : 80HCPS1848 POWER AND DECOUPLING

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			

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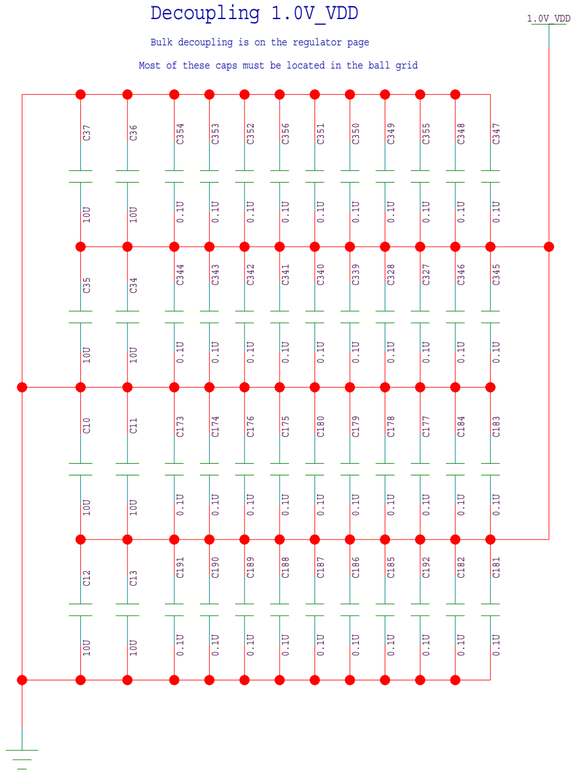
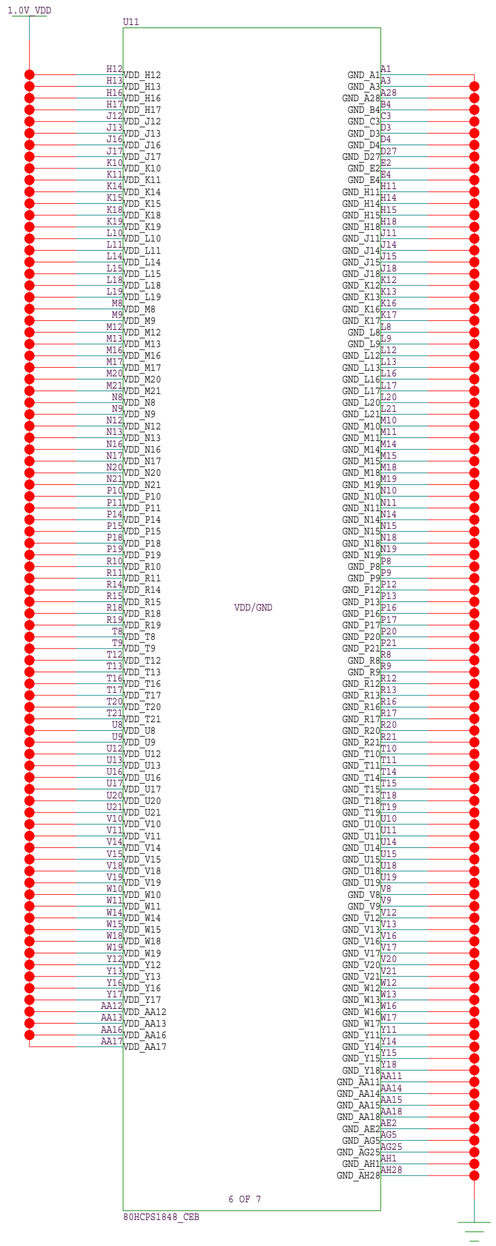
80HCPS1848 Power and Ground

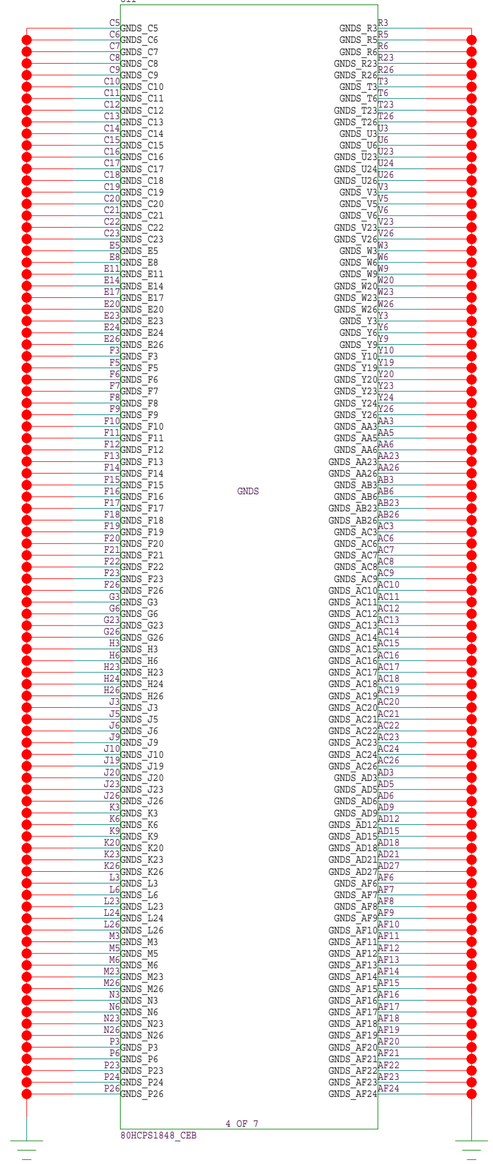
Decoupling 1.0V_VDD

Bulk decoupling is on the regulator page

Most of these caps must be located in the ball grid

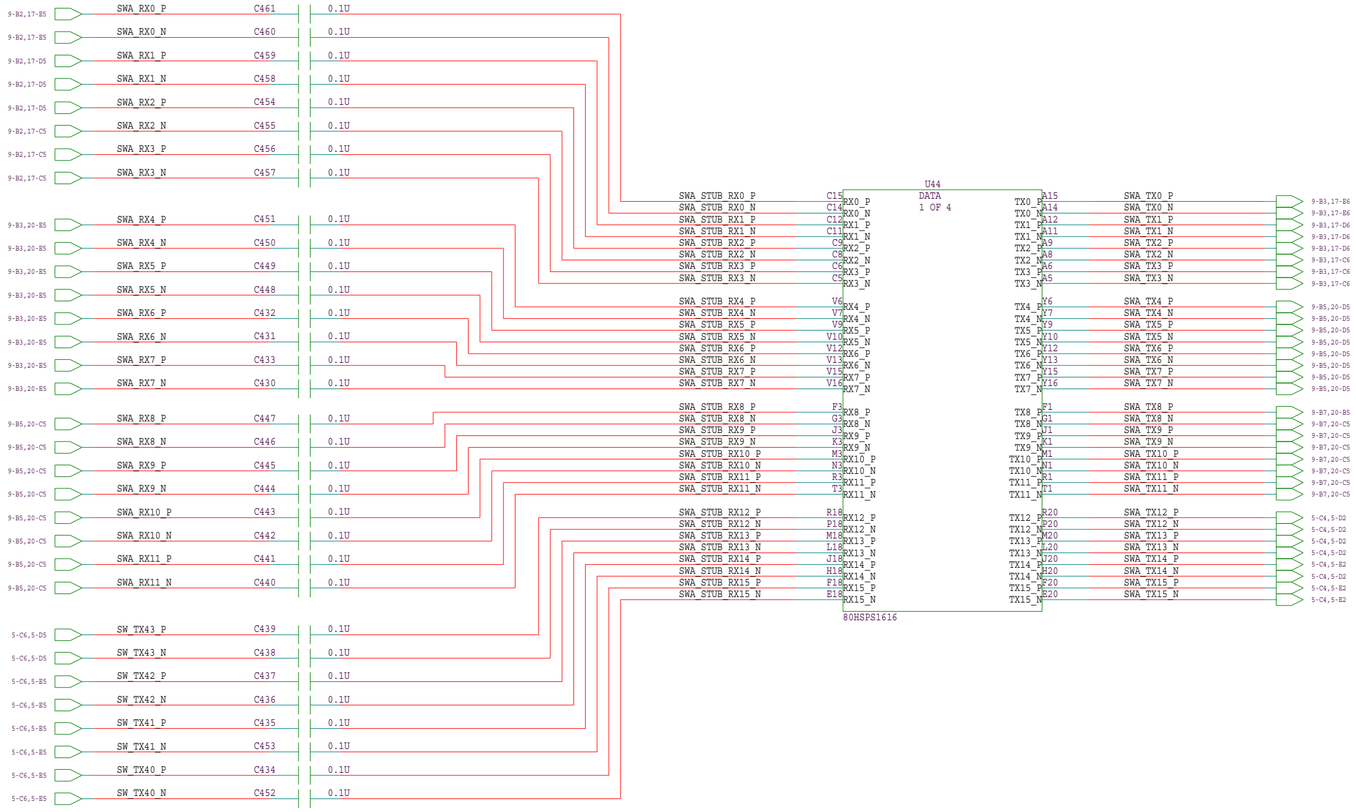




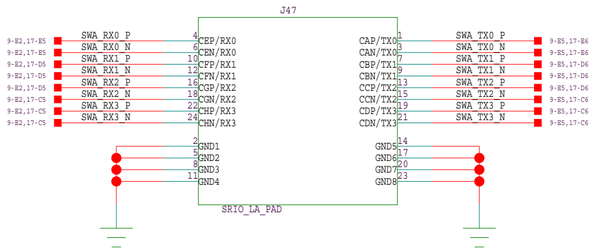


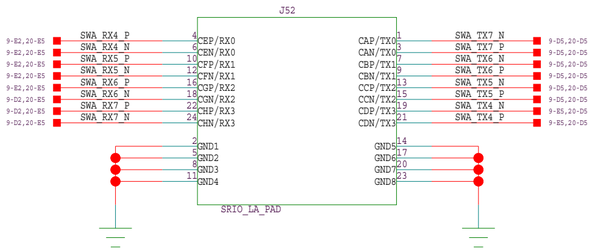
TITLE : 80HCPS1848 POWER AND GROUND			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:46	SHEET 8 OF 25		

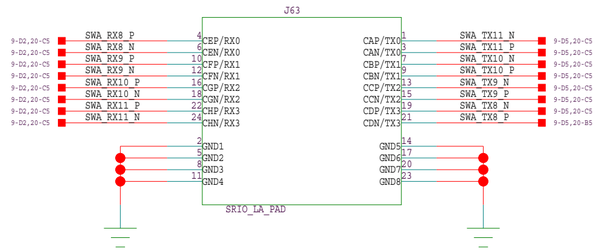
80HSPS1616 Ports



L.A. PADS

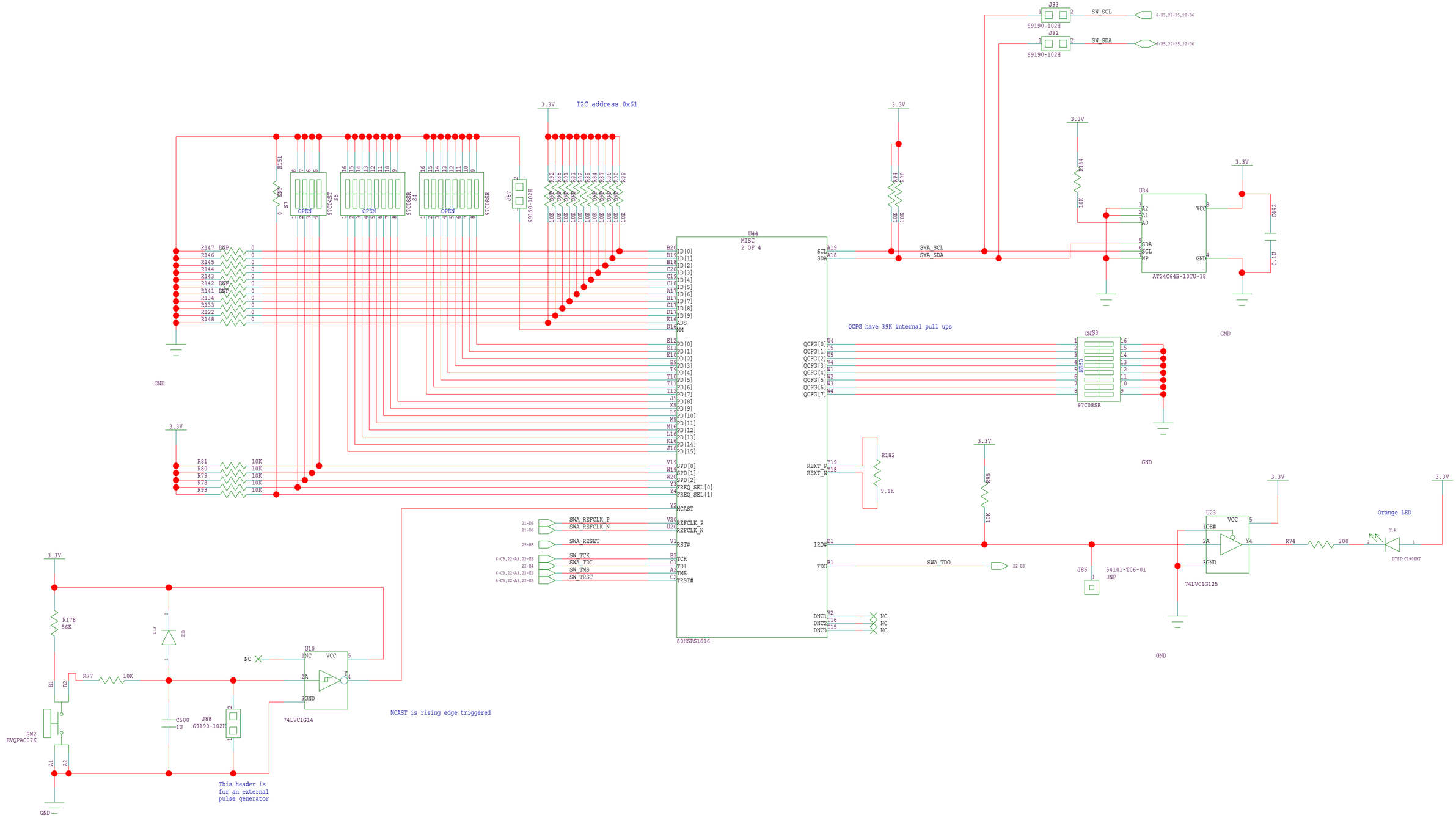






TITLE : 80HSPS1616 PORTS			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:46	SHEET 9 OF 25		

80HSPS1616 Config



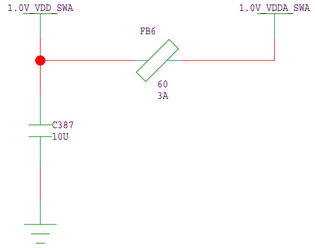
TITLE : 80HSPS1616 CONFIG			
SIZE: C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:46	SHEET 10 OF 25		

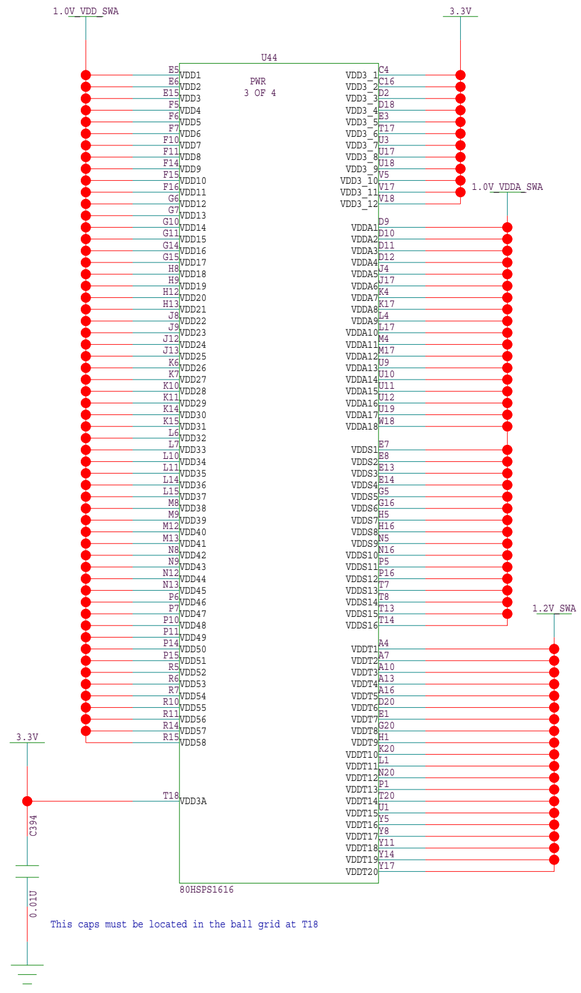
80HSPS1616 Power

Board layout note:

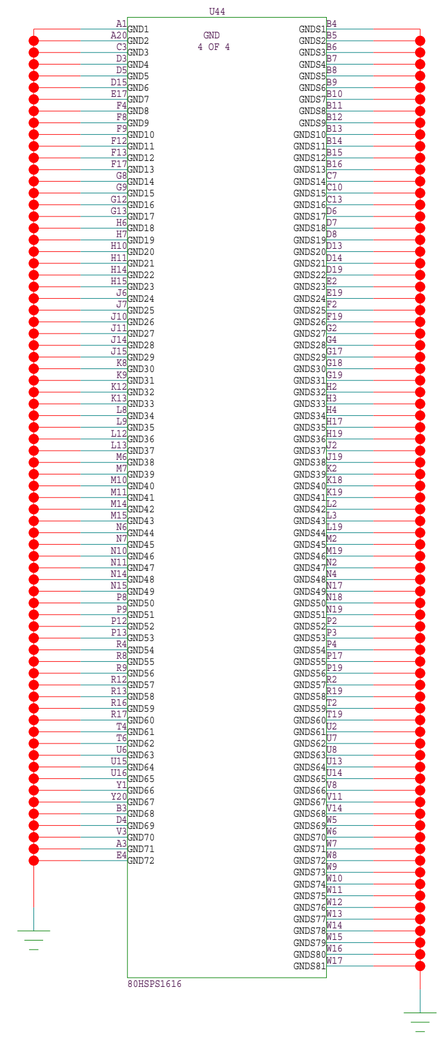
Make two seperate power planes: 1.0V_VDD and 1.0V_VDDA

VDDA ~ 1A
VDDS ~ 0.7A



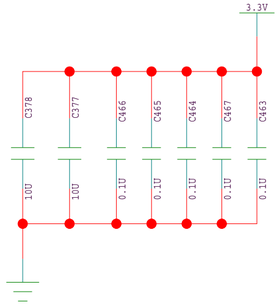


This caps must be located in the ball grid at T18



Decoupling 3.3V

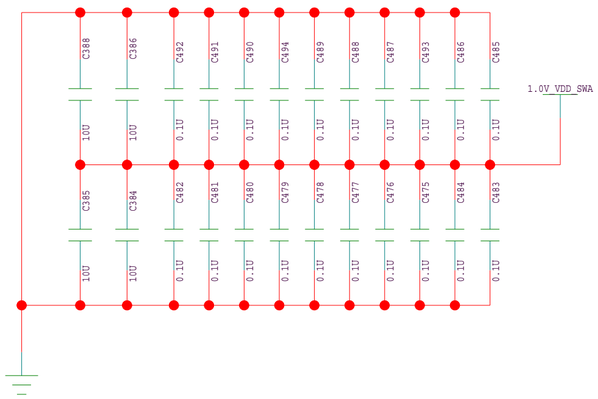
These caps must be located in the ball grid except for >0.1uF



Decoupling 1.0V_VDD

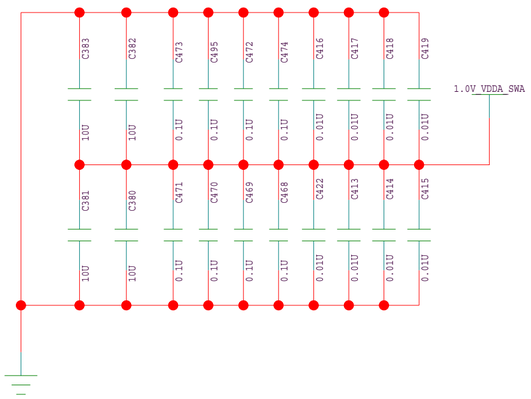
Bulk decoupling is on the regulator page

Most of these caps must be located in the ball grid



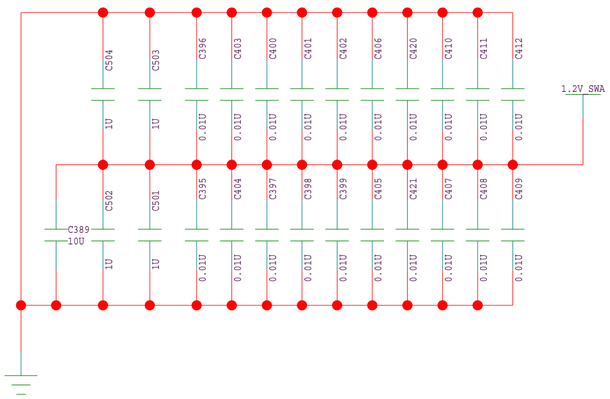
Decoupling 1.0V_VDDA

These caps must be located in the ball grid except for >0.1uF



Decoupling 1.2V_VDDT

These caps must be located in the ball grid (one per VDDT ball) except for >0.1uF



TITLE : 80HSPS1616 POWER			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
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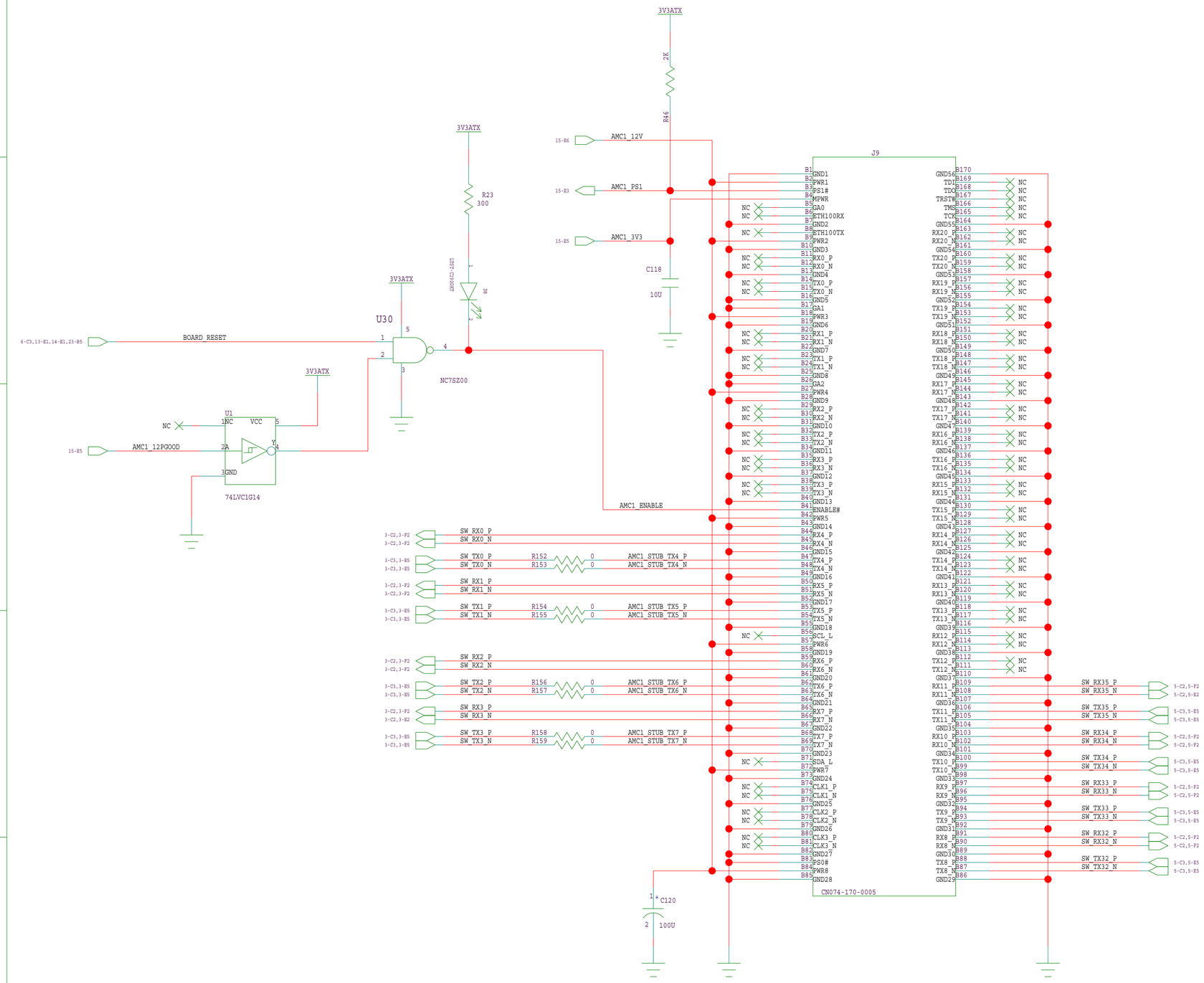
AMC-1 Connector



TITLE :	AMC-1 CONNECTOR
SIZE	C
DRAWING NUMBER :	
Version:	
DESIGNER :	
LAST MODIFIED DATE :	7-22-2010_16:45
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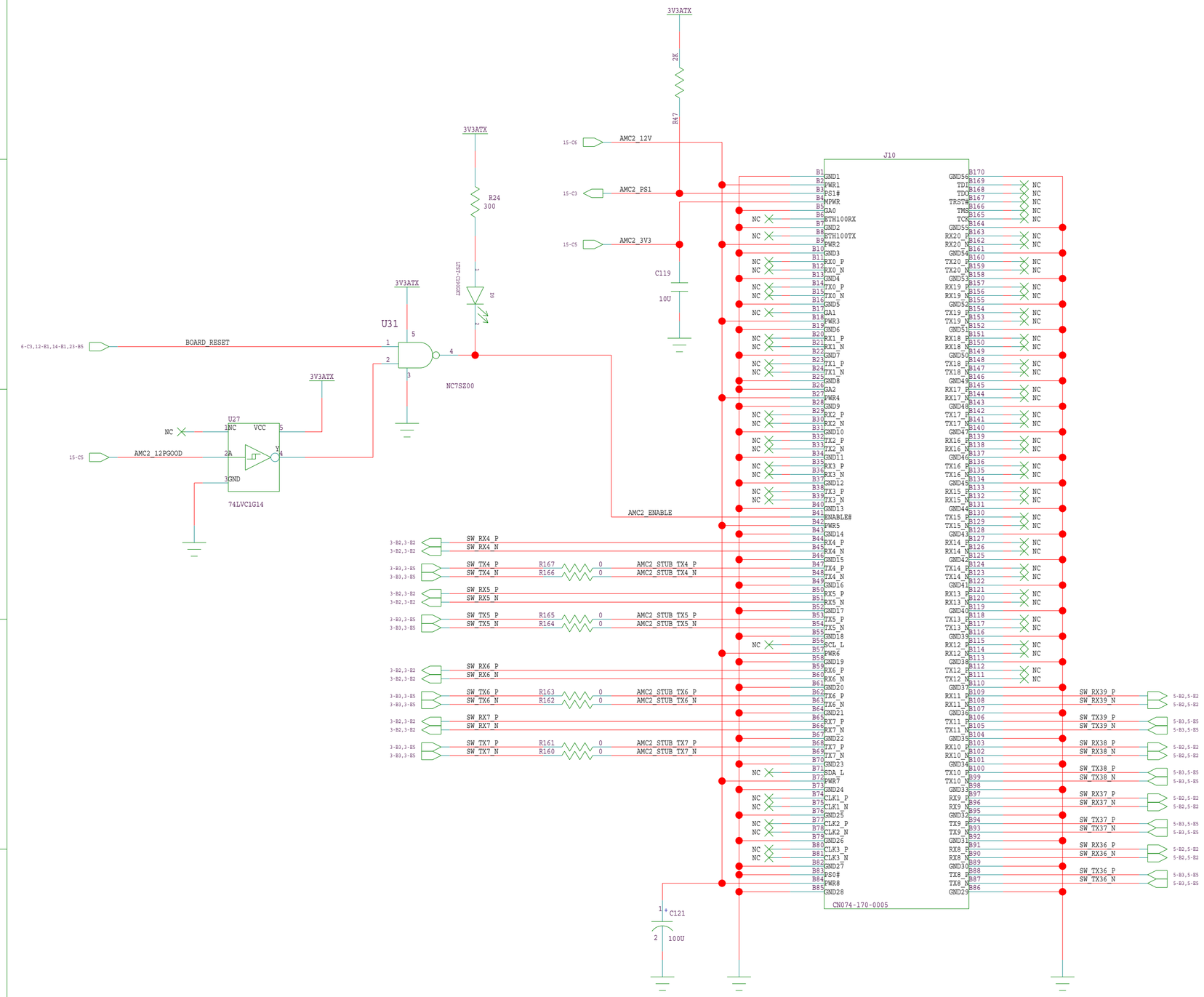
AMC-2 Connector



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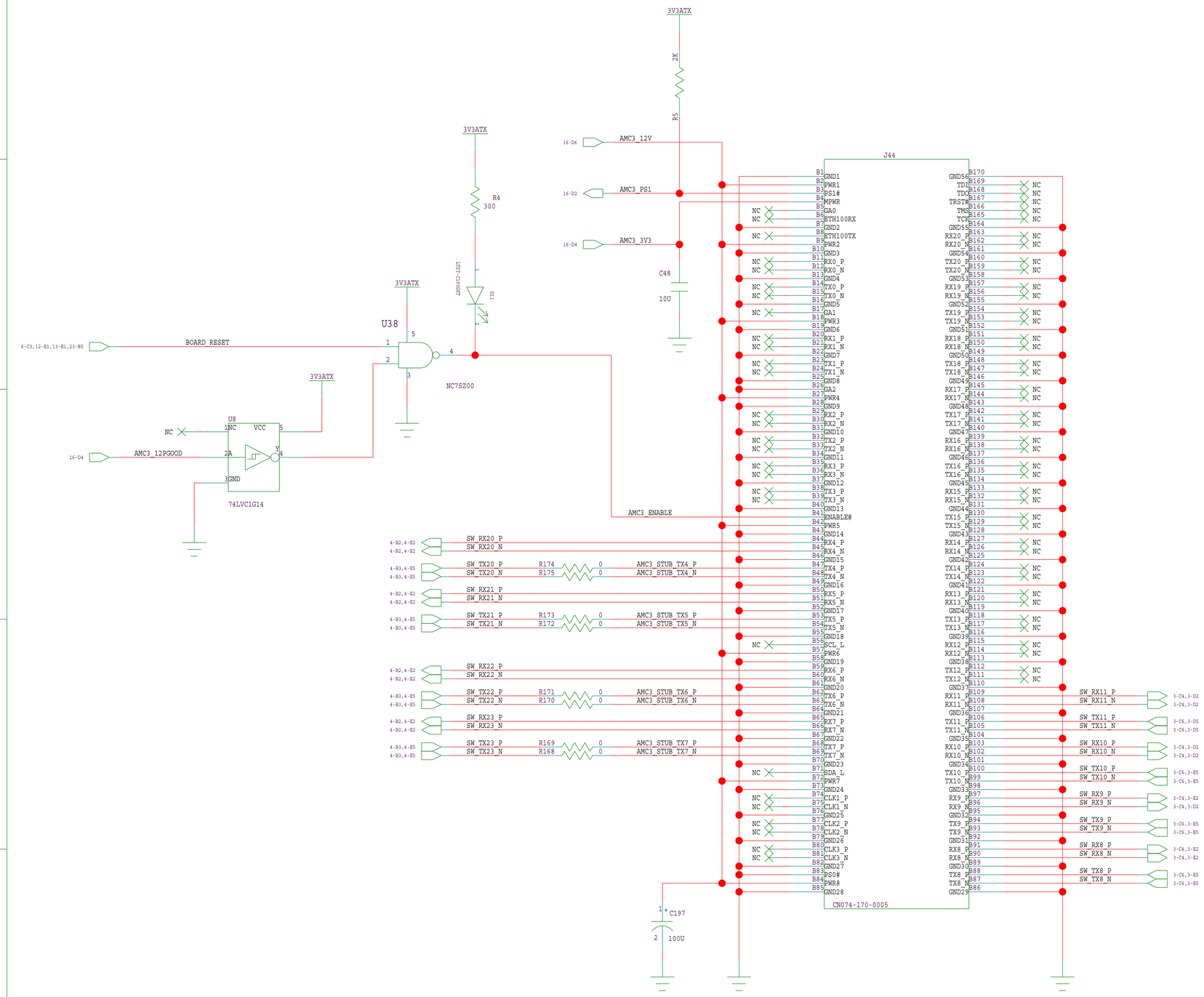
TITLE : AMC-2 CONNECTOR			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:45	SHEET 13 OF 25		

AMC-3 Connector



TITLE :	AMC-3 CONNECTOR
SIZE	C
DRAWING NUMBER :	
Version:	
DESIGNER :	
LAST MODIFIED DATE :	7-22-2010_16:45
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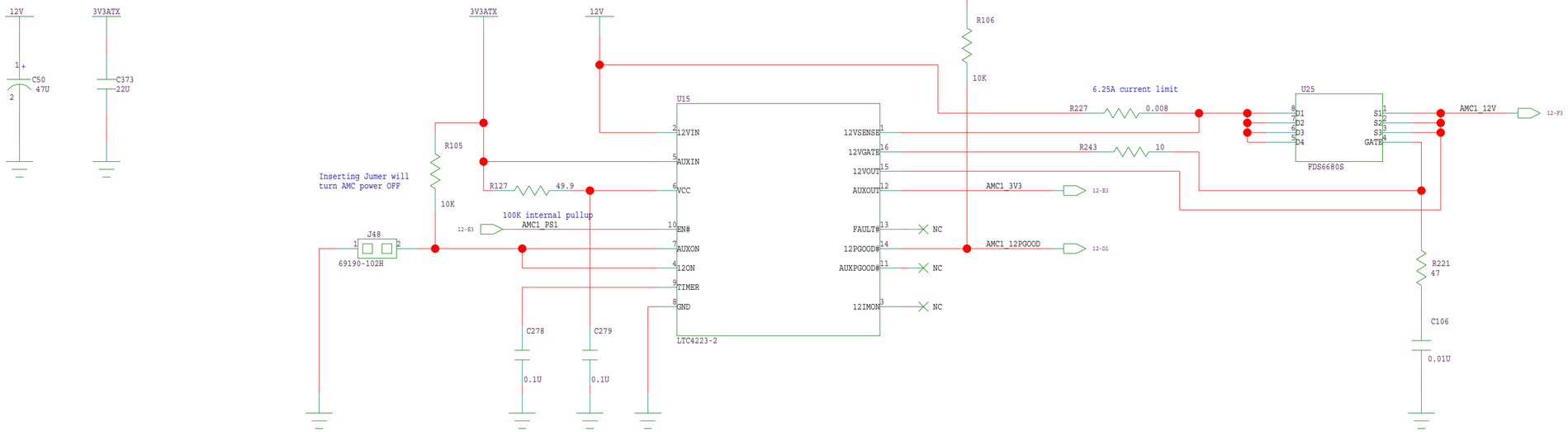
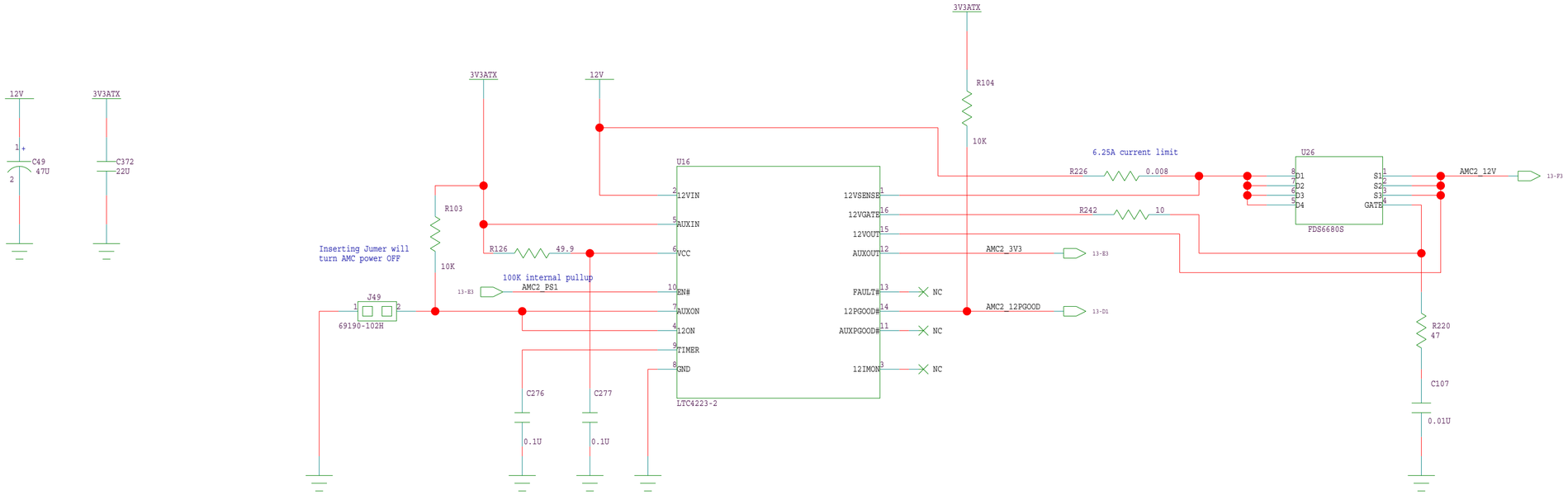
AMC 1 & 2 Hotswap Controllers





IDT

TITLE : AMC 1 & 2 HOTSWAP CONTROLLERS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			

LAST MODIFIED DATE : 7-22-2010_16:45

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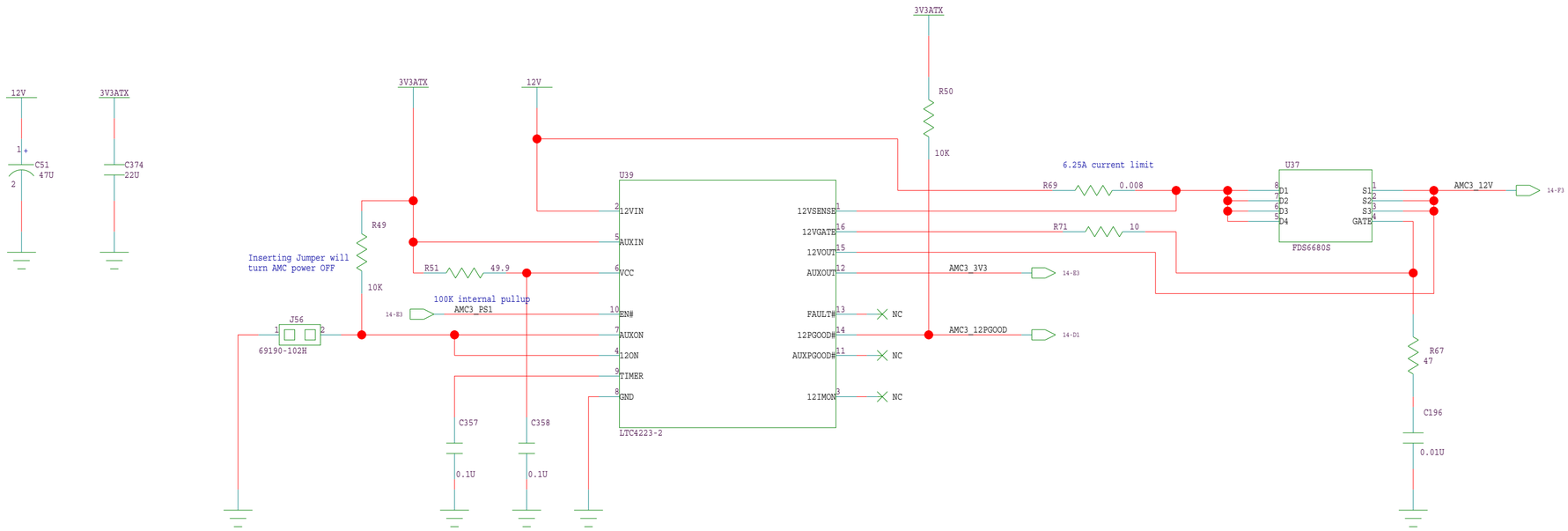
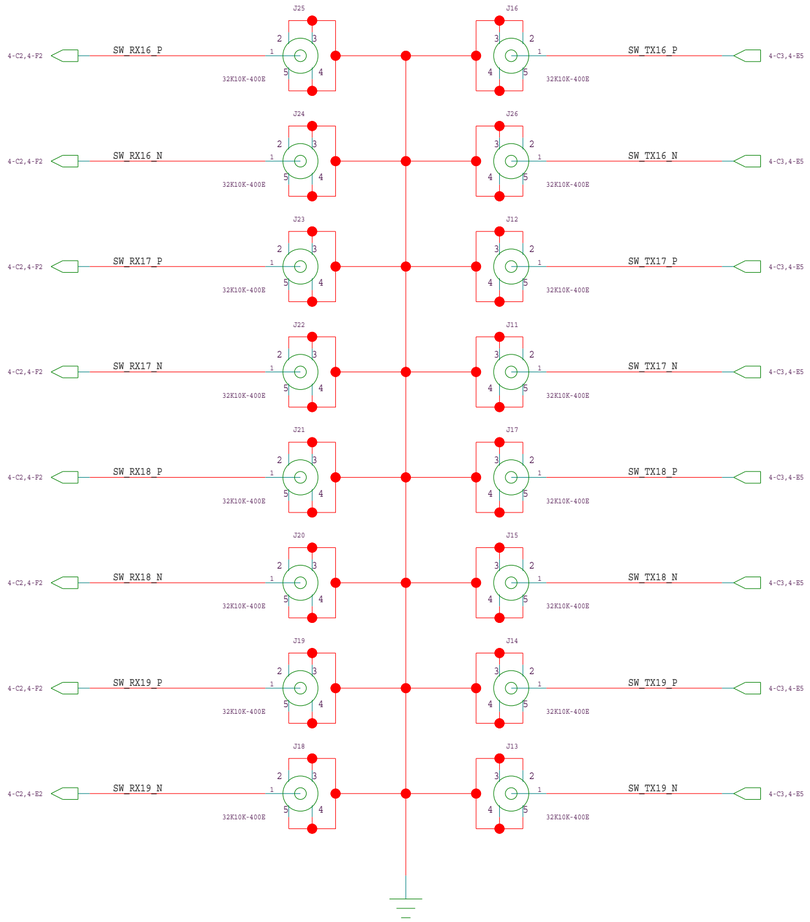
AMC 3 Hotswap Controller



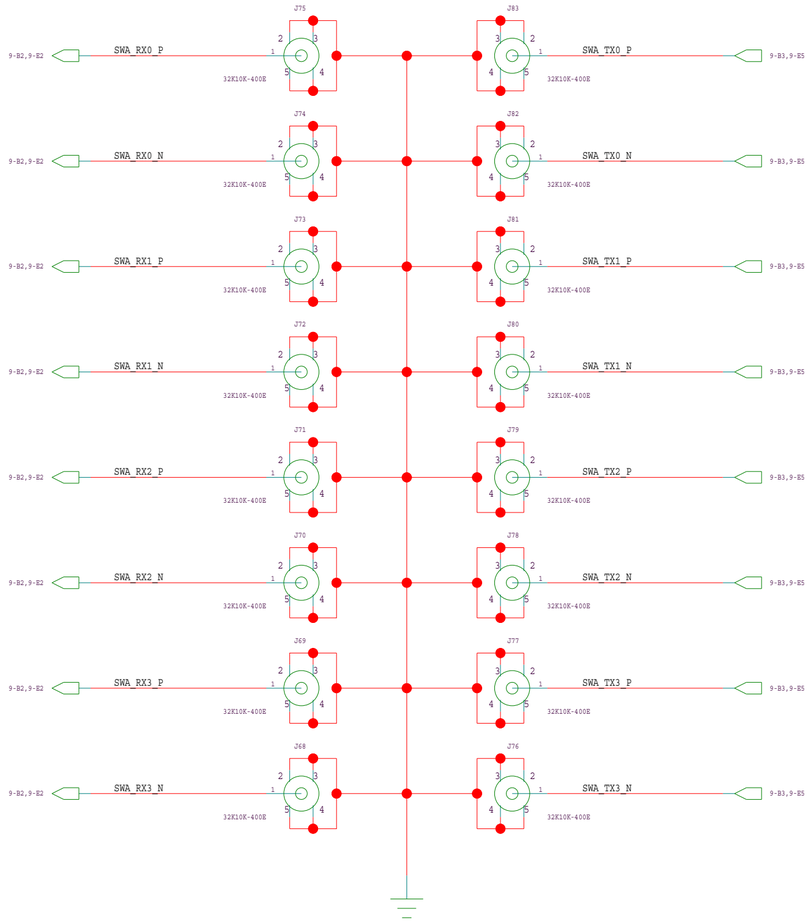
TITLE : AMC 3 HOTSWAP CONTROLLER			
SIZE: C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:45	SHEET 16 OF 25		

SMA Field

80HCPS1848 SMAs

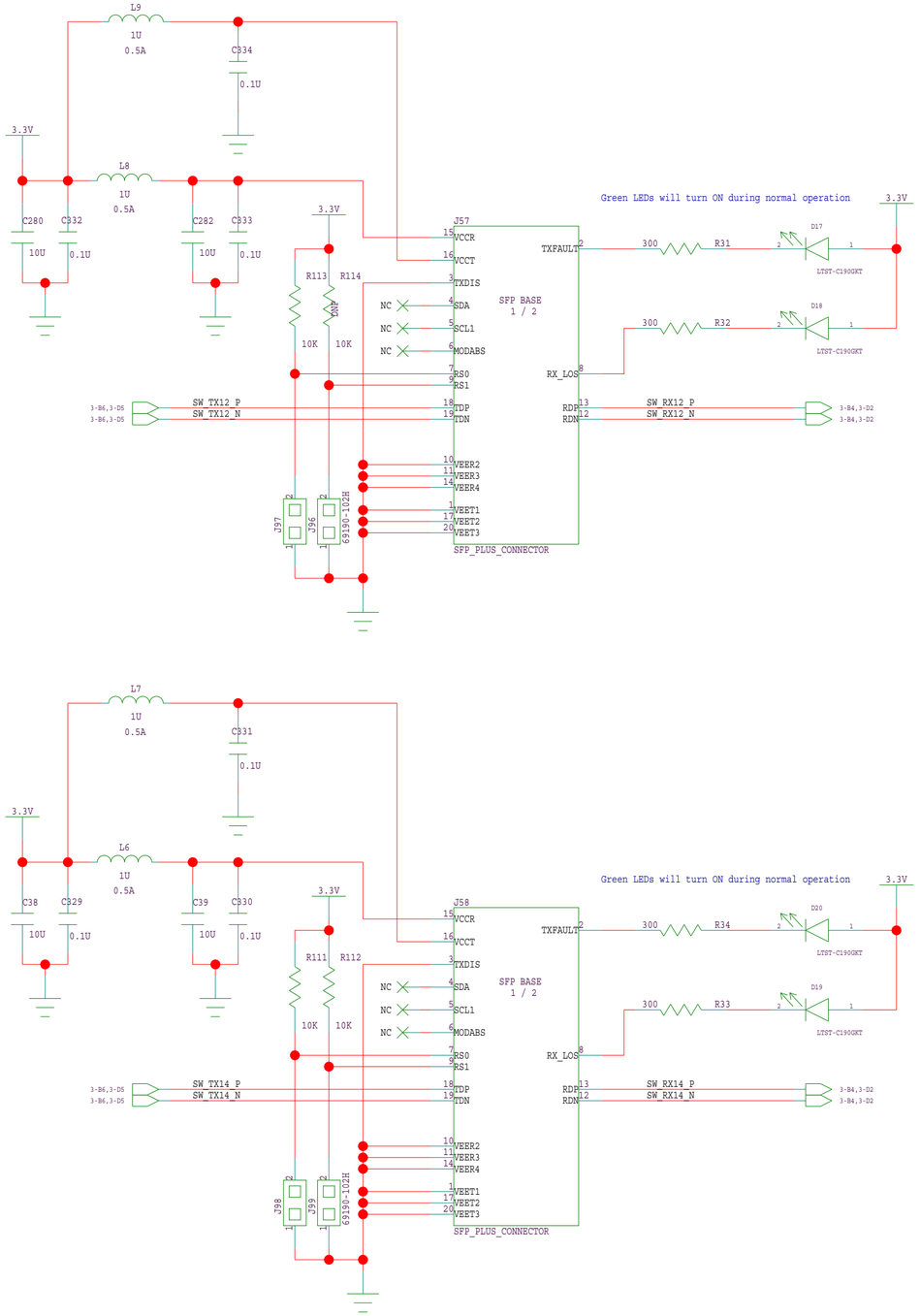


80HSPS1616 SMAs

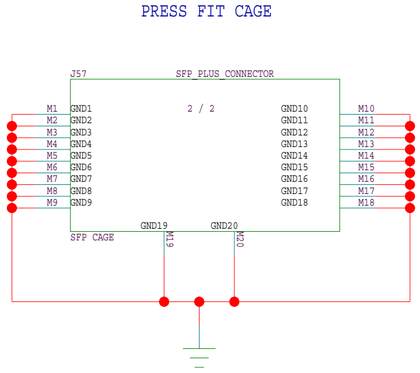


TITLE : SMA FIELD			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:45		SHEET 17 OF 25	

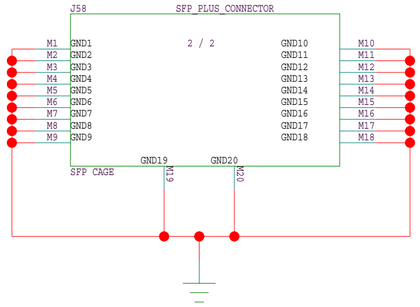
SFP Connectors



PRESS FIT CAGE



PRESS FIT CAGE



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TITLE : SFP CONNECTORS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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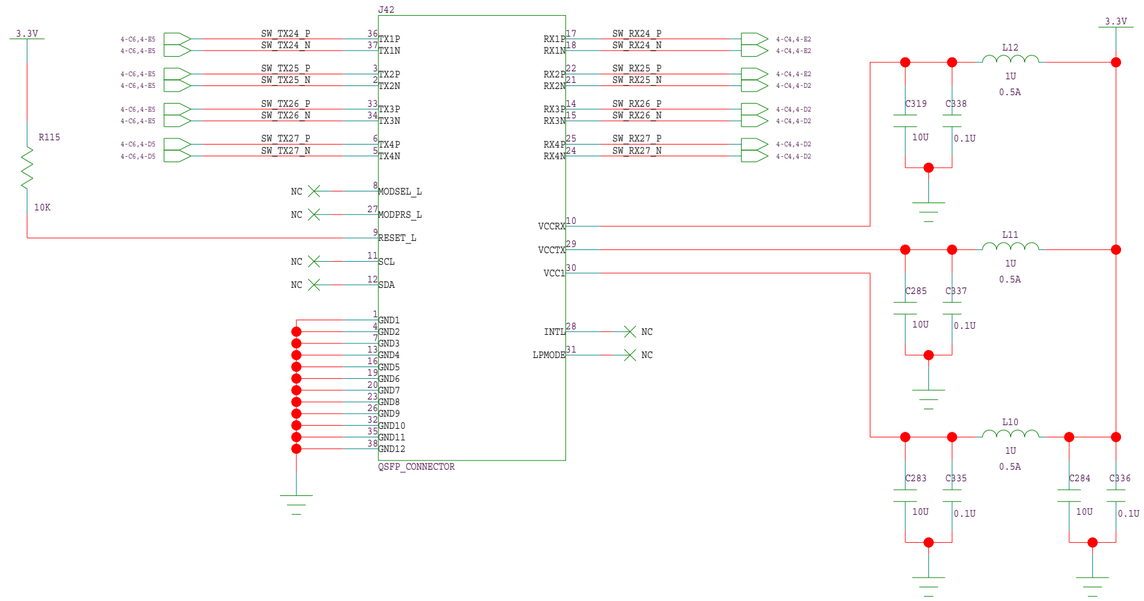
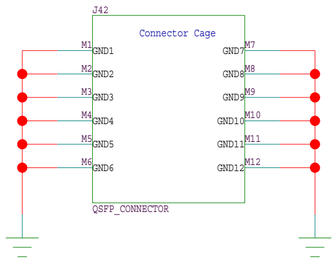
QSFP Connector



PRESS FIT CAGE



TITLE : QSFP CONNECTOR

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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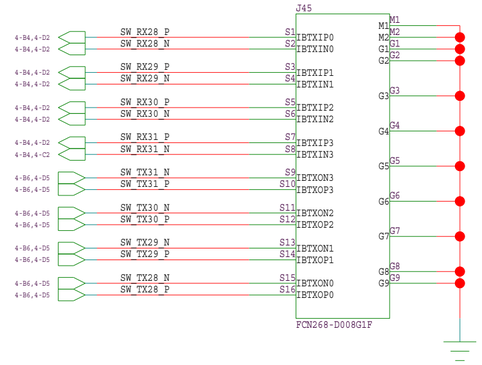
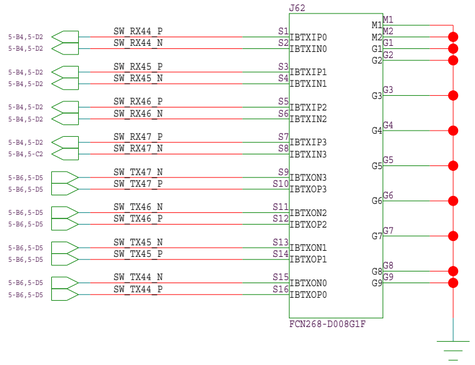
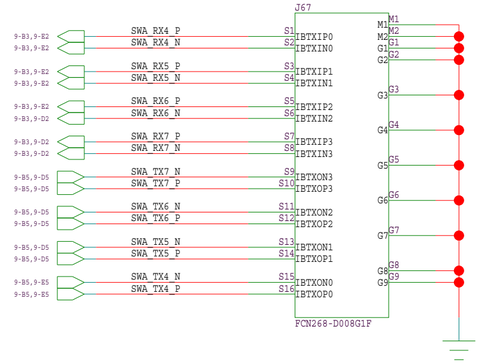
INFINIBAND Connectors

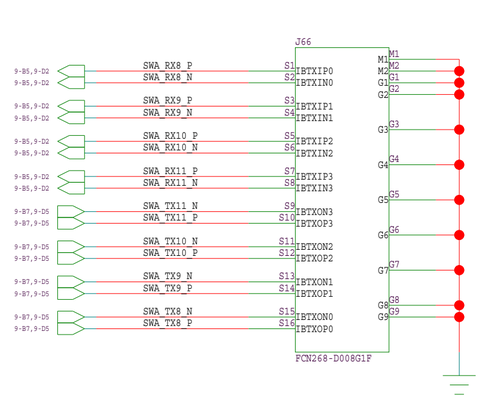
80HCPS1848 Connectors





80HSPS1616 Connectors





TITLE : INFINIBAND CONNECTORS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			

LAST MODIFIED DATE : 7-22-2010_16:45

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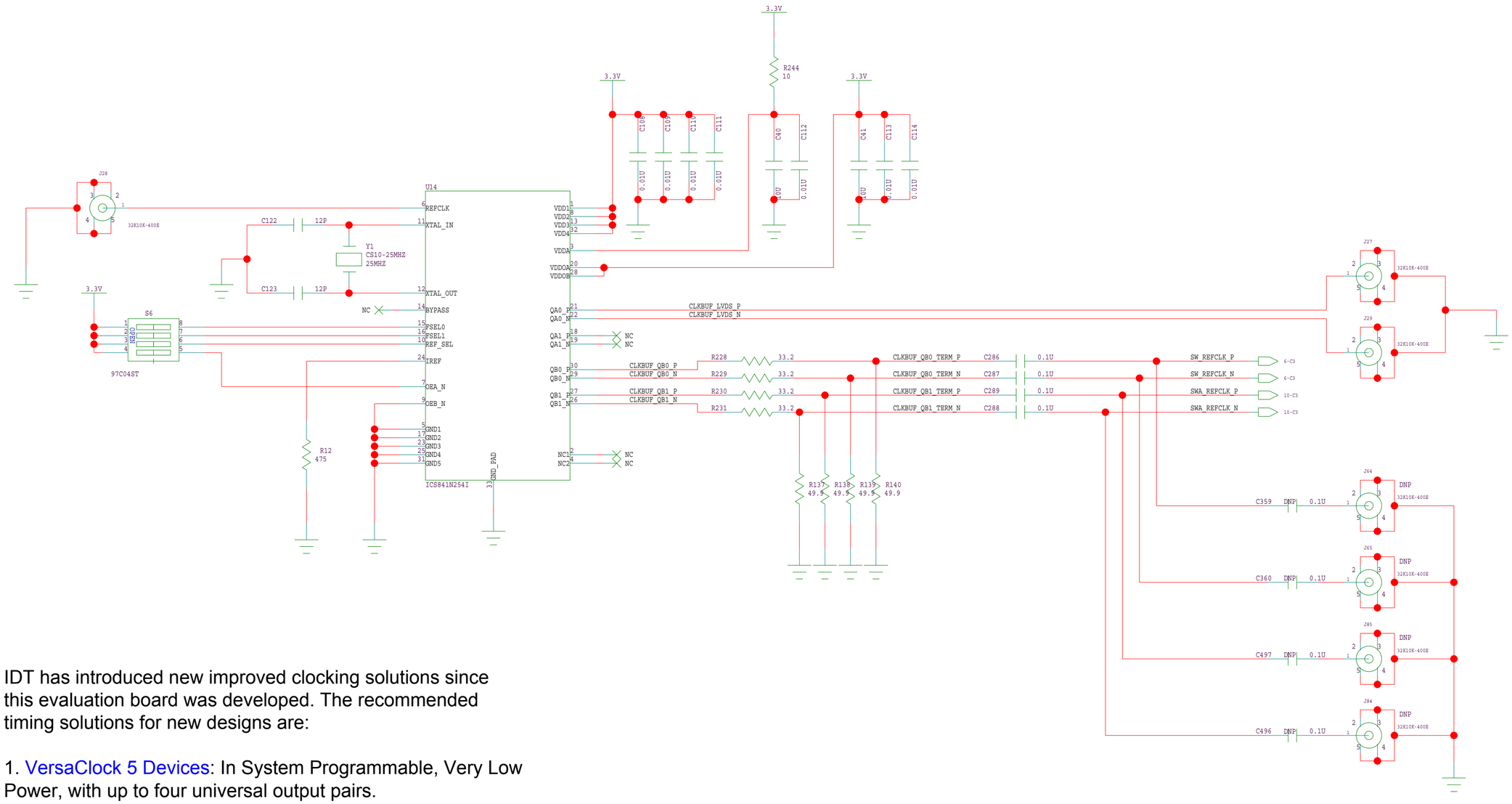
Clocking



IDT has introduced new improved clocking solutions since this evaluation board was developed. The recommended timing solutions for new designs are:

1. VersaClock 5 Devices: In System Programmable, Very Low Power, with up to four universal output pairs.

2. XUM LVDS Crystal Oscillator: Ultra precise with only 300fs typical phase jitter. If using a 156.25 MHz clock source then the applicable part number is XUM535156.250JS6I8.

TITLE : CLOCKING				
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :	
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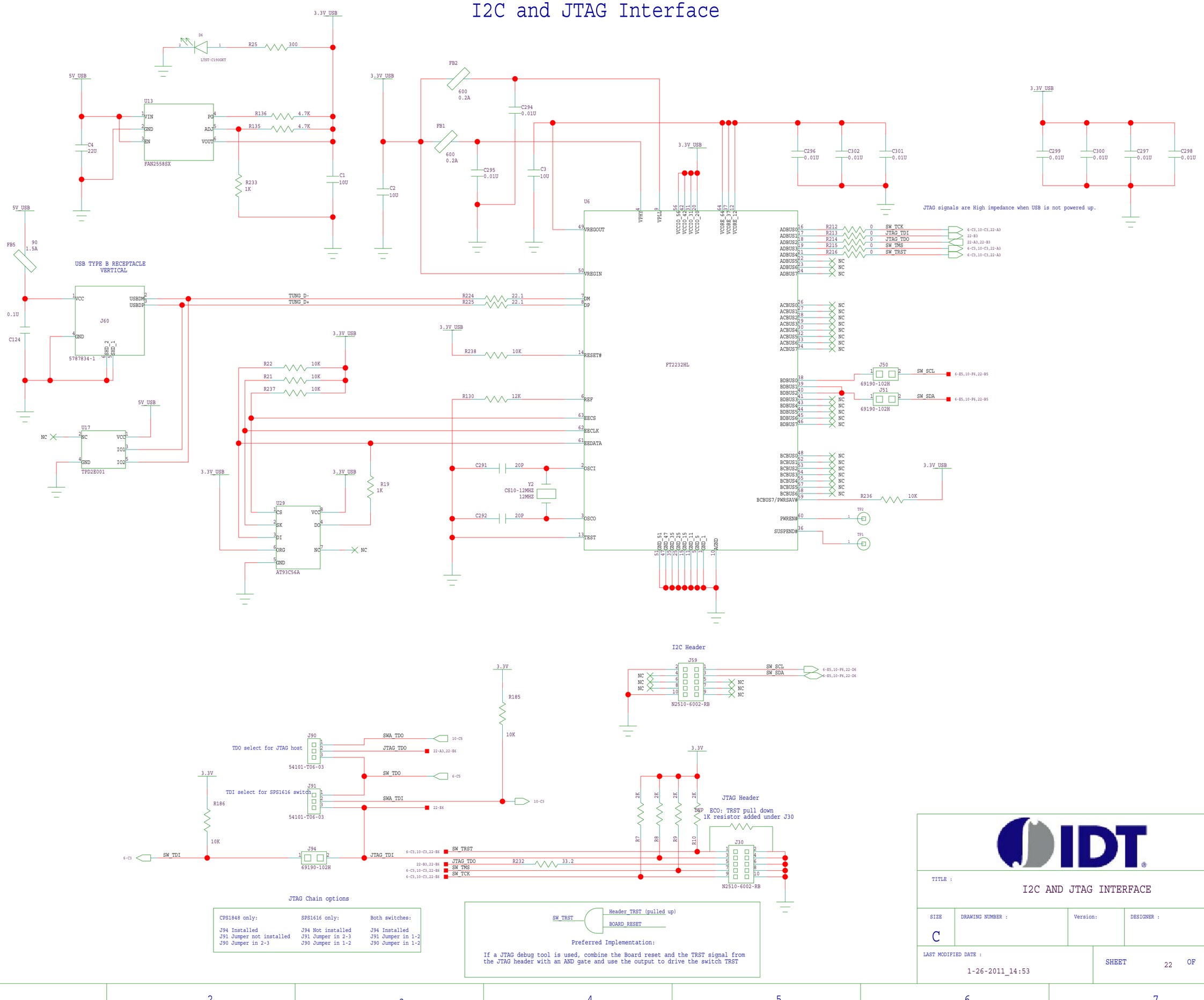
I2C and JTAG Interface



JTAG Chain options

CPS1848 only:	SPS1616 only:	Both switches:
J94 Installed	J94 Not installed	J94 Installed
J91 Jumper not installed	J91 Jumper in 2-3	J91 Jumper in 1-2
J90 Jumper in 2-3	J90 Jumper in 1-2	J90 Jumper in 1-2

Preferred Implementation:

If a JTAG debug tool is used, combine the Board reset and the TRST signal from the JTAG header with an AND gate and use the output to drive the switch TRST

IDT

TITLE :

I2C AND JTAG INTERFACE

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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1-26-2011_14:53

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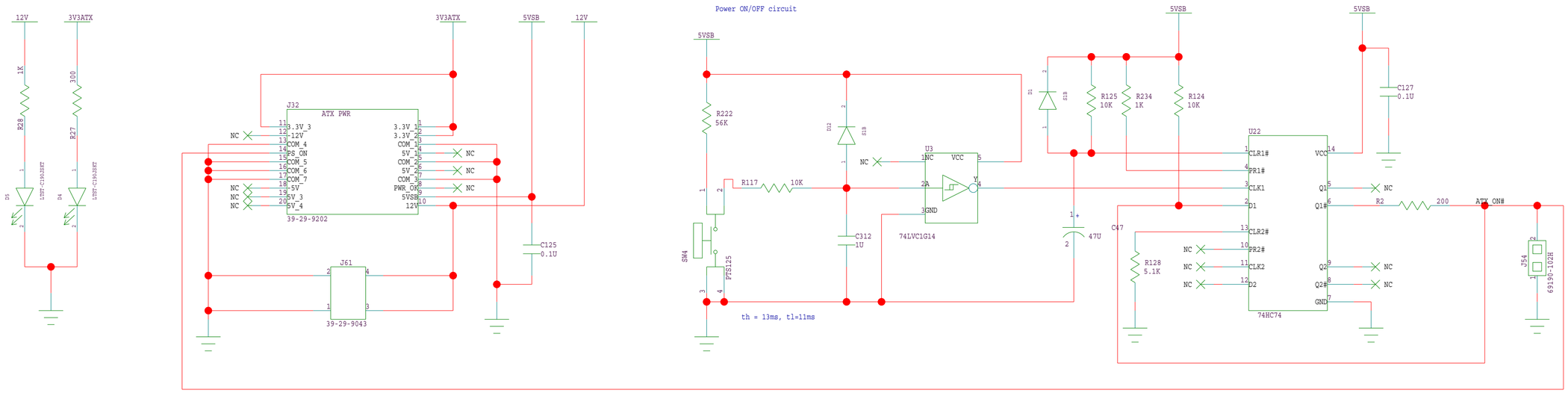
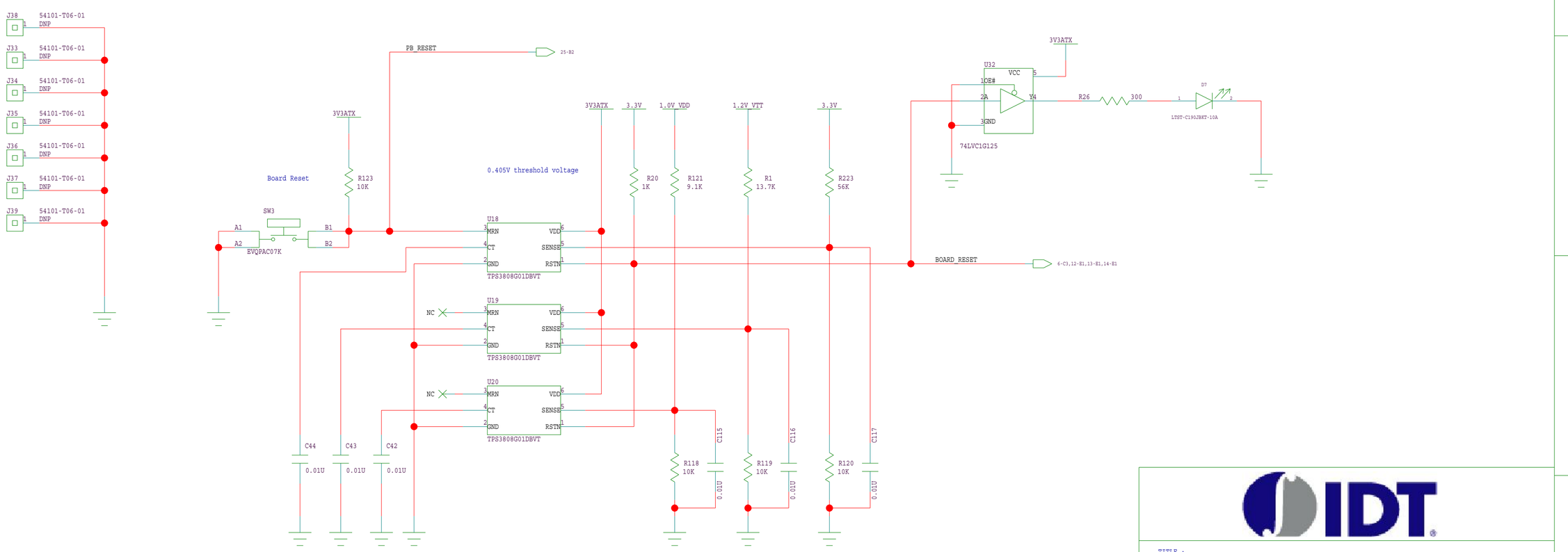
ATX Power



Voltage Monitors

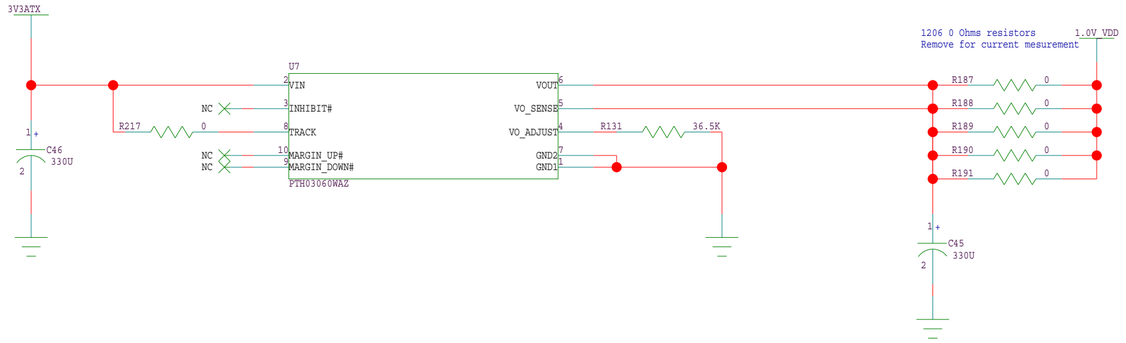
Board Reset

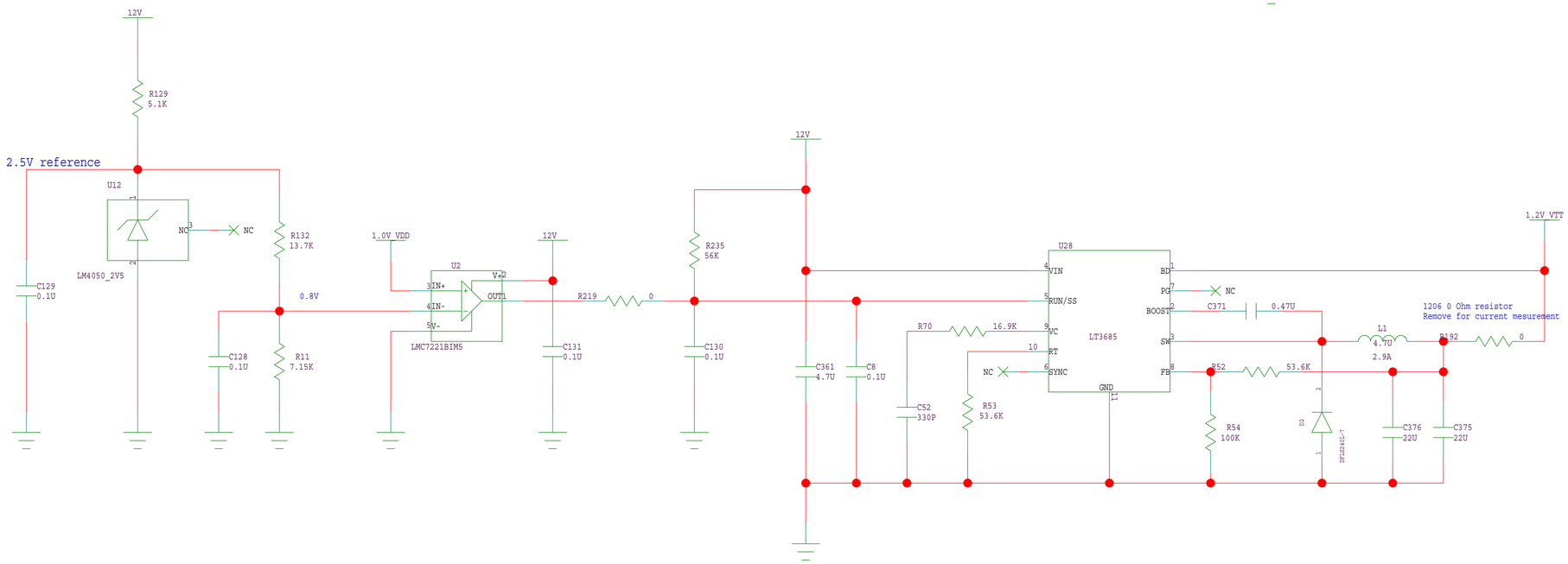


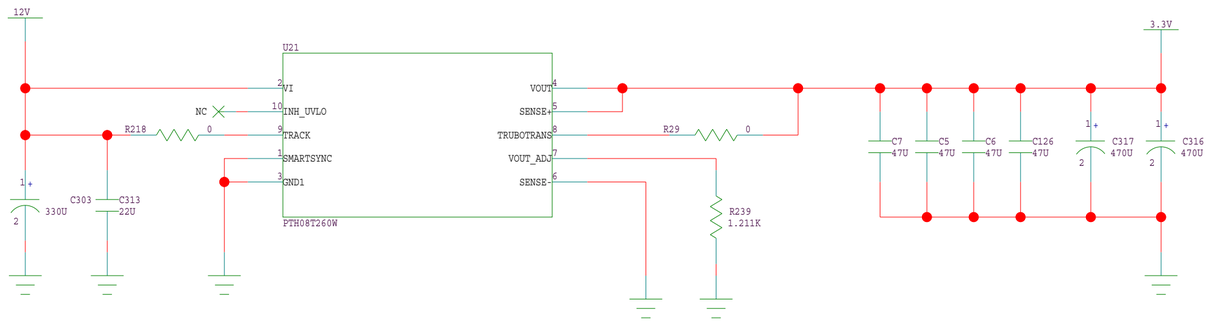
TITLE : ATX POWER			
SIZE: C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:45	SHEET 23 OF 25		

Voltage Regulators for 80HCPS1848

Following power-up sequence is necessary in order for the device to function properly: The serdes voltage (VDDS) needs to power-up first followed by serdes voltage (VDDT). The voltages on any Input or I/O pins cannot exceed its corresponding supply voltage during power supply ramp up.







IDT

TITLE :

80HCPS1848 REGULATORS

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			

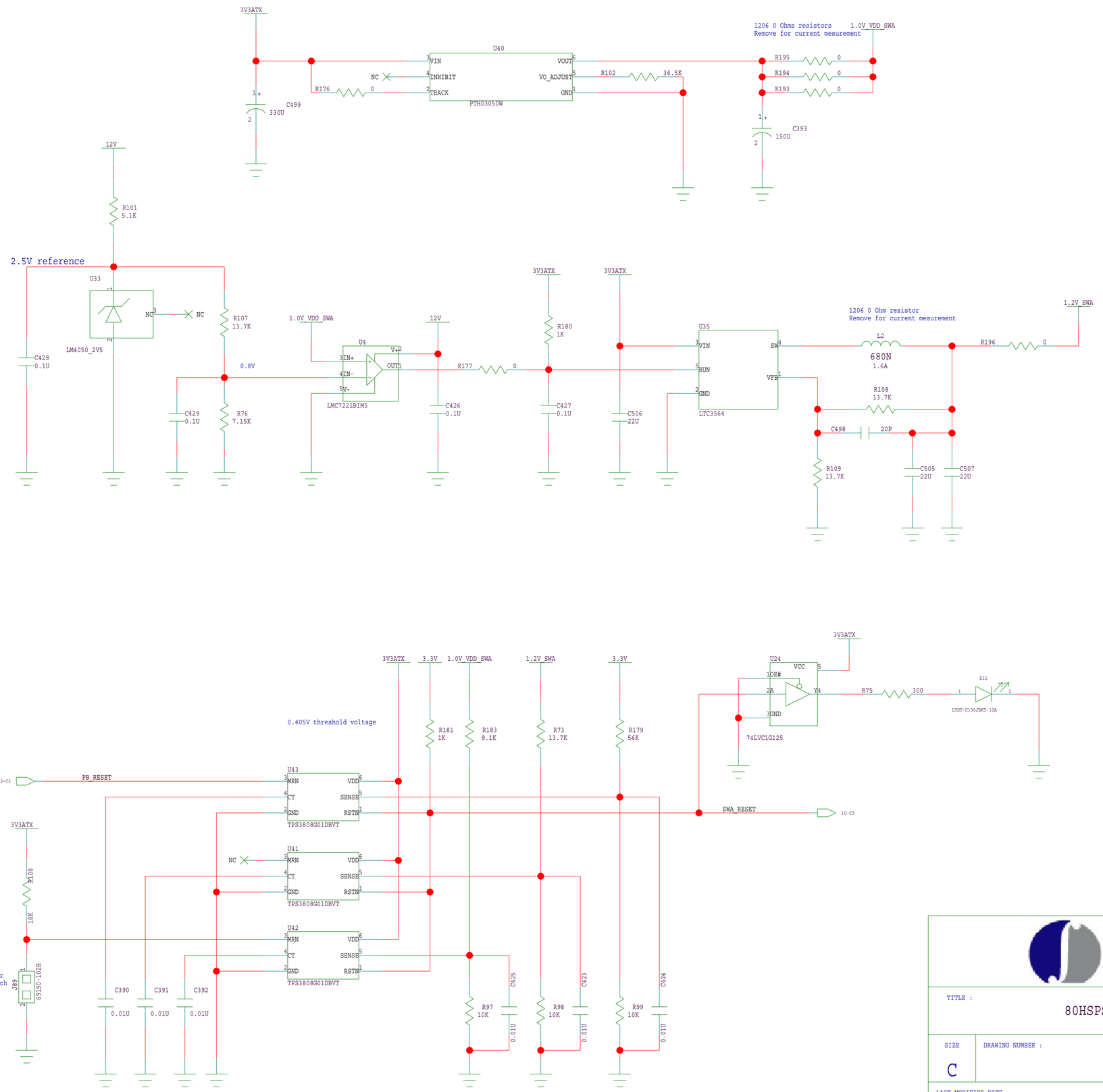
LAST MODIFIED DATE :

7-22-2010_16:45

SHEET 24 OF 25

Voltage Regulators for 80HSPS1616

Following power-up sequence is necessary in order for the device to function properly: The serdes voltage (VDDS) needs to power-up first followed by serdes voltage (VDDT). The voltages on any Input or I/O pins cannot exceed its corresponding supply voltage during power supply ramp up.



TITLE : 80HSPS1616 REGULATORS			
SIZE: C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:45	SHEET 25 OF 25		

Revision History

April 7, 2015 -- Added a note on sheet 21 on improving clocking solutions for S-RIO components.

April 1, 2011 -- Changed FB3/FB4 on sheet 7, and FB6 on sheet 11, to 60 Ohms 3A.

January 26, 2011 -- Added a JTAG TRST implementation note on sheet 22.

September 13, 2010 -- Updated the JTAG Header resistor on sheet 22.

July 26, 2010 -- First release of document.

TITLE : Revision History			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE :	SHEET		