

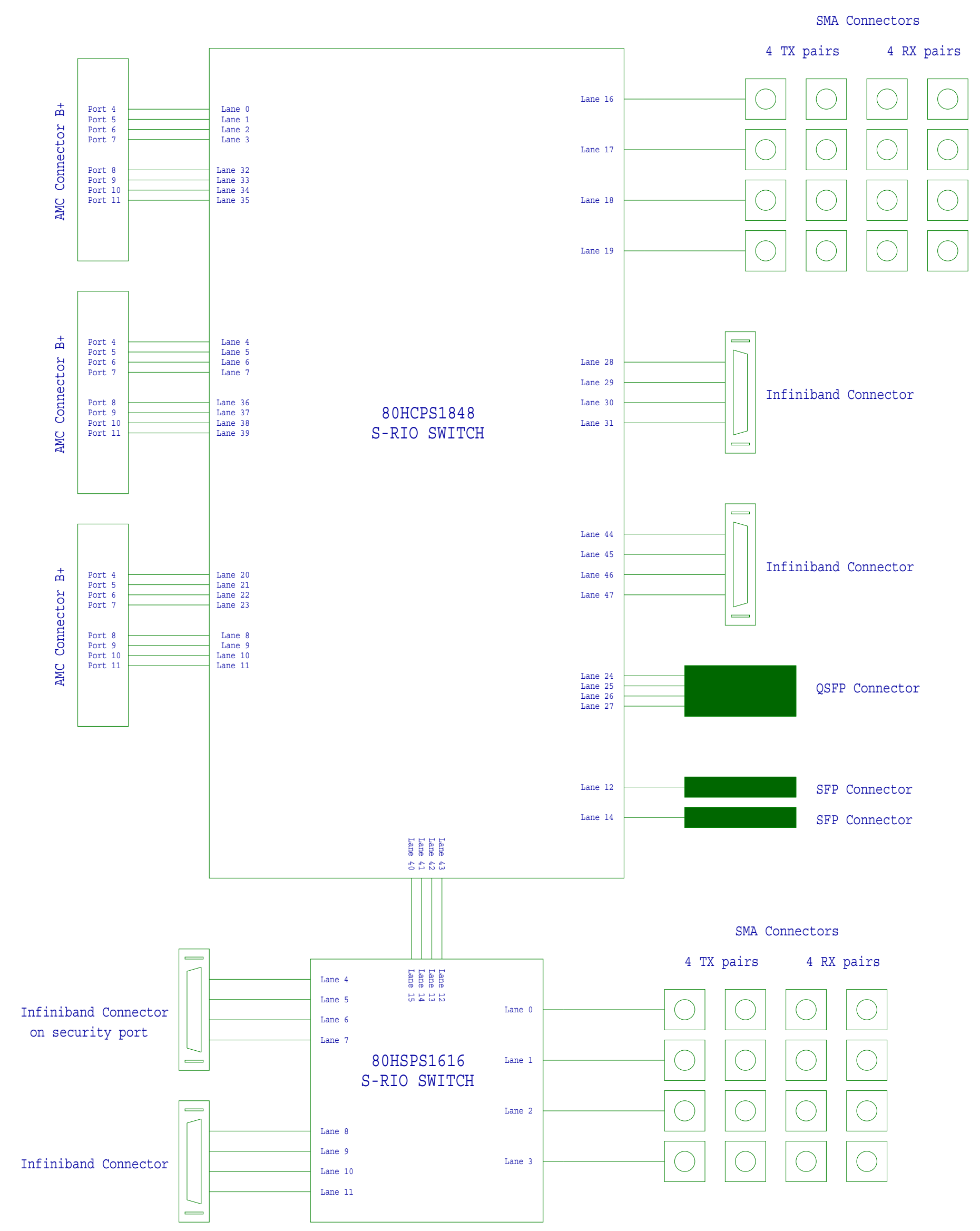
Serial RapidIO Gen2 Development Platform (SRDP2)

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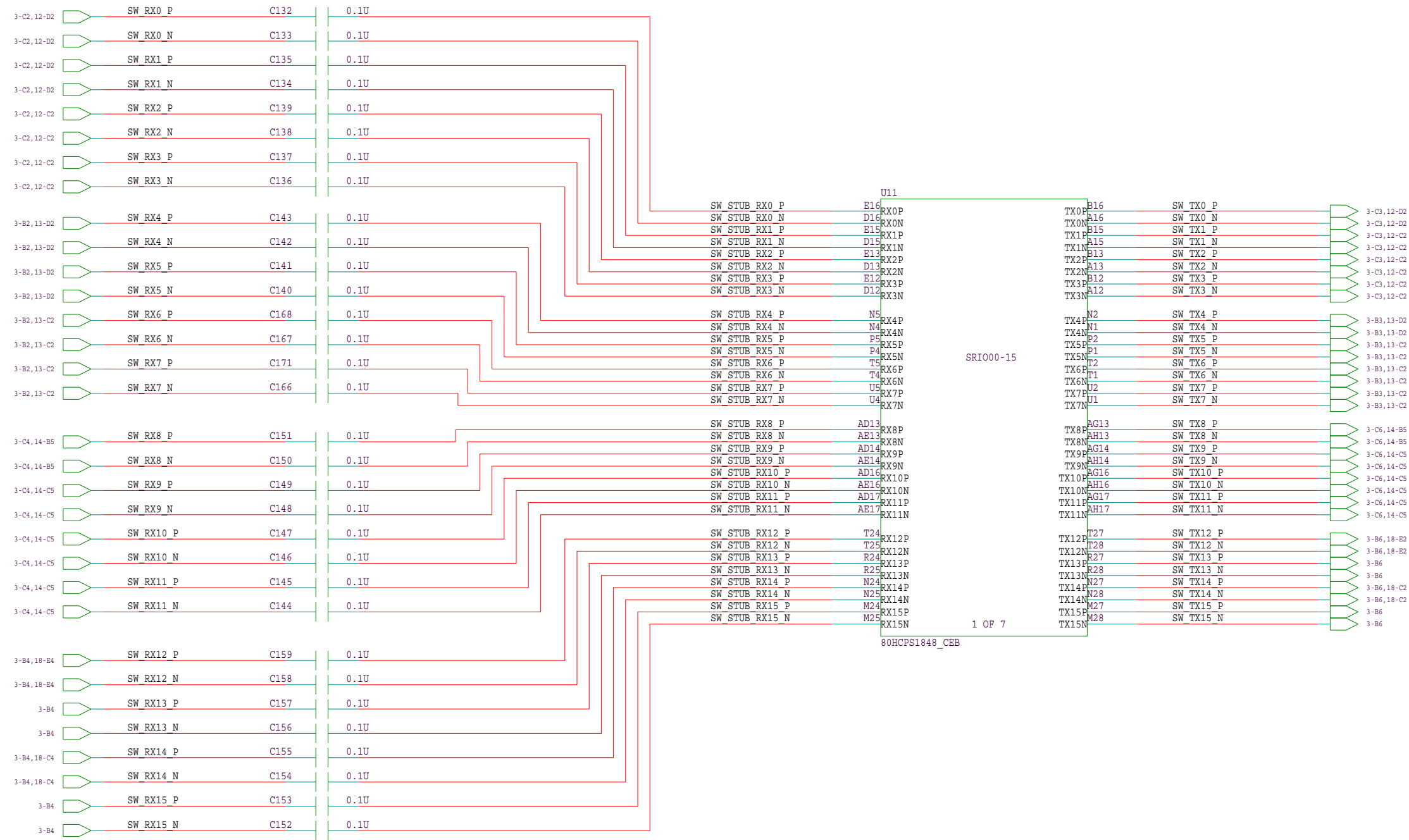
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TITLE SHEET			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
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LAST MODIFIED DATE :		SHEET 1 OF 25	
7-22-2010_16:46			

Block Diagram

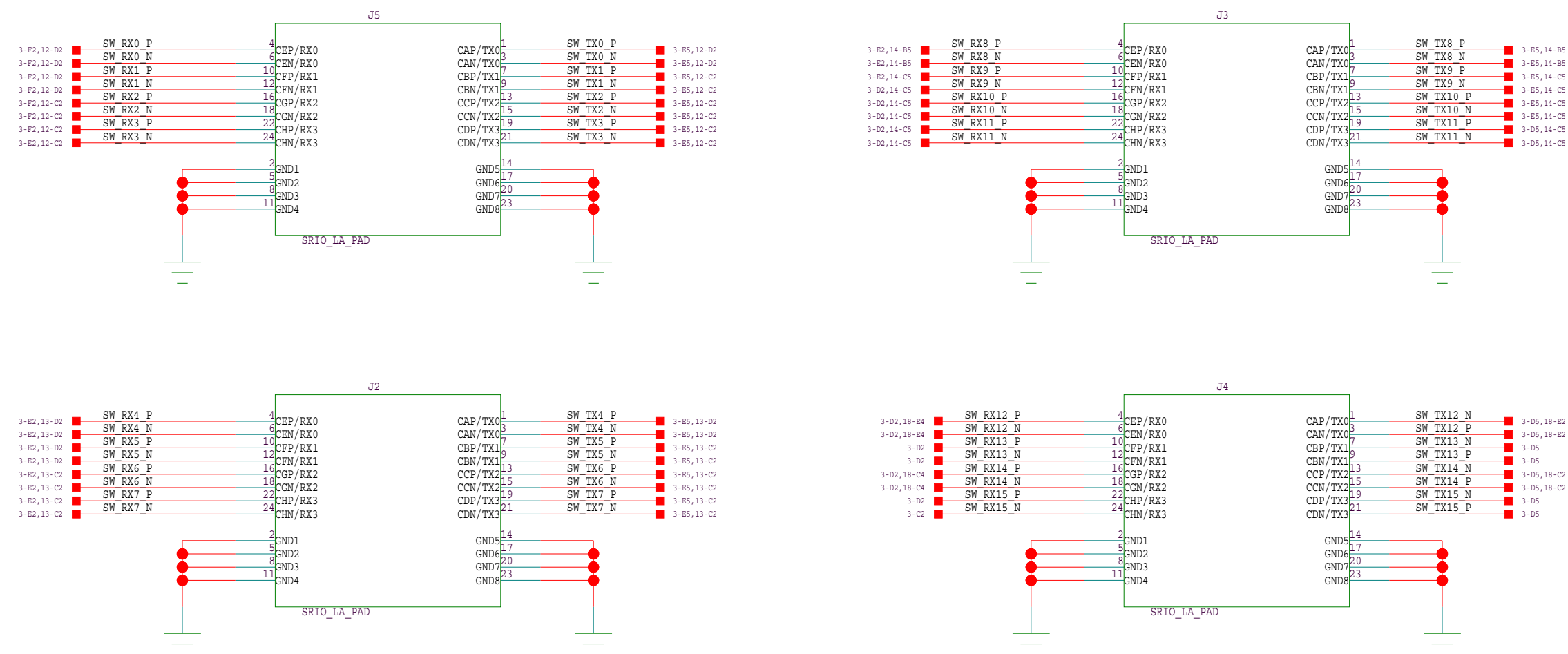


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LAST MODIFIED DATE : 7-22-2010_16:46		SHEET 2 OF 25	

80HCPS1848 Lanes 0-15

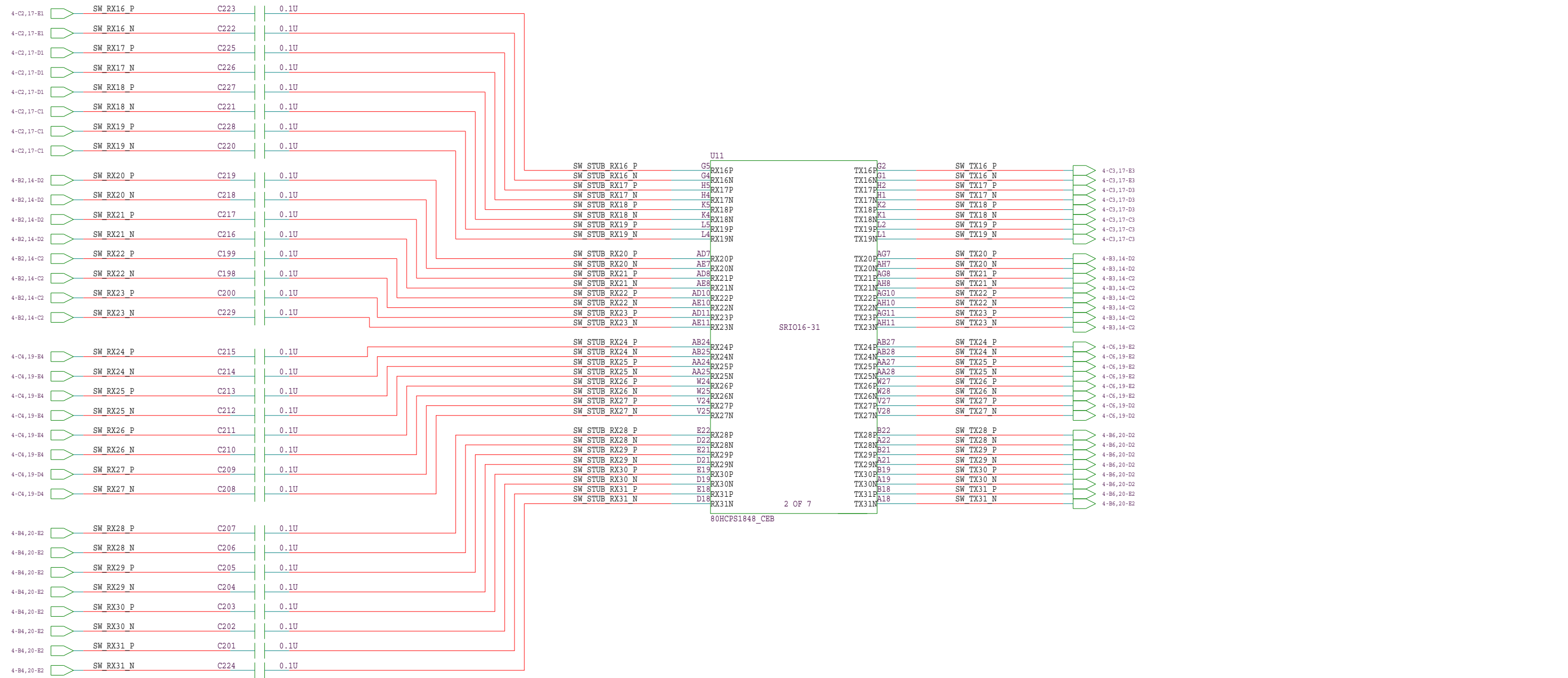


L.A. PADS

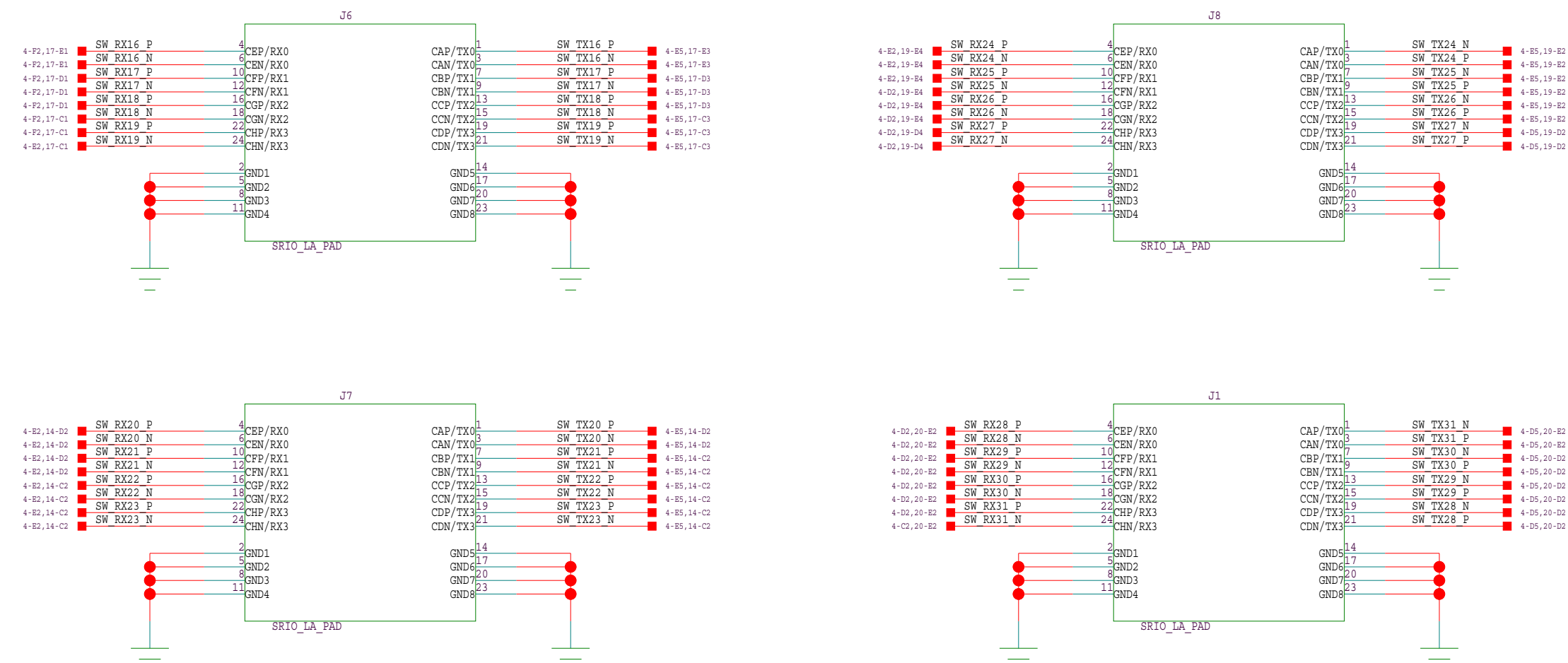


TITLE : 80HCPS1848 LANES 0-15			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			
LAST MODIFIED DATE :		SHEET	
7-22-2010_16:46		3 OF 25	

80HCPS1848 Lanes 16-31

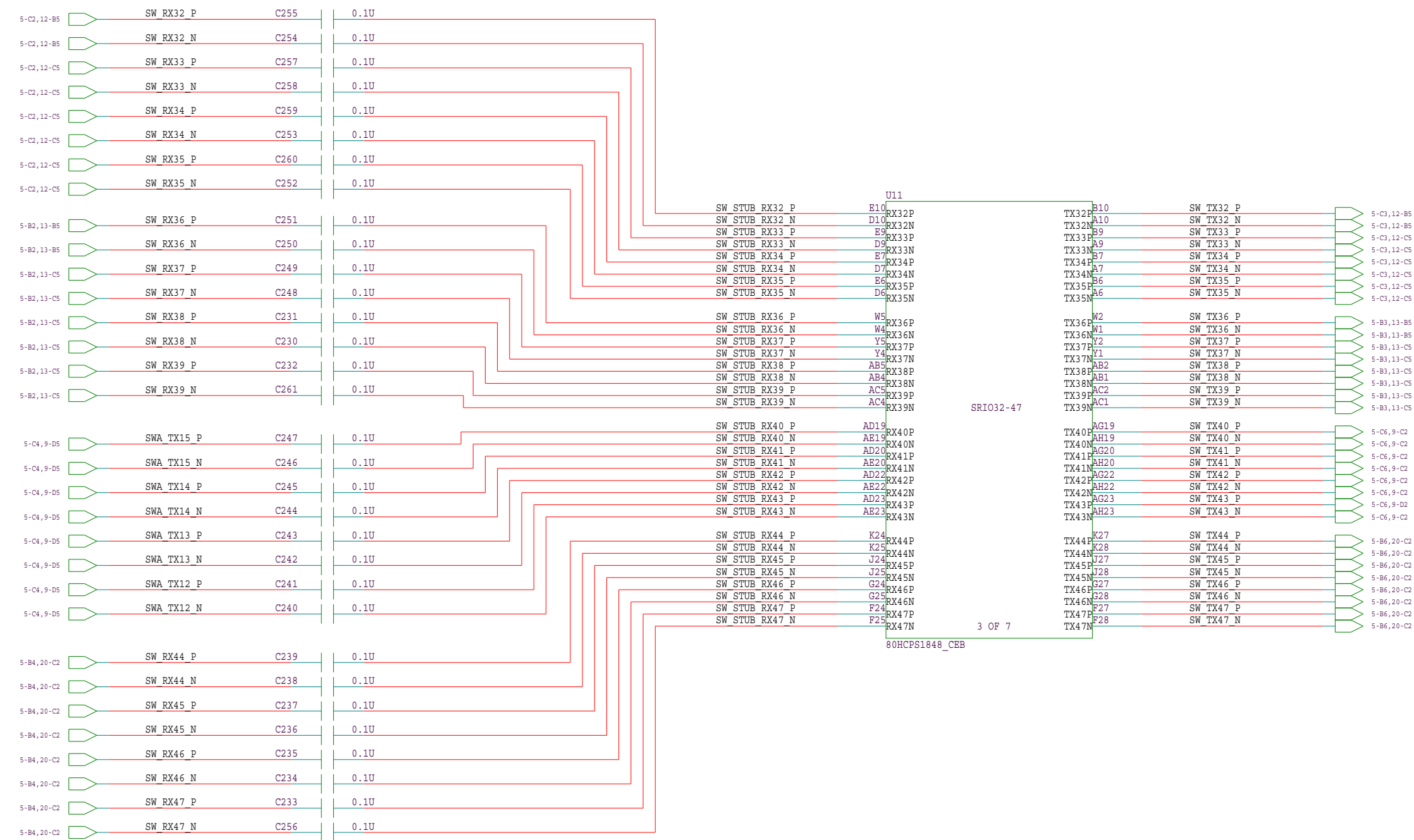


L.A. PADS

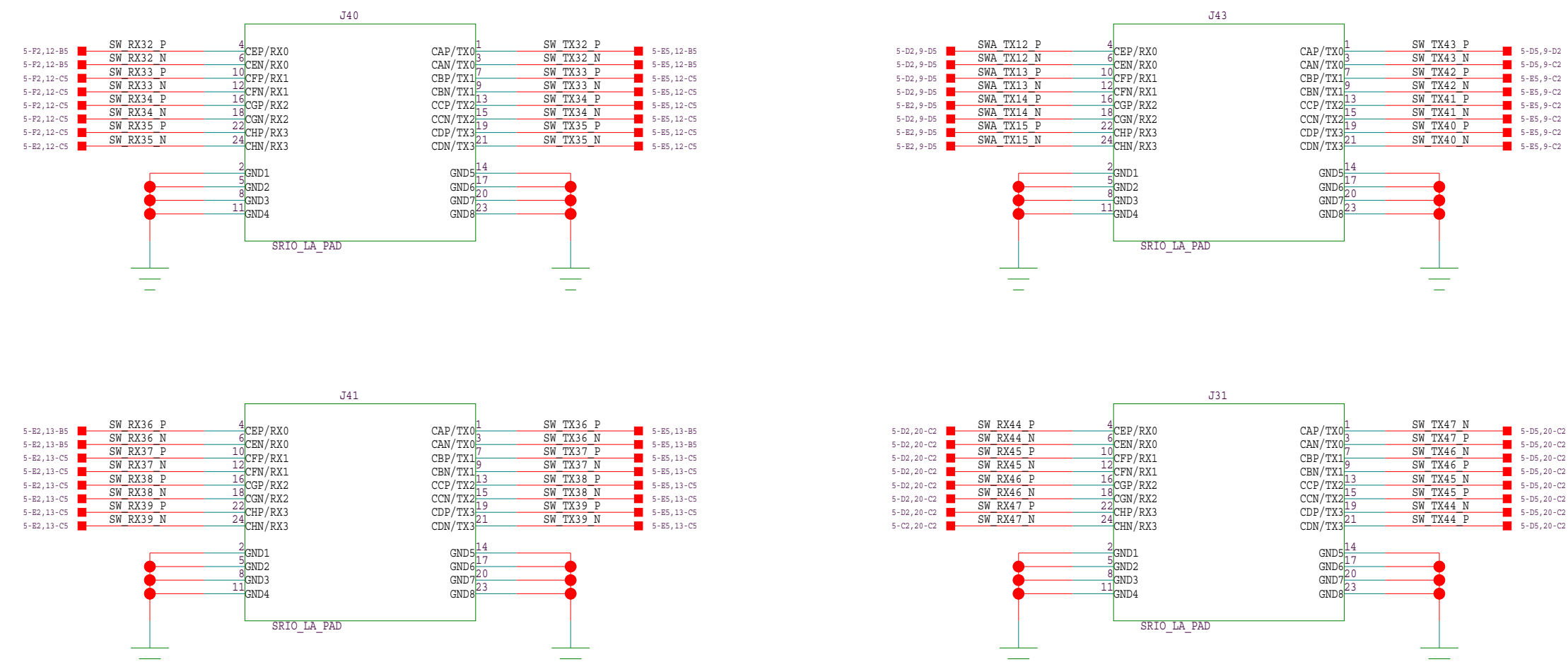


TITLE : 80HCPS1848 LANES 16-31			
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LAST MODIFIED DATE : 7-22-2010_16:46		SHEET 4 OF 25	

80HCPS1848 Lanes 32-47

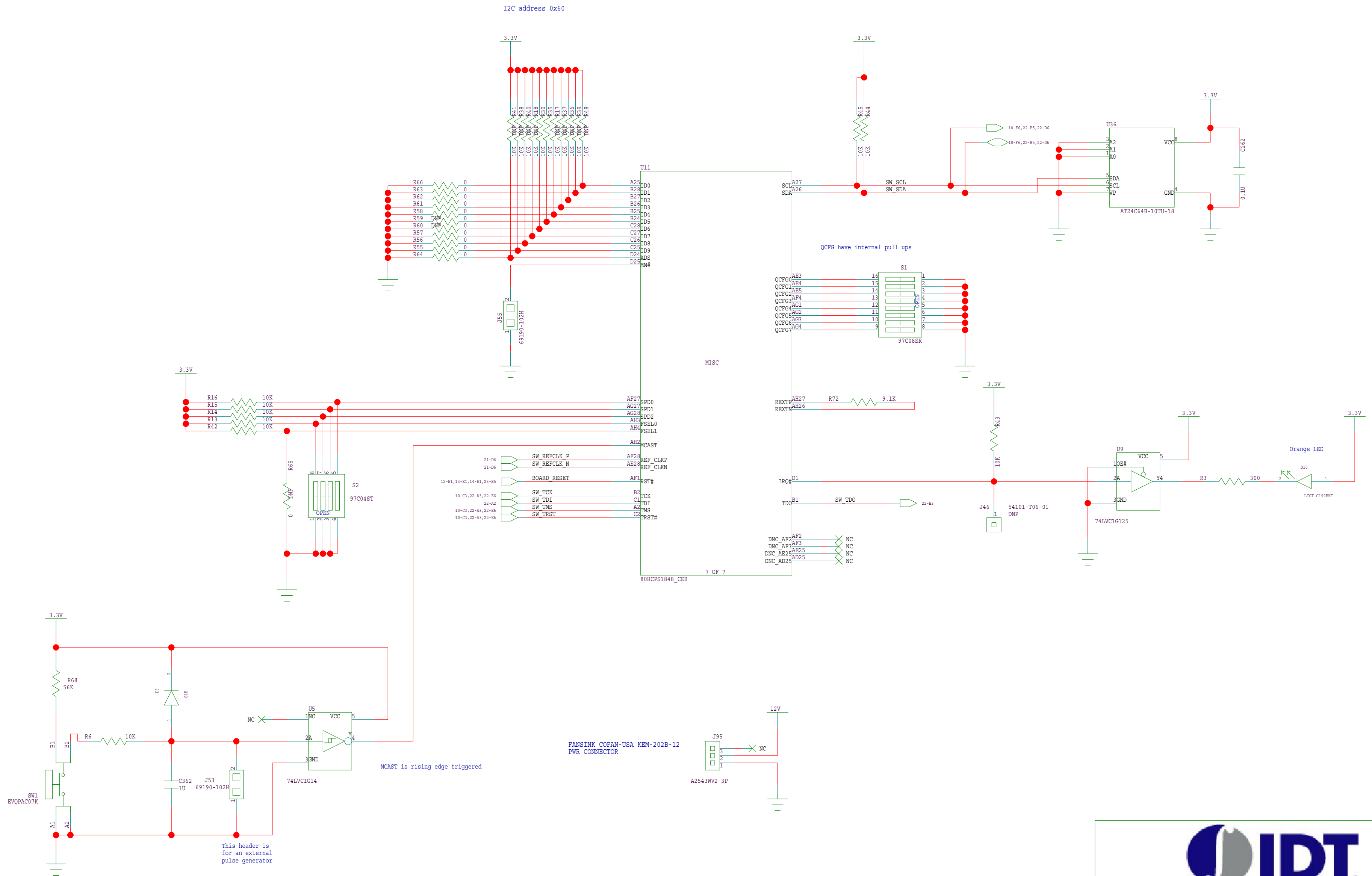


L.A. PADS



TITLE : 80HCPS1848 LANES 32-47			
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80HCPS1848 Config

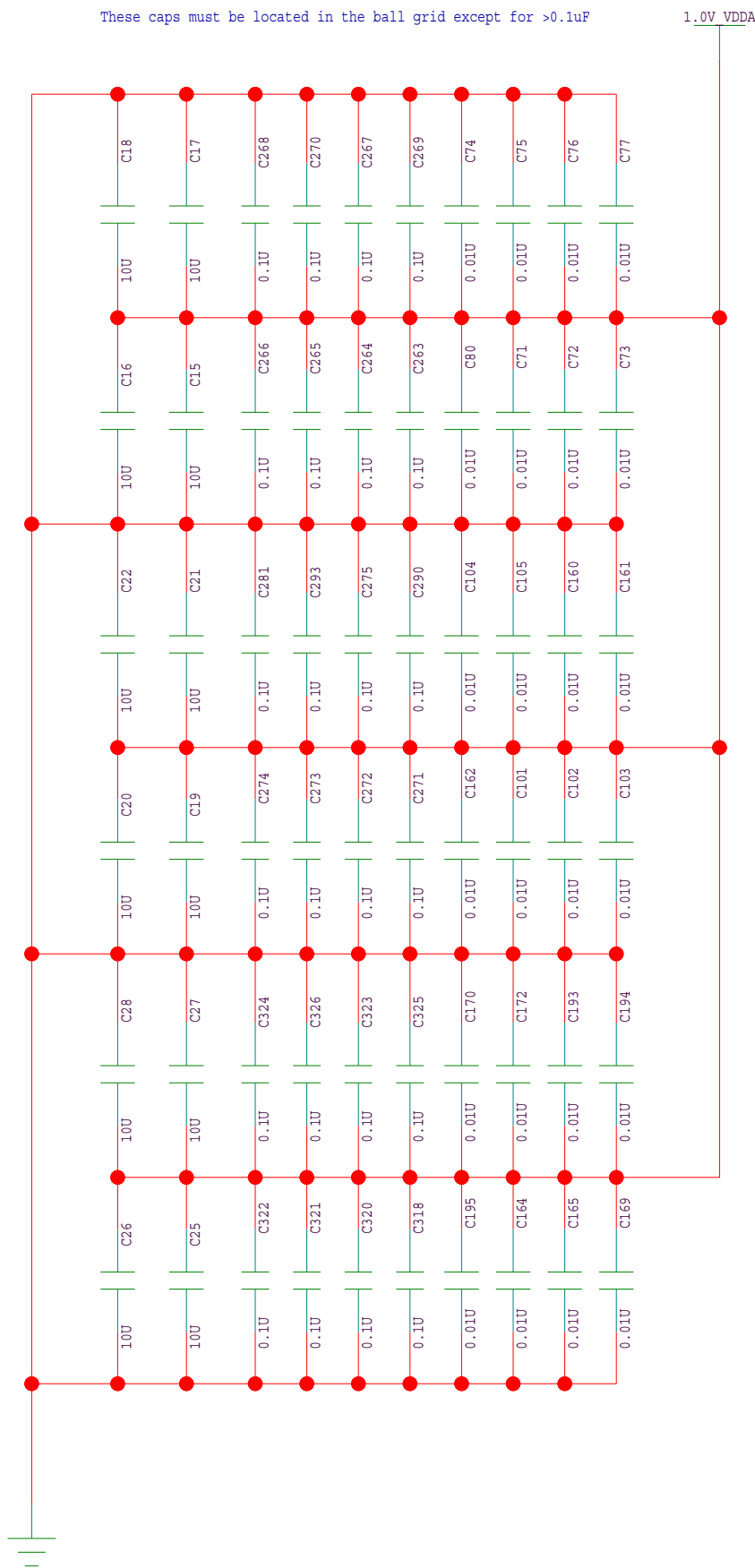


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SIZE : C	DRAWING NUMBER :	Version :	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:46		SHEET 6 OF 25	

80HCPS1848 Power and Decoupling

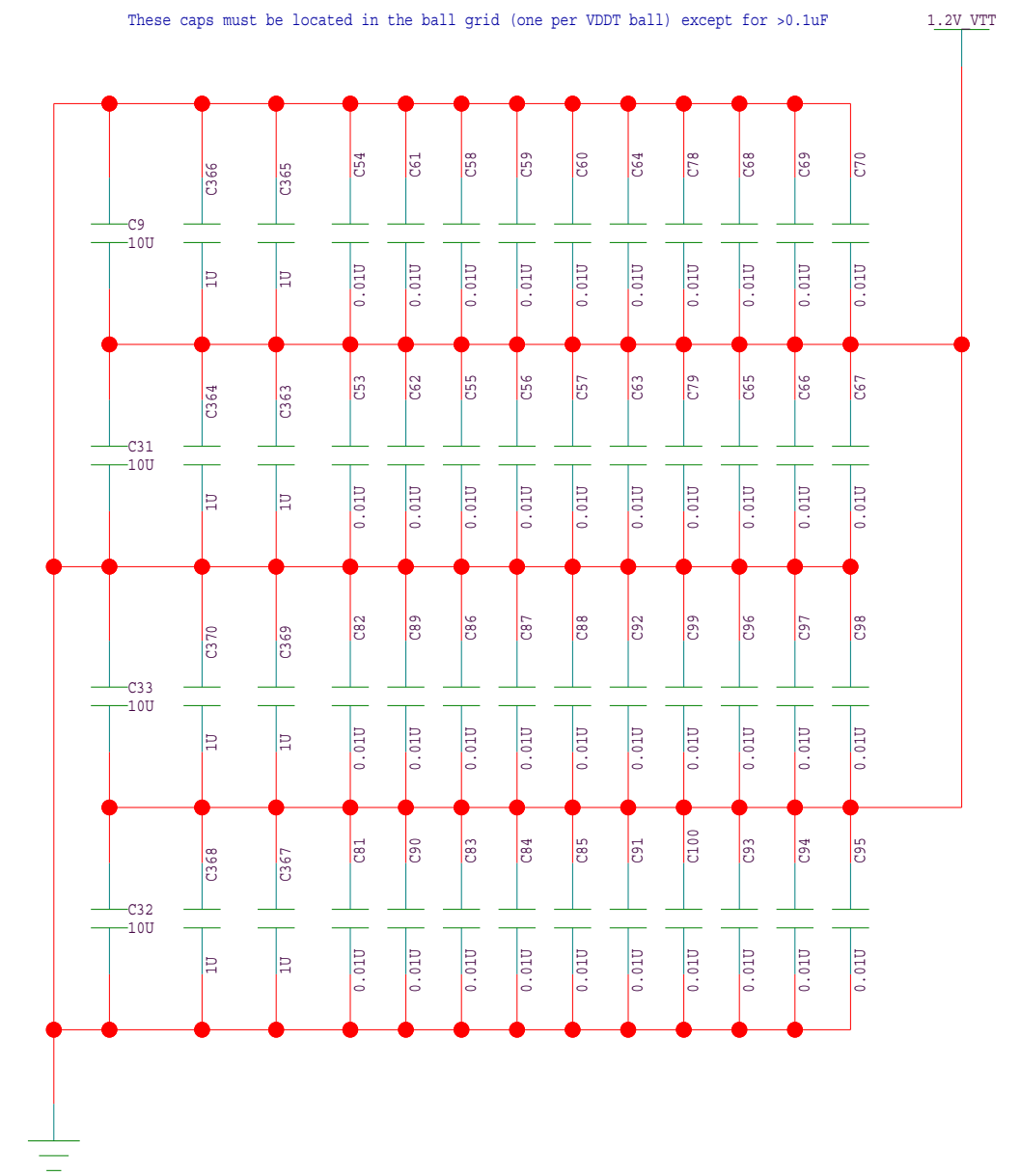
Decoupling 1.0V_VDDA

These caps must be located in the ball grid except for >0.1uF



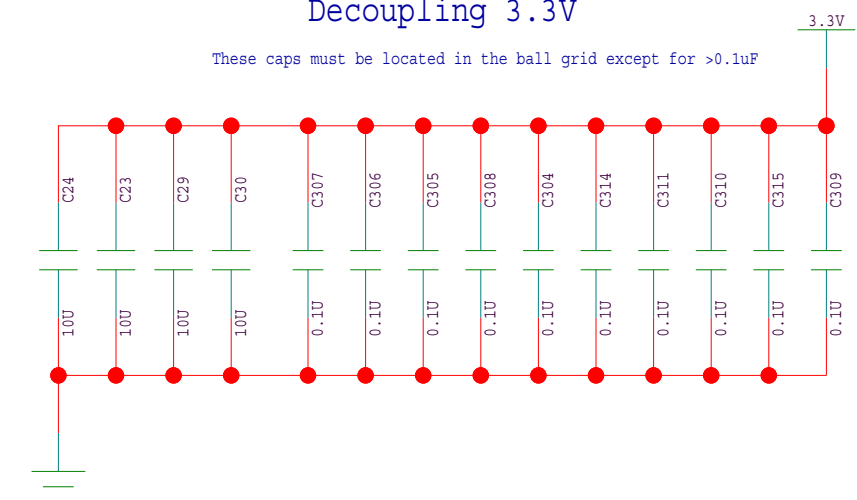
Decoupling 1.2V_VDDT

These caps must be located in the ball grid (one per VDDT ball) except for >0.1uF



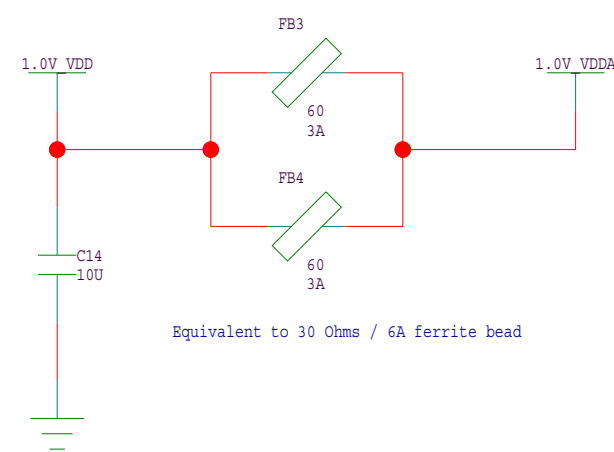
Decoupling 3.3V

These caps must be located in the ball grid except for >0.1uF

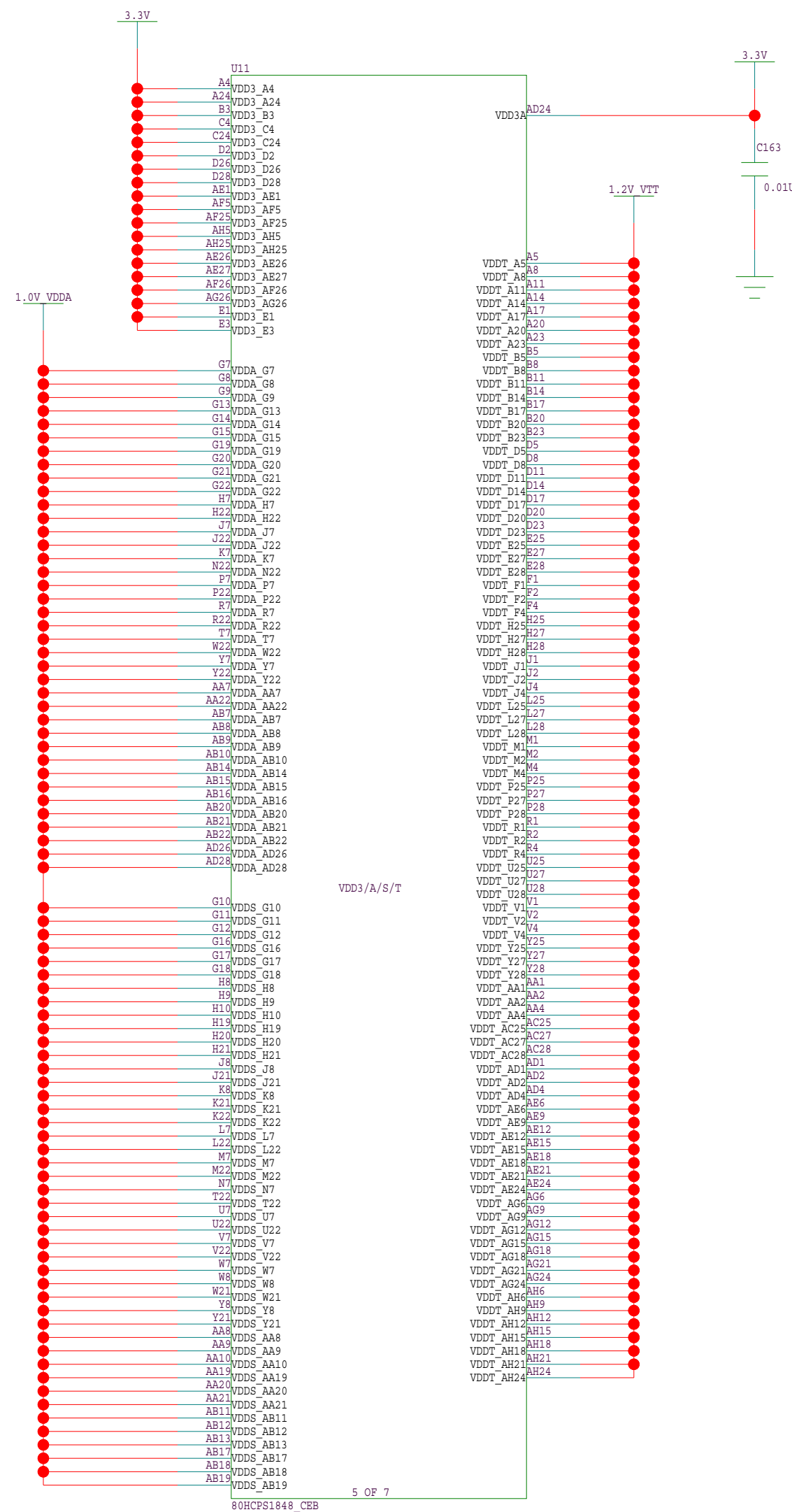


Board layout note:

Make two separate power planes: 1.0V_VDD and 1.0V_VDDA



Equivalent to 30 Ohms / 6A ferrite bead



TITLE : 80HCPS1848 POWER AND DECOUPLING

SIZE DRAWING NUMBER : Version: DESIGNER :

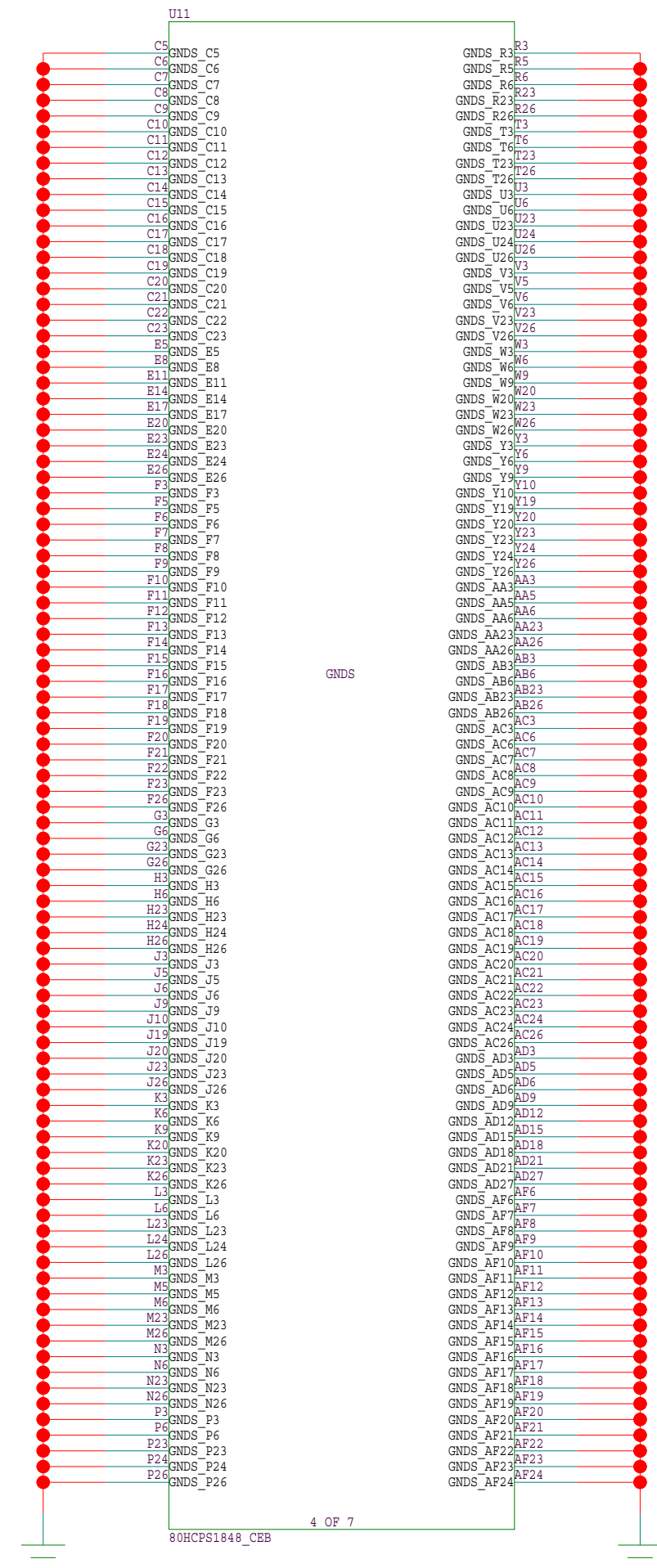
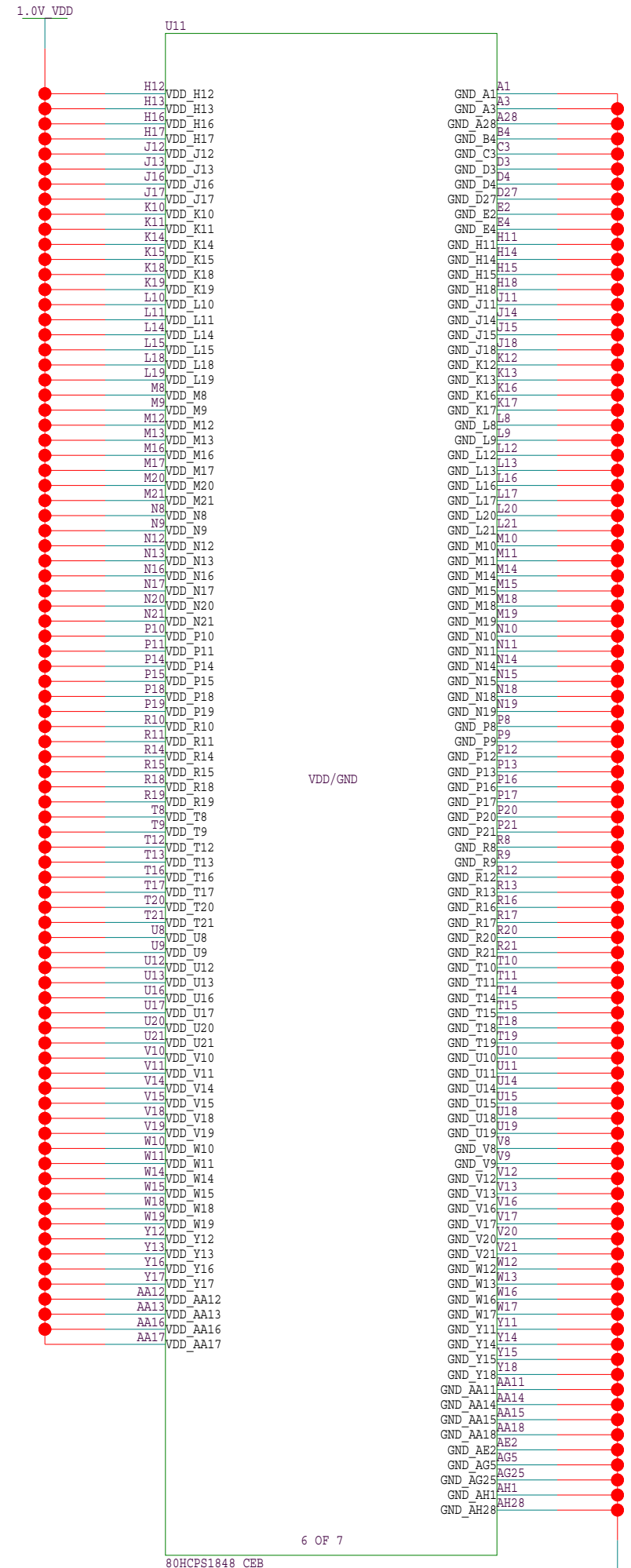
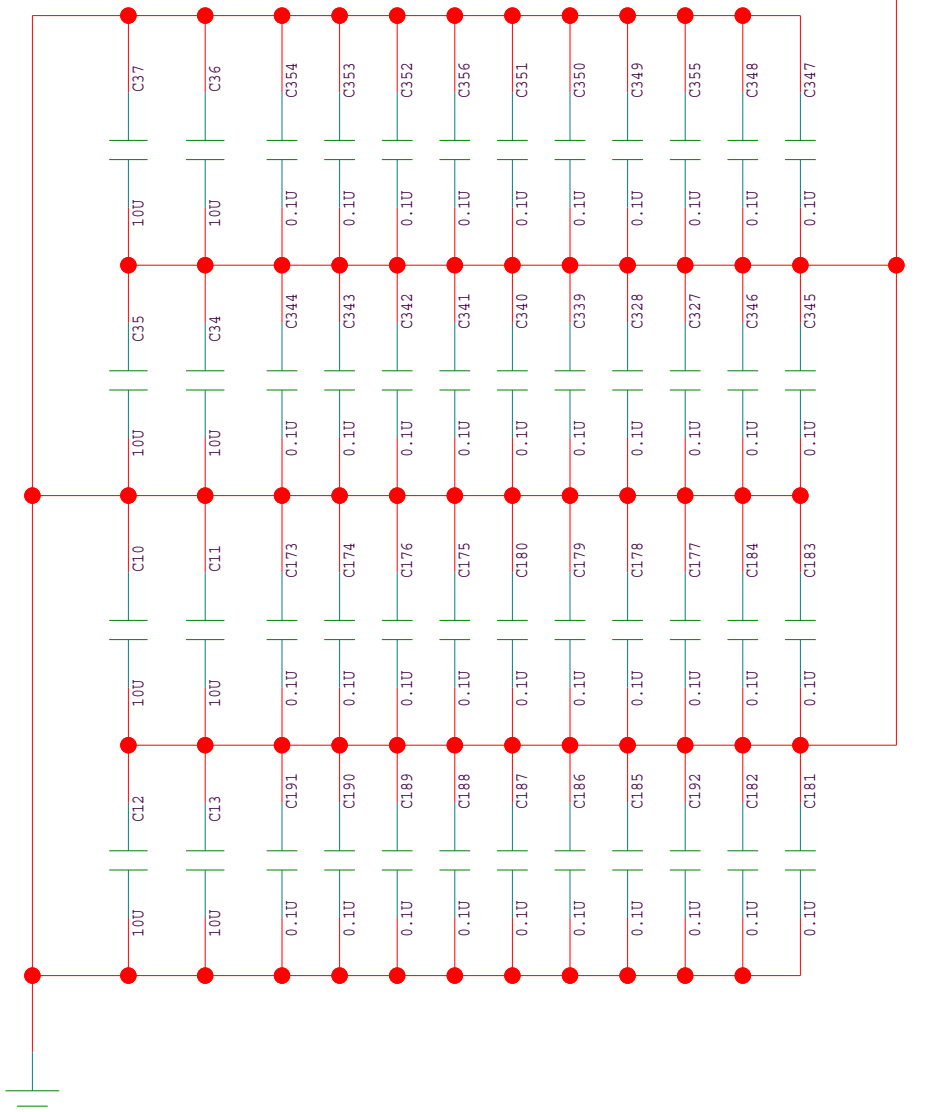

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80HCPS1848 Power and Ground

Decoupling 1.0V_VDD

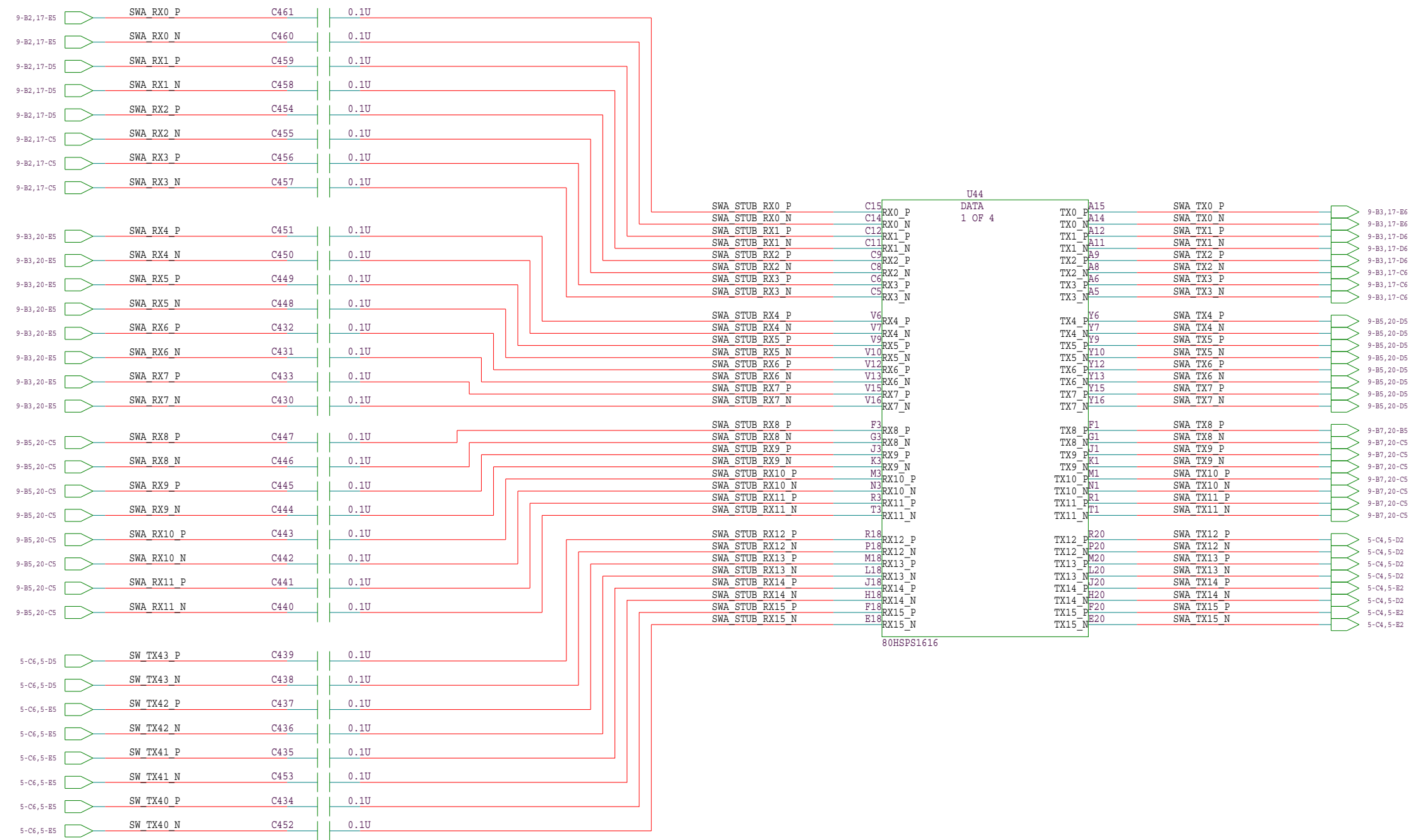
Bulk decoupling is on the regulator page
Most of these caps must be located in the ball grid

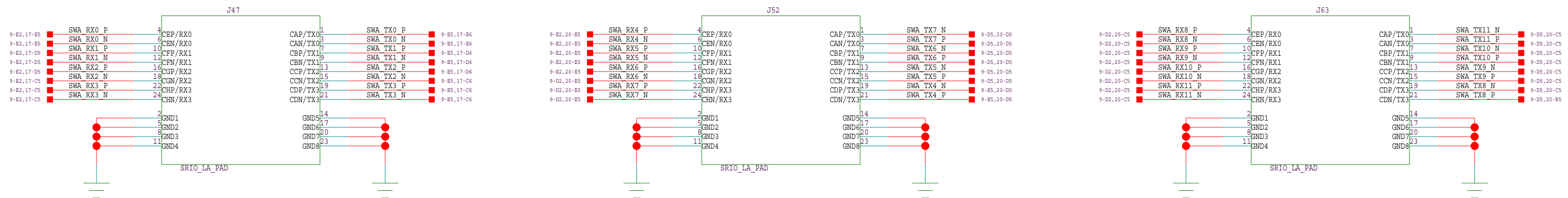
TITLE : 80HCPS1848 POWER AND GROUND

SIZE : C	DRAWING NUMBER :	Version :	DESIGNER :
LAST MODIFIED DATE : 7-22-2010, 16:46		SHEET 8 OF 25	

80HSPS1616 Ports

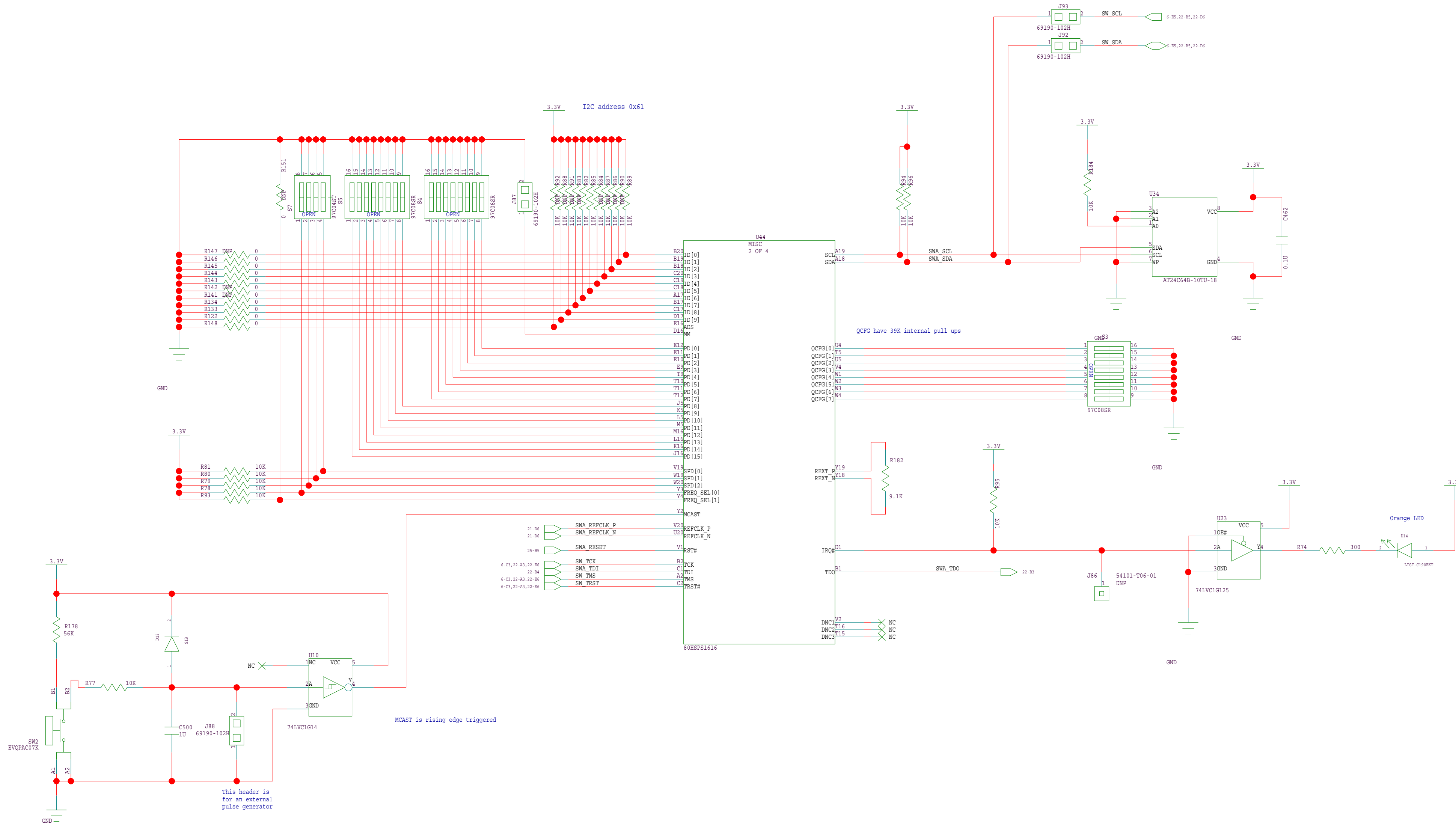


L.A. PADS



TITLE : 80HSPS1616 PORTS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			
LAST MODIFIED DATE : 7-22-2010_16:46		SHEET 9 OF 25	

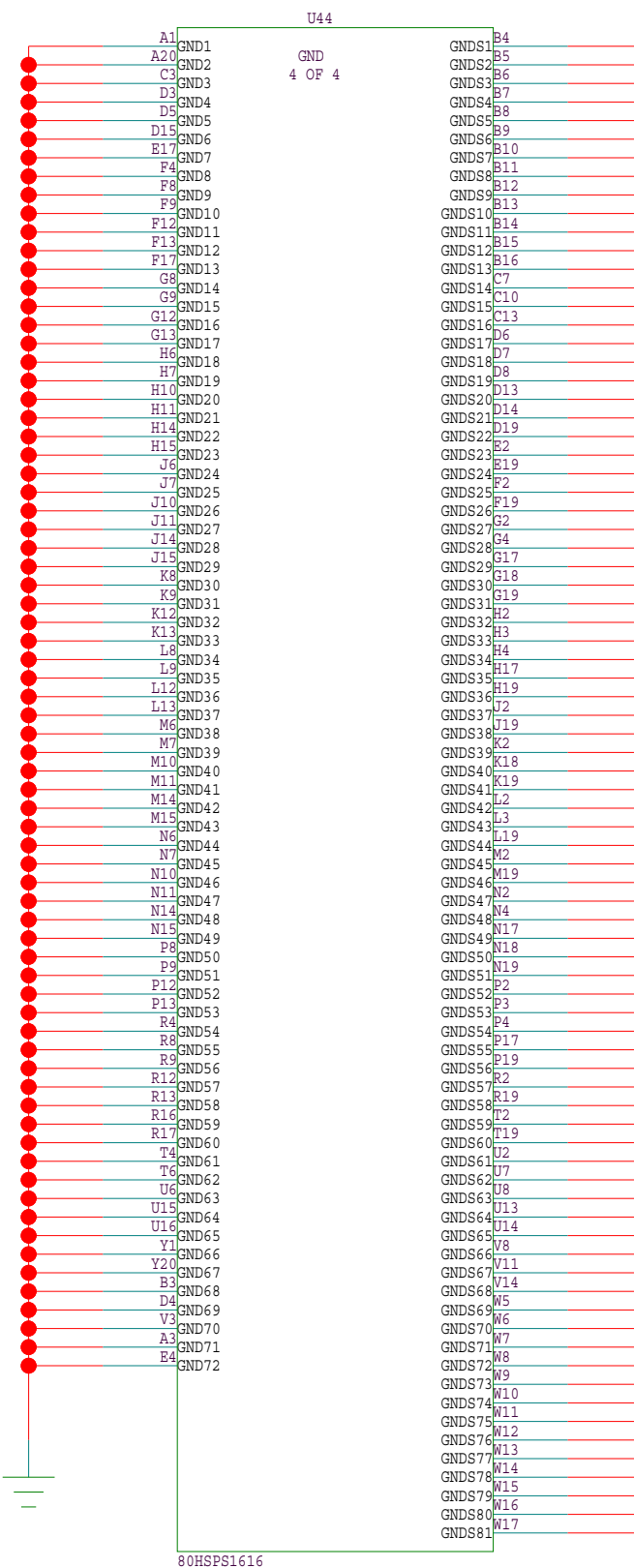
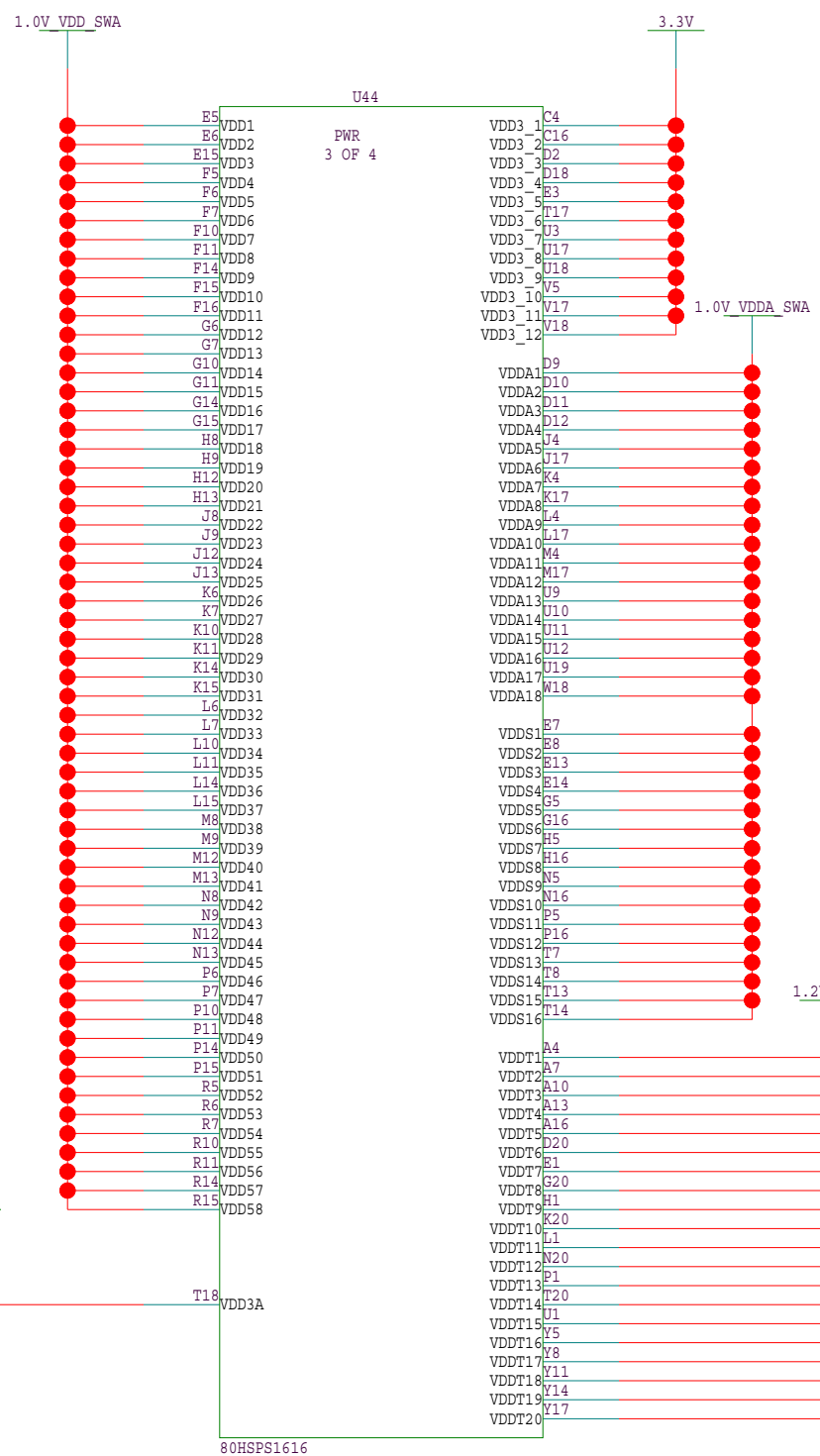
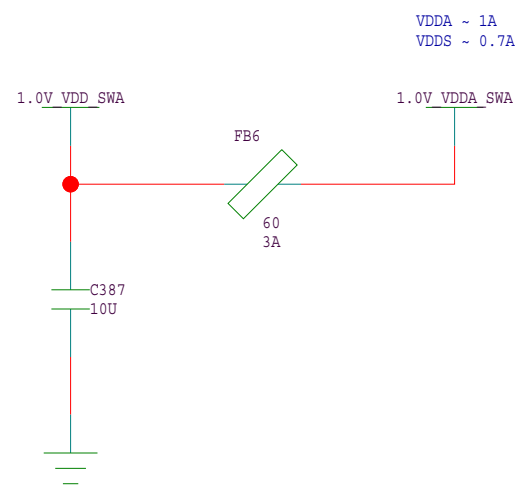
80HSPS1616 Config



TITLE : 80HSPS1616 CONFIG			
SIZE : C	DRAWING NUMBER :	Version :	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:46		SHEET 10 OF 25	

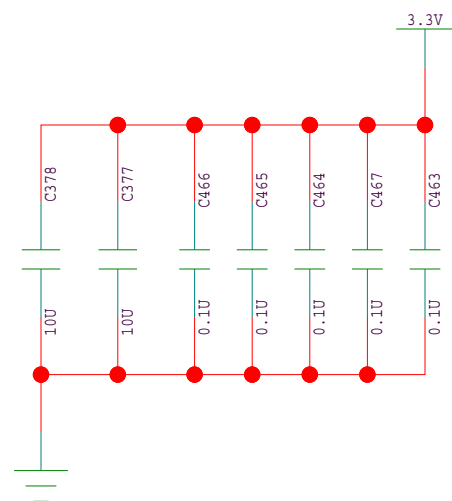
80HSPS1616 Power

Board layout note:
Make two separate power planes: 1.0V_VDD and 1.0V_VDDA



Decoupling 3.3V

These caps must be located in the ball grid except for >0.1uF



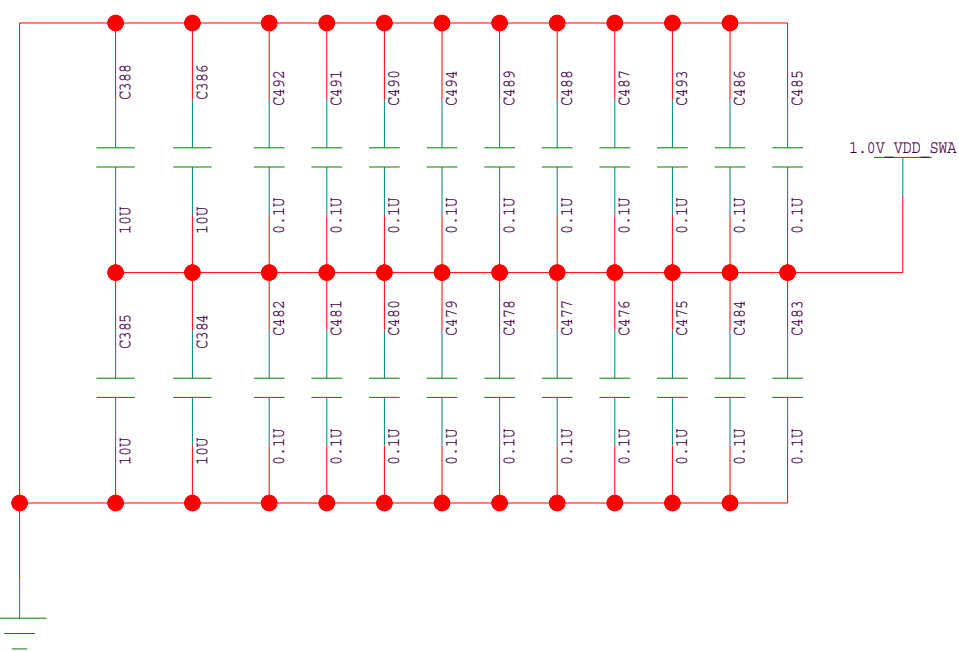
This caps must be located in the ball grid at T18



Decoupling 1.0V_VDD

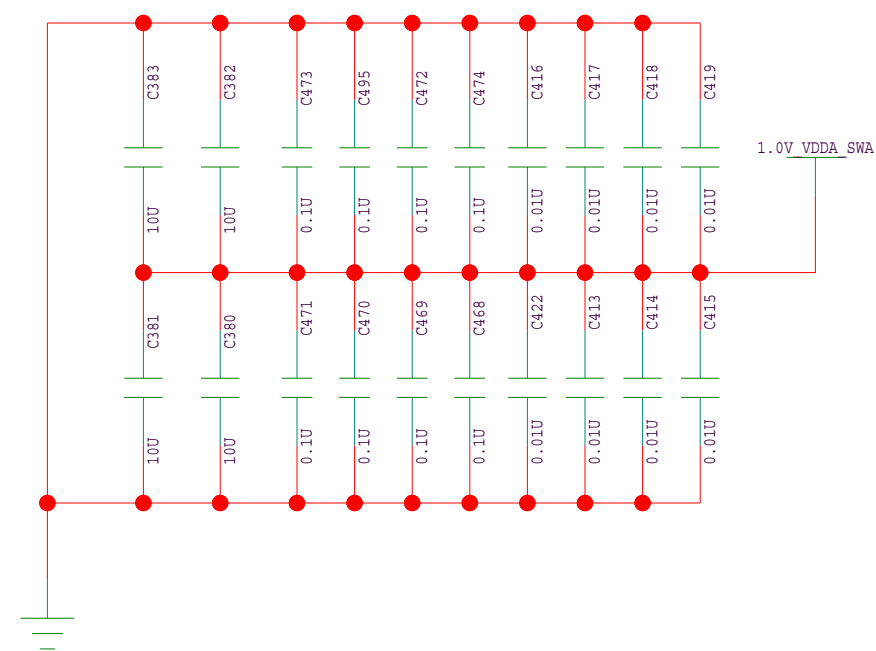
Bulk decoupling is on the regulator page

Most of these caps must be located in the ball grid



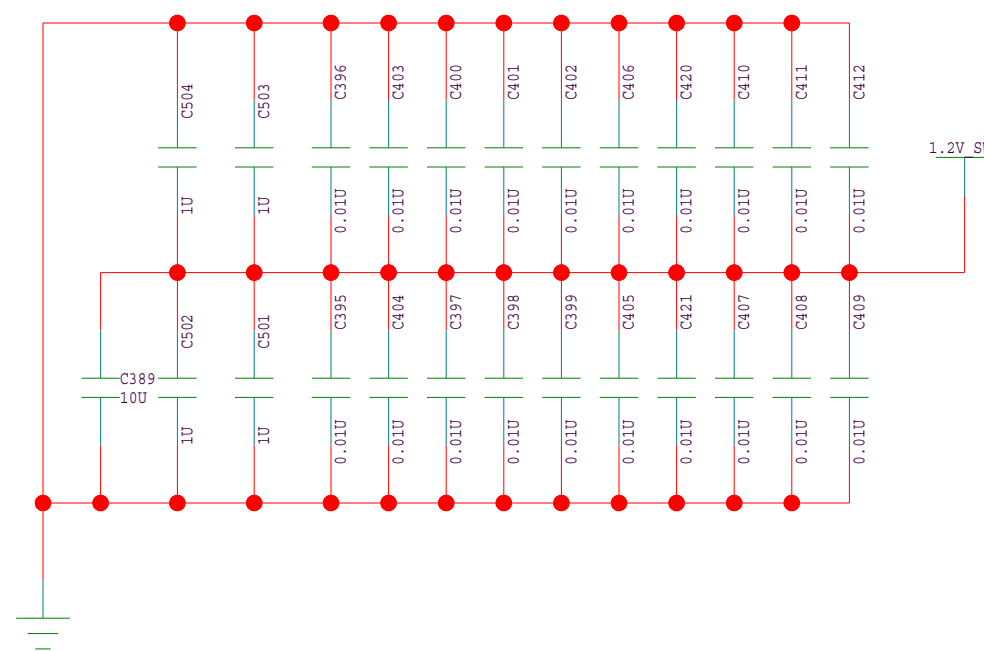
Decoupling 1.0V_VDDA

These caps must be located in the ball grid except for >0.1uF



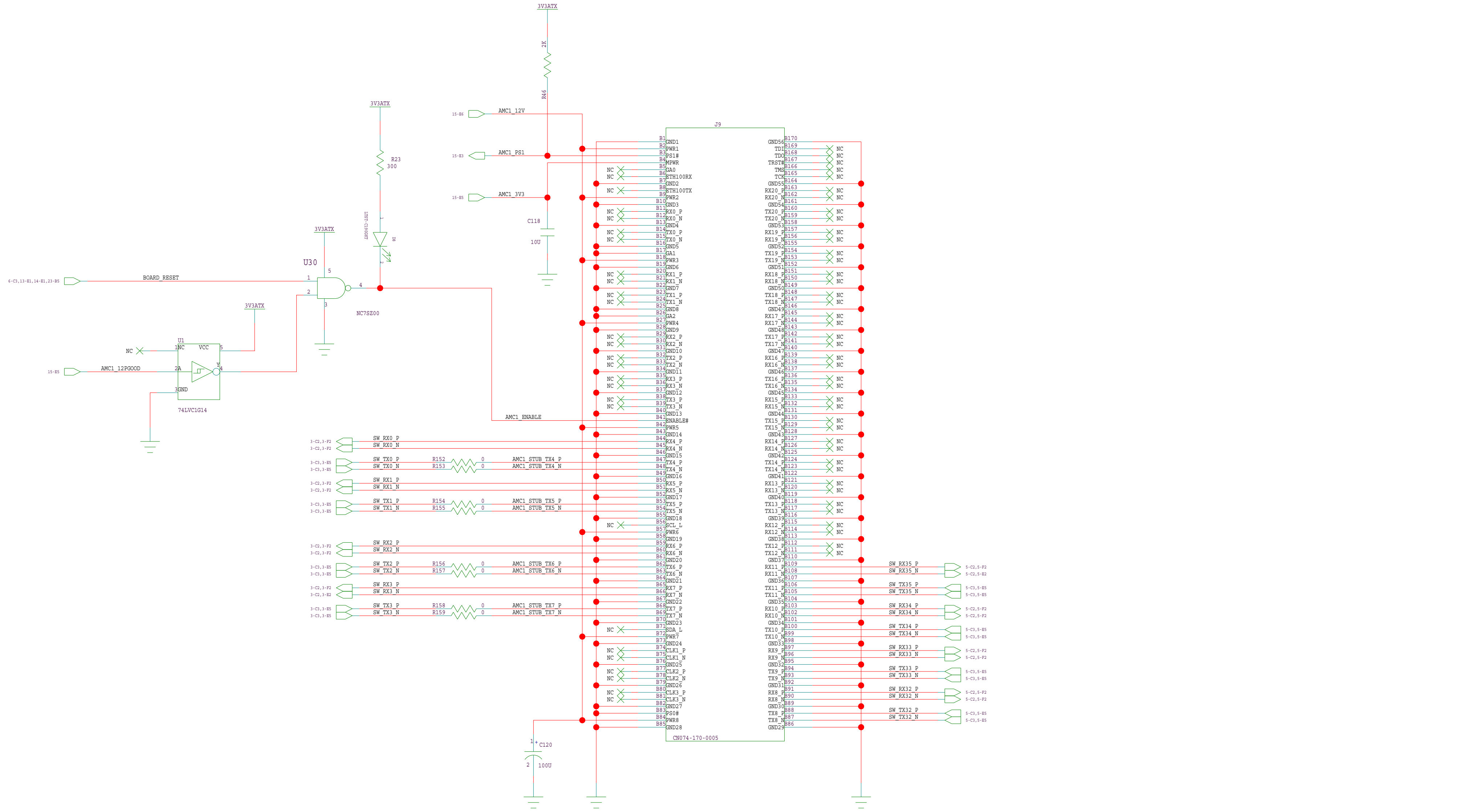
Decoupling 1.2V_VDDT

These caps must be located in the ball grid (one per VDDT ball) except for >0.1uF



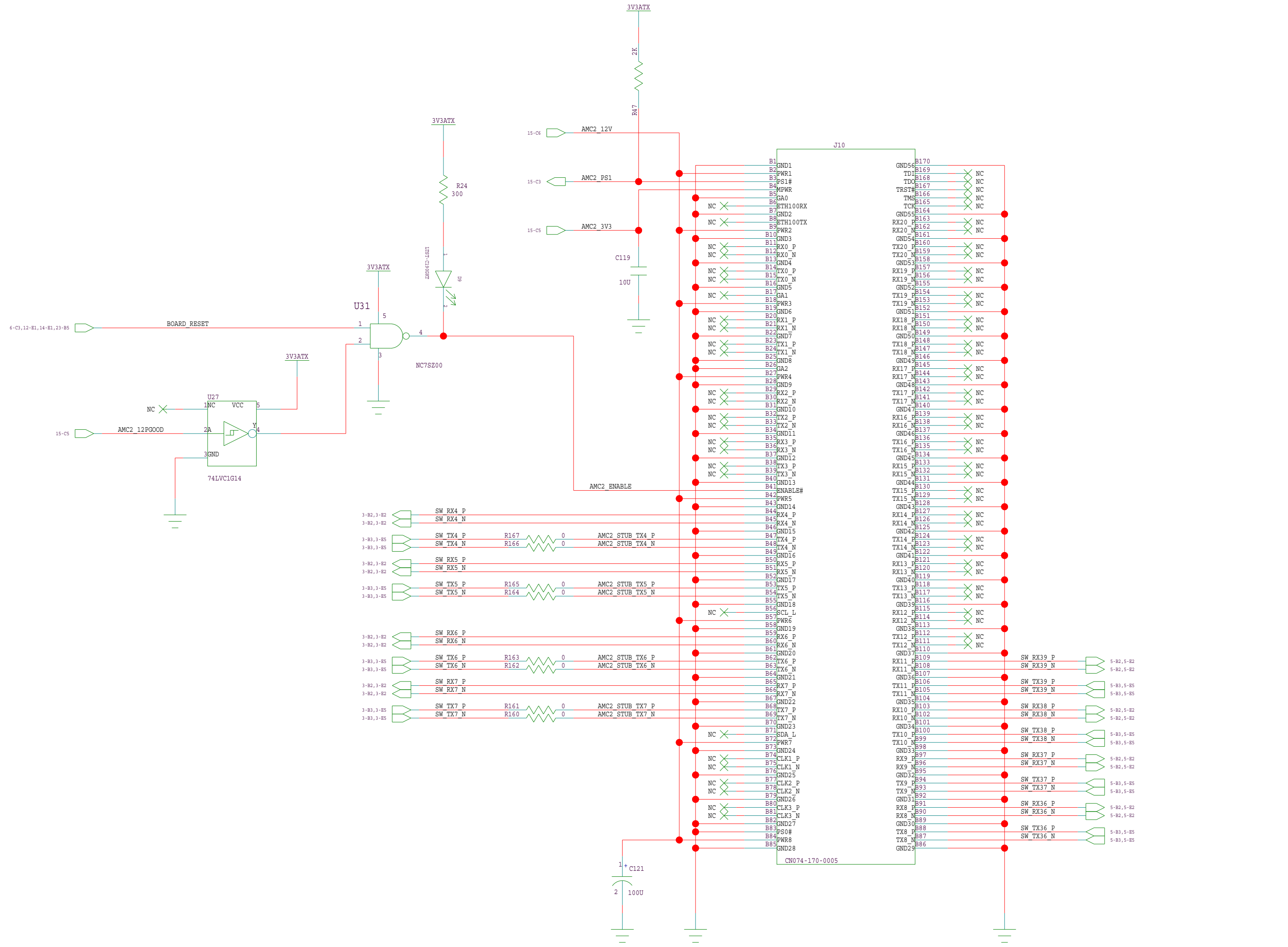
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SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			
LAST MODIFIED DATE : 7-22-2010_16:45		SHEET 11 OF 25	


AMC-1 Connector



TITLE : AMC-1 CONNECTOR			
SIZE : C	DRAWING NUMBER :	Version :	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:45		SHEET 12 OF 25	

AMC-2 Connector



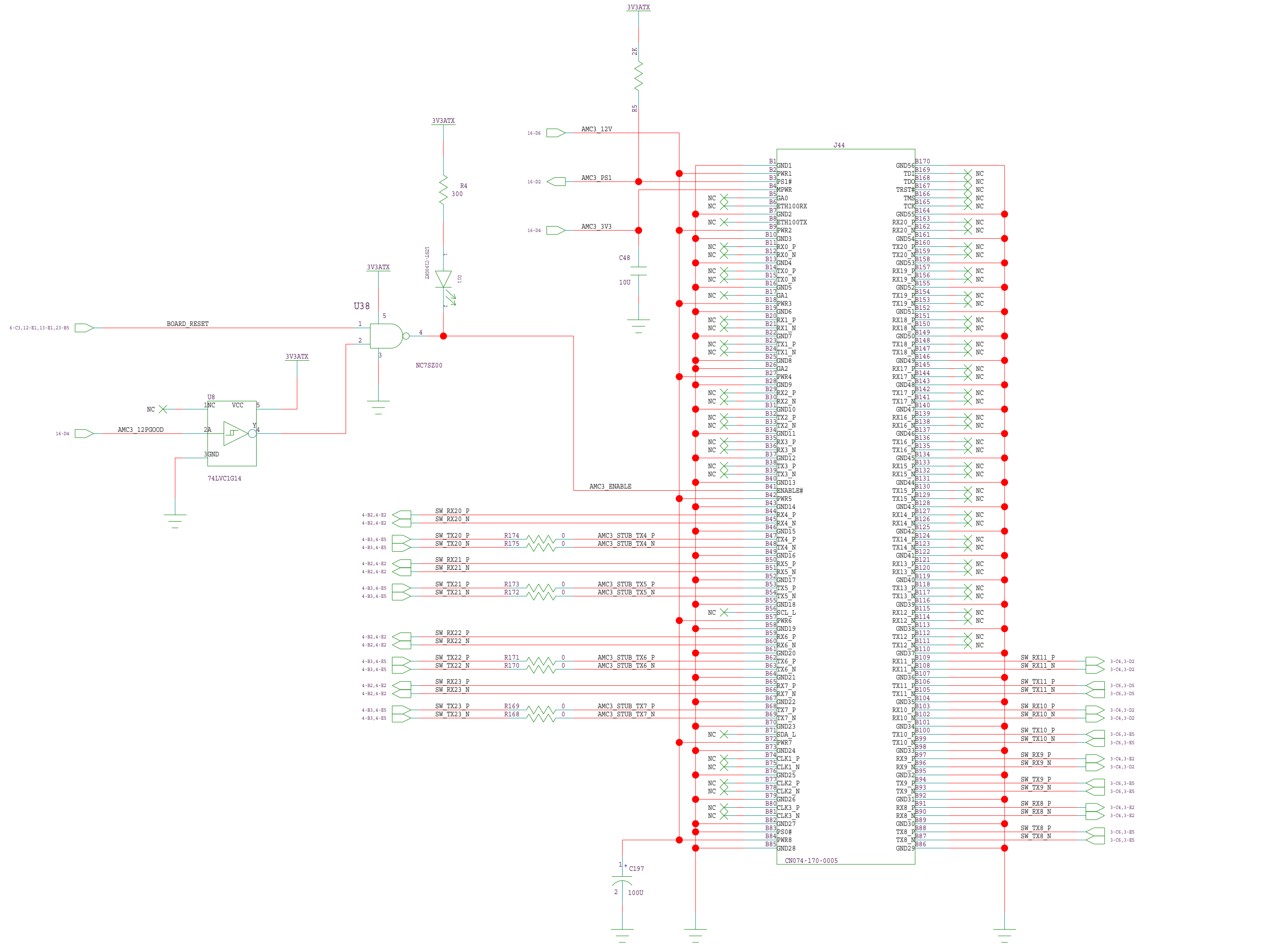



IDT

TITLE : AMC-2 CONNECTOR

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			
LAST MODIFIED DATE :		SHEET	
7-22-2010_16:45		13 OF 25	

AMC-3 Connector



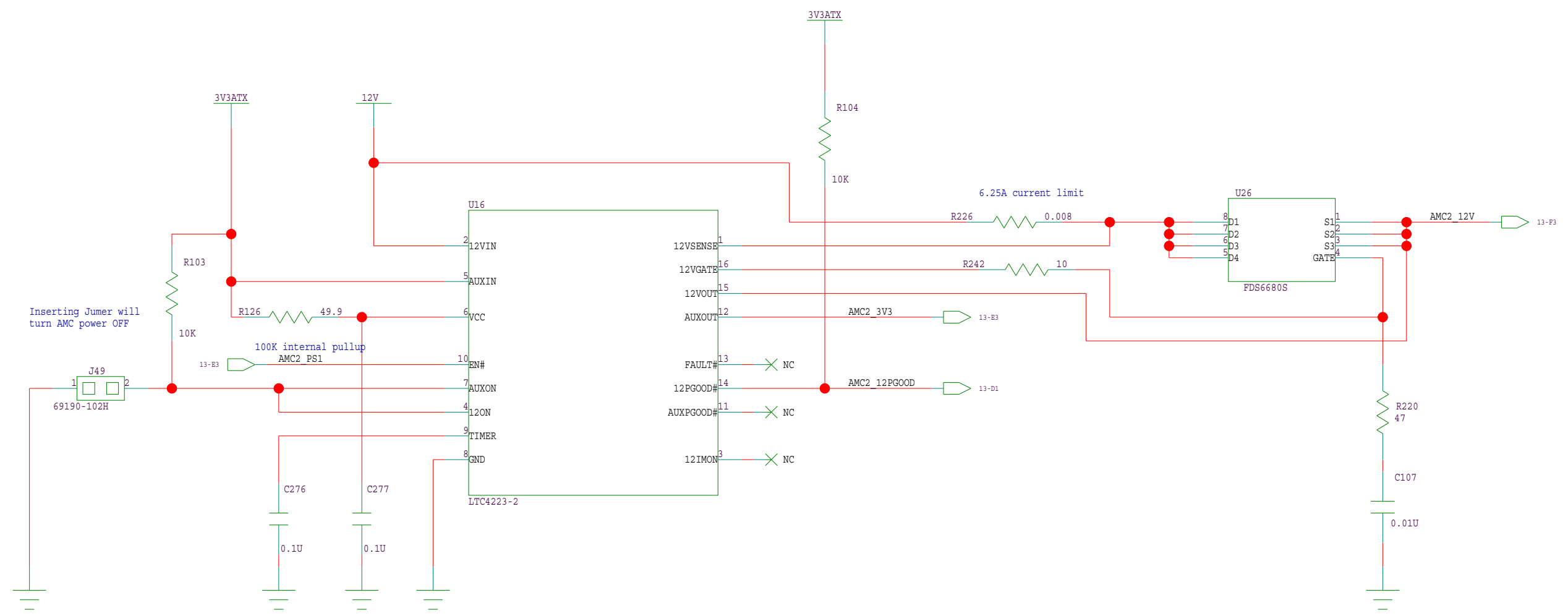
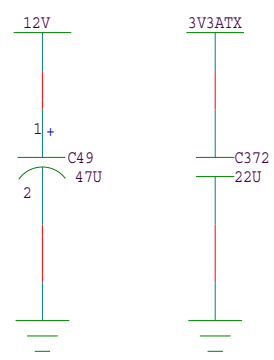
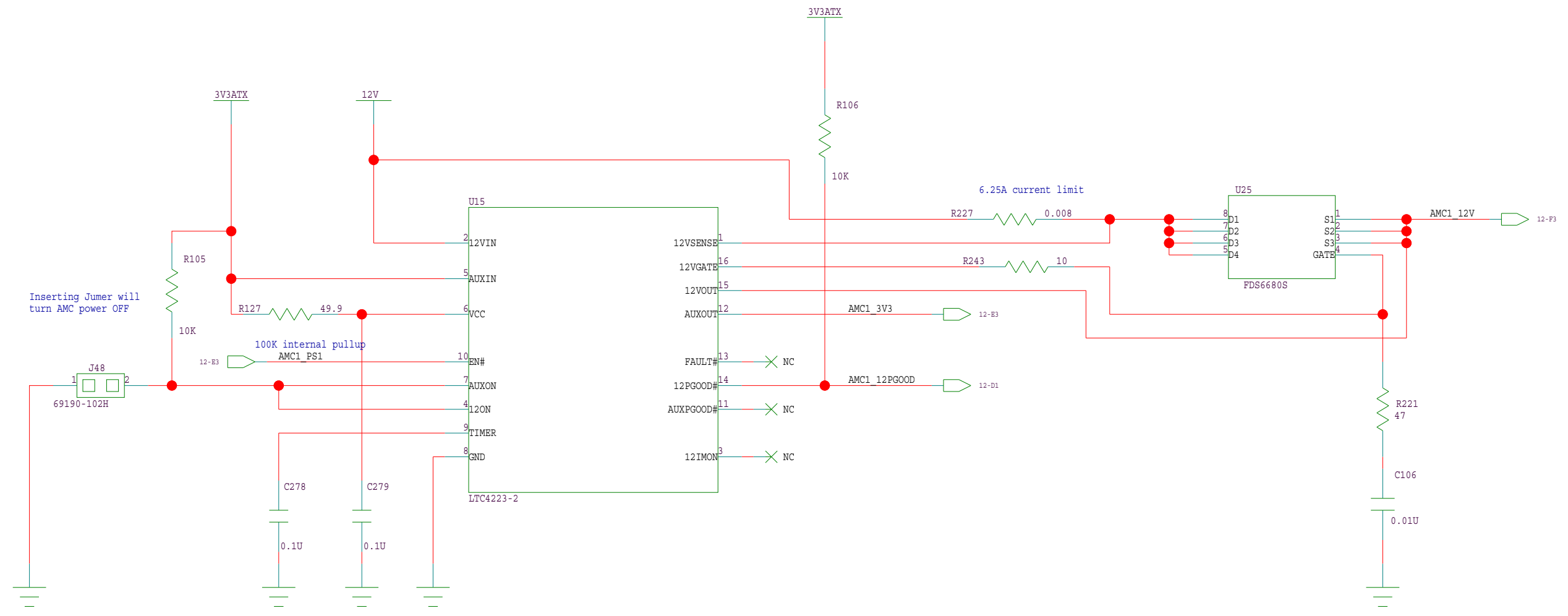
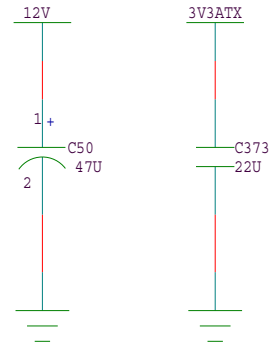


IDT

TITLE : AMC-3 CONNECTOR

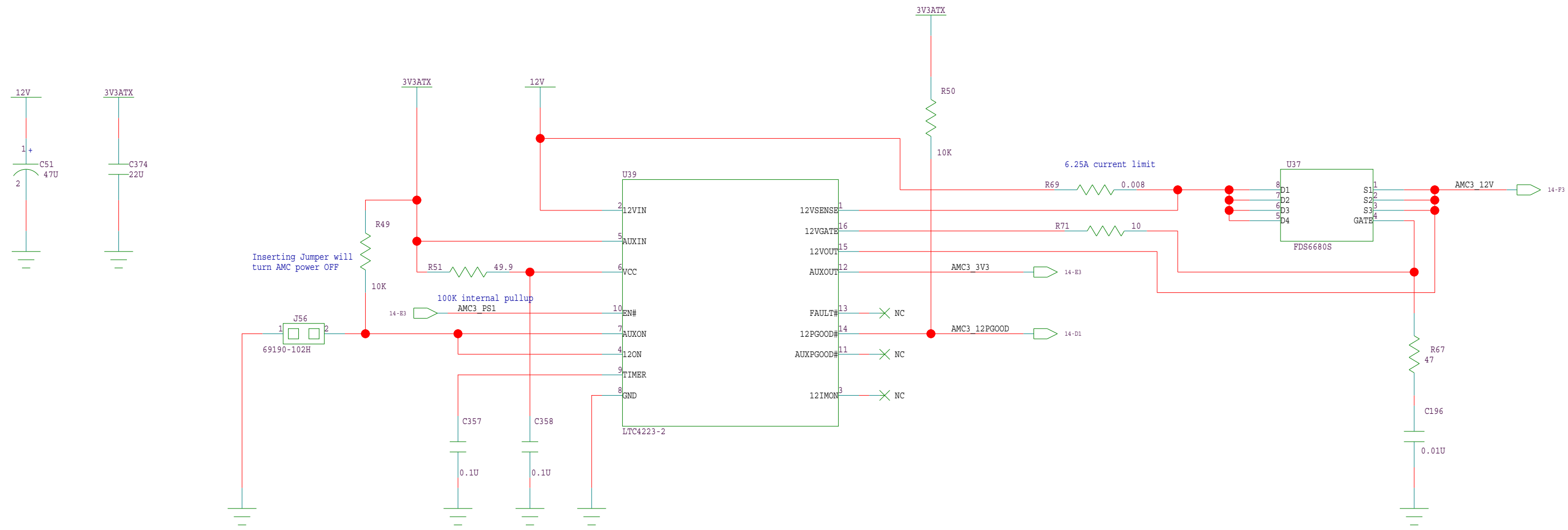
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C			
LAST MODIFIED DATE :		SHEET	
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AMC 1 & 2 Hotswap Controllers



TITLE : AMC 1 & 2 HOTSWAP CONTROLLERS			
SIZE : C	DRAWING NUMBER :	Version :	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:45			SHEET 15 OF 25

AMC 3 Hotswap Controller



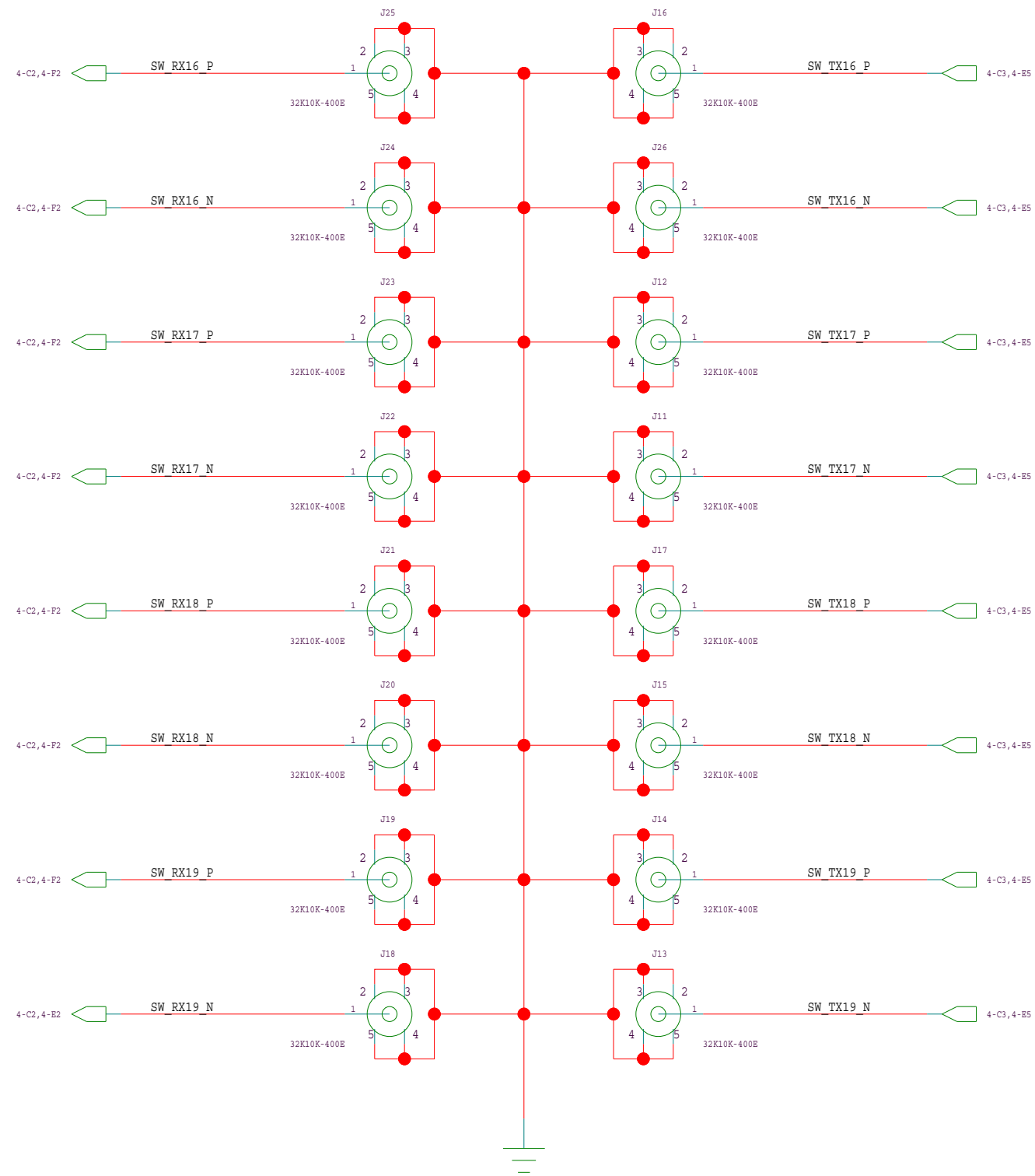
TITLE : AMC 3 HOTSWAP CONTROLLER

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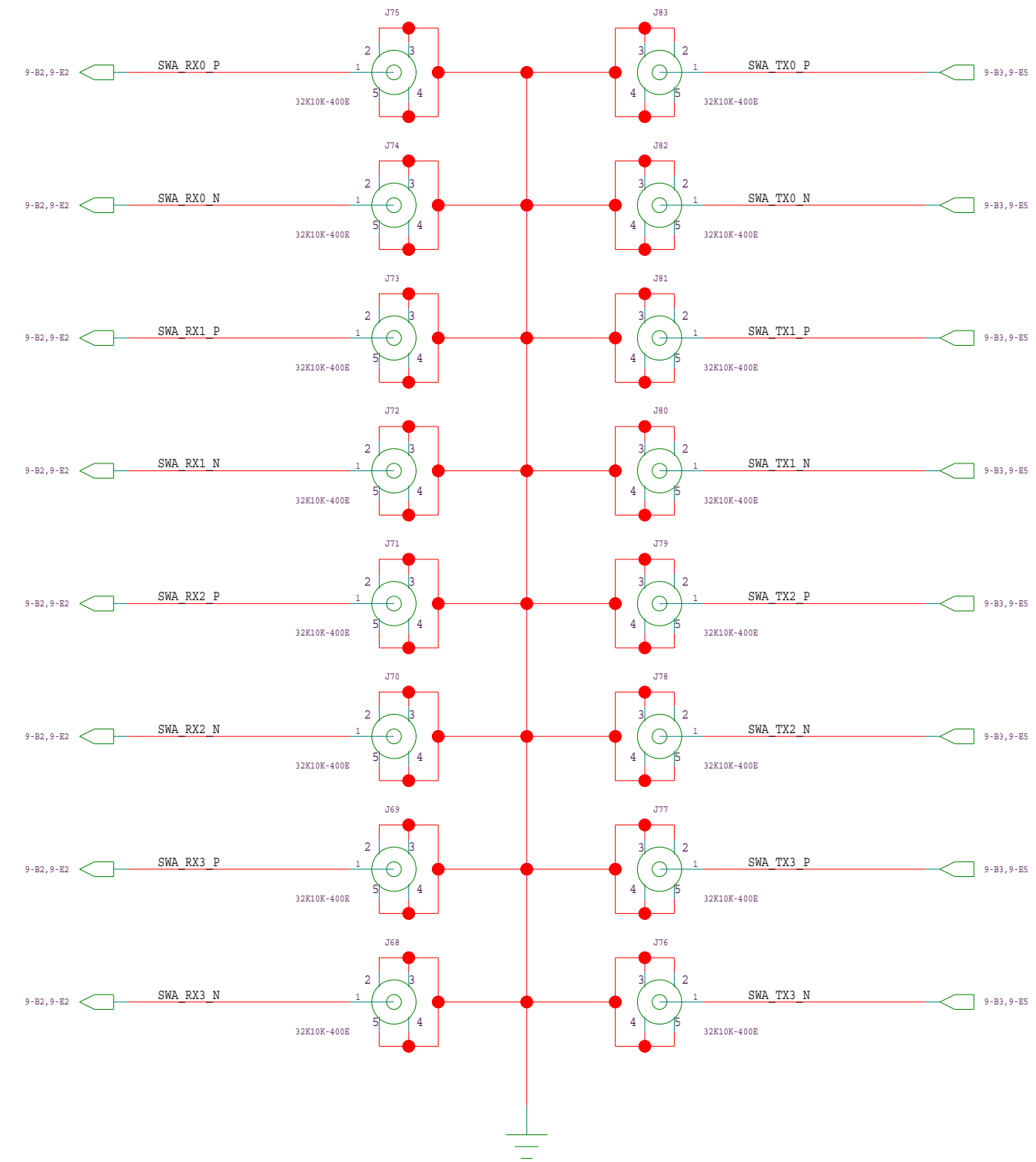
LAST MODIFIED DATE : 7-22-2010_16:45 SHEET 16 OF 25

SMA Field

80HCPS1848 SMAs

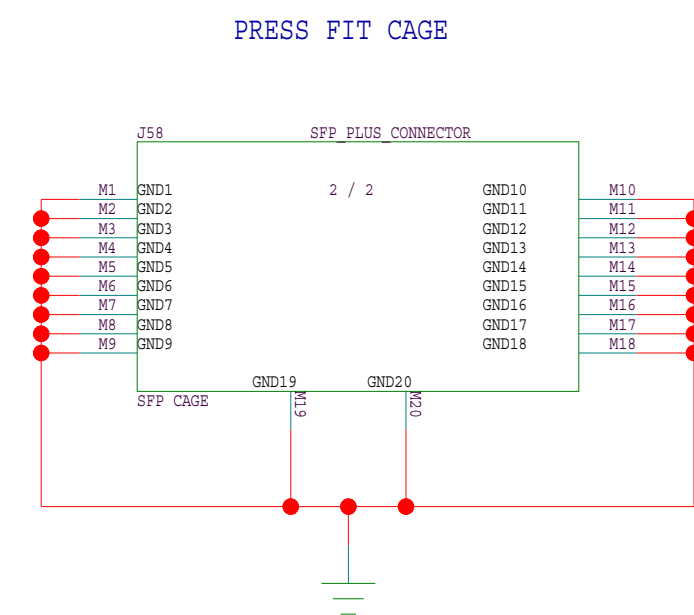
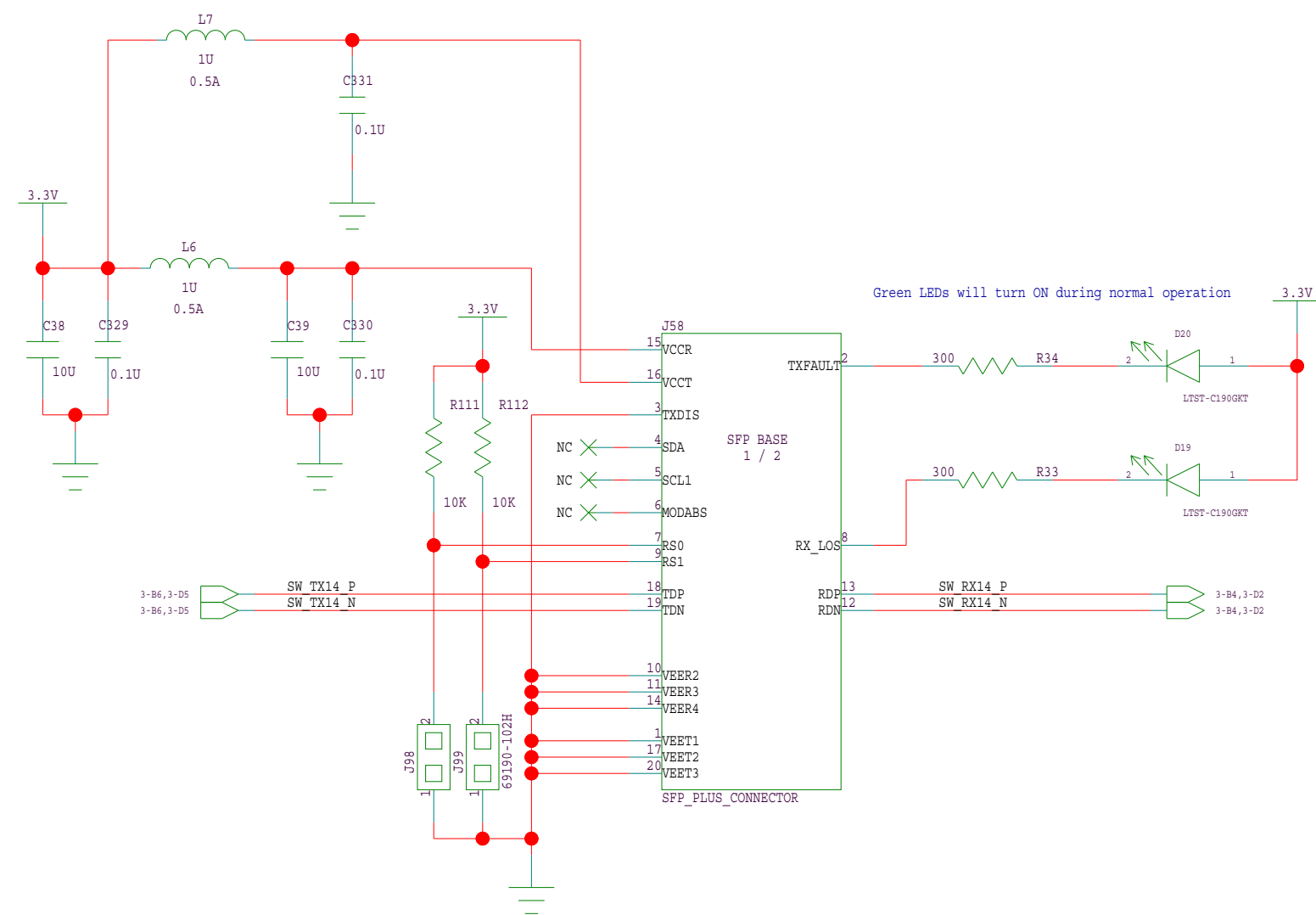
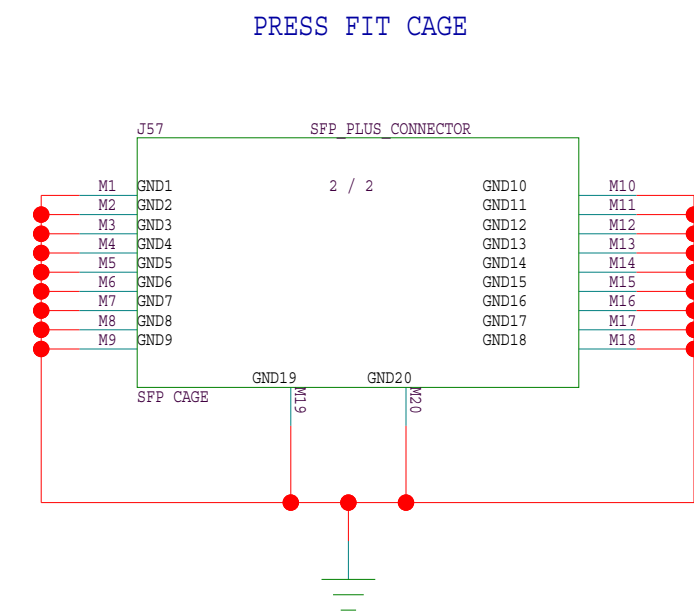
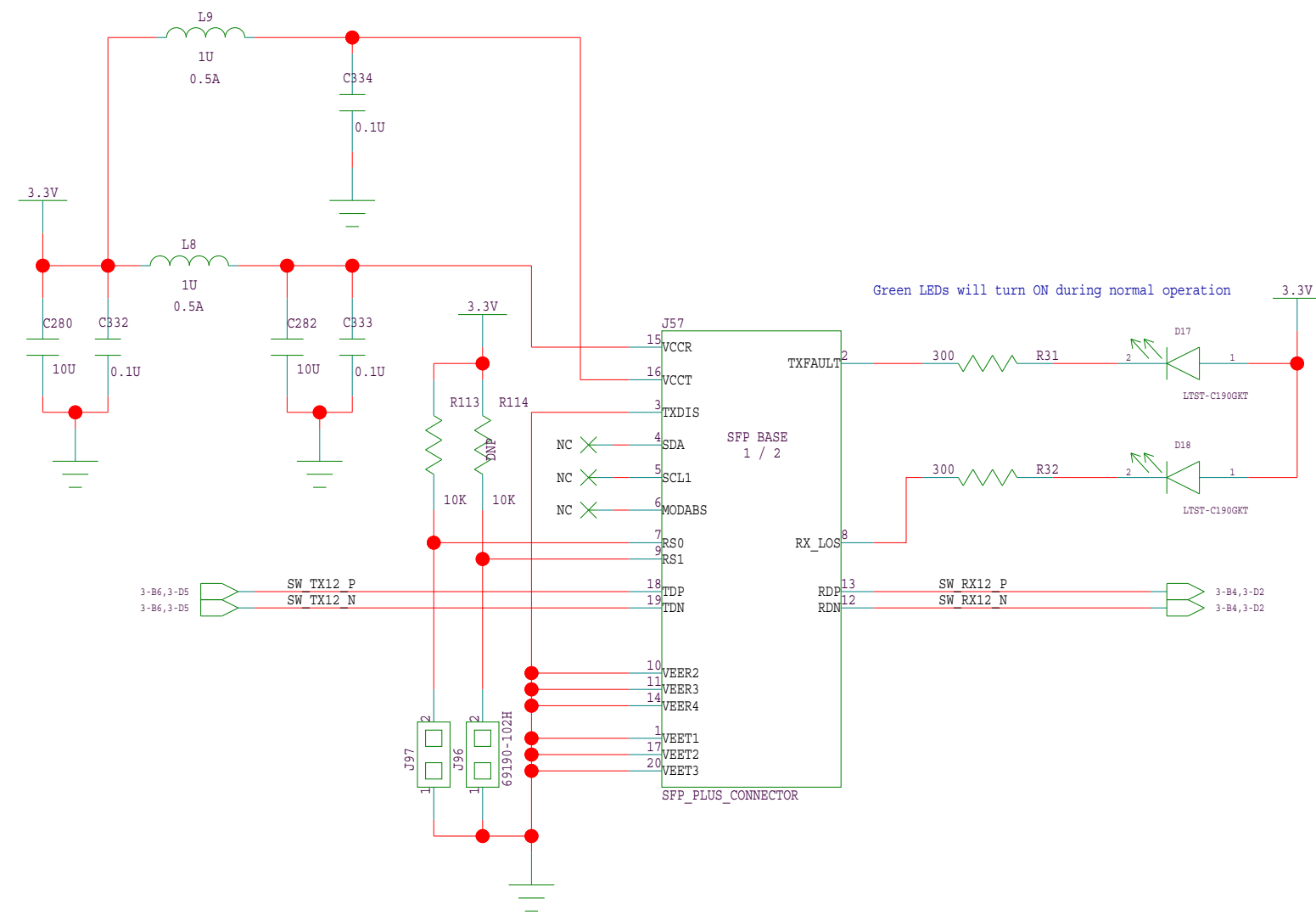


80HSPS1616 SMAs



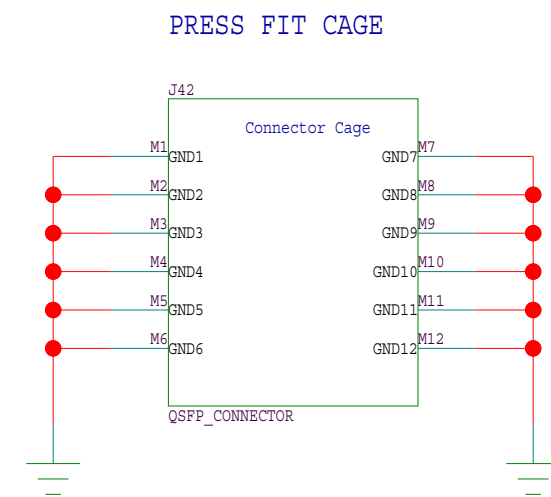
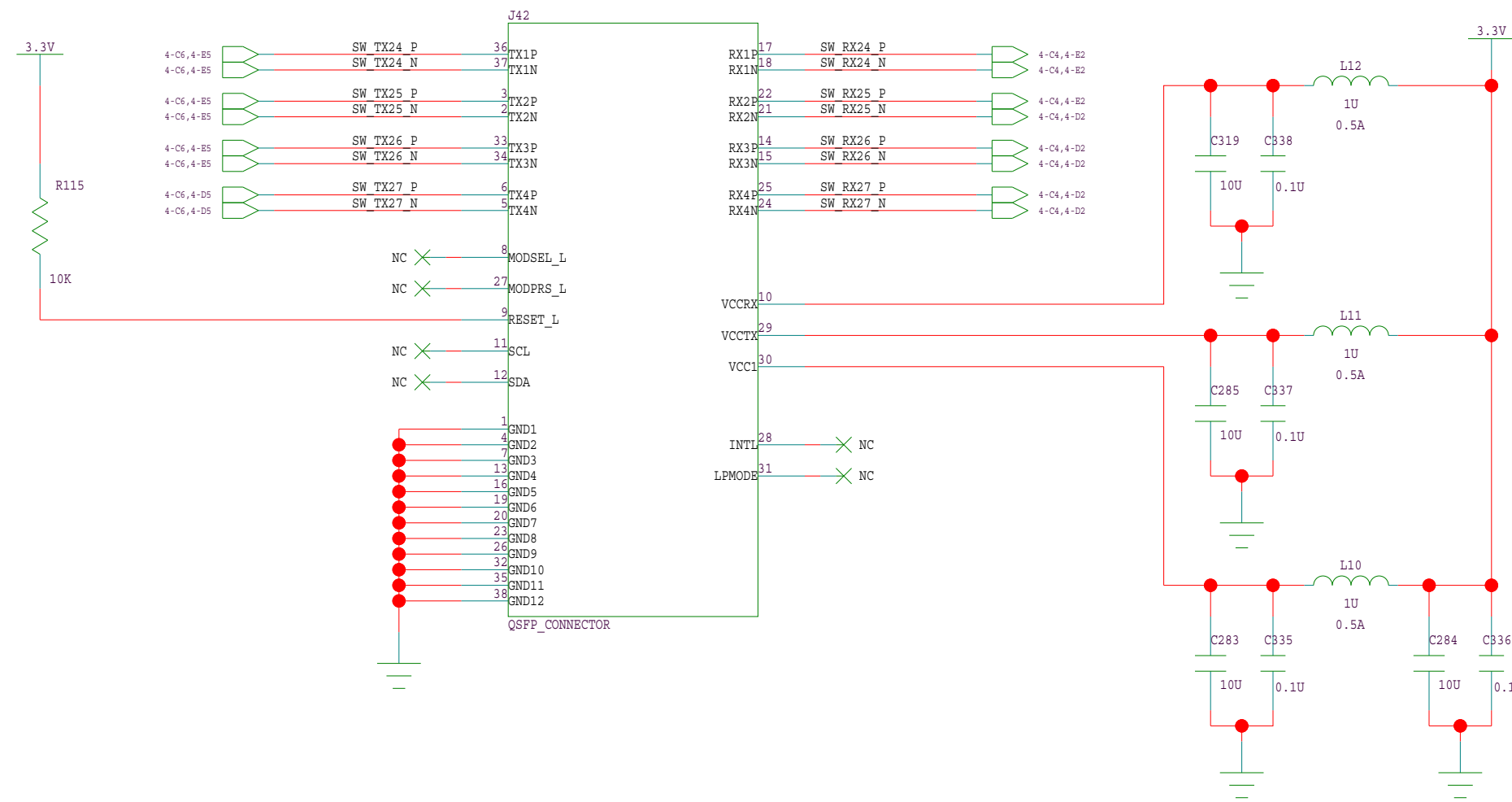
TITLE : SMA FIELD			
SIZE : C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:45		SHEET	17 OF 25

SFP Connectors



TITLE : SFP CONNECTORS			
SIZE : C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:45		SHEET 18 OF 25	

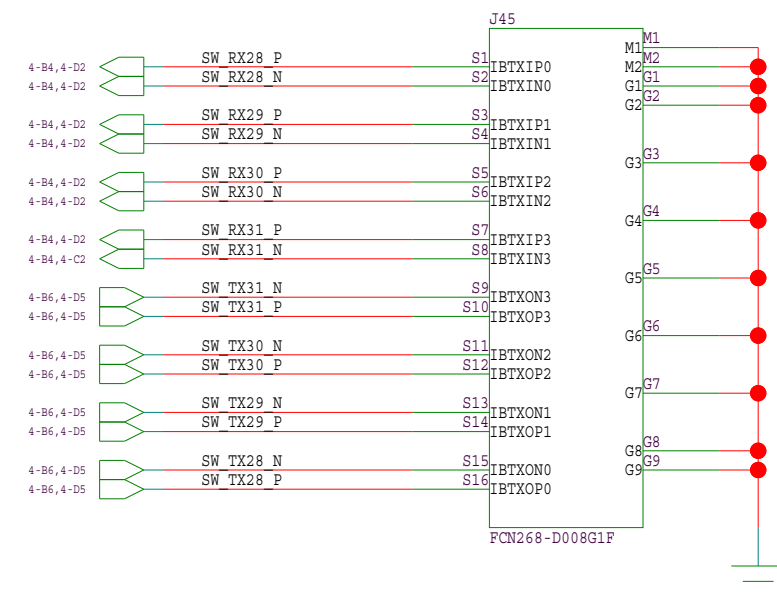
QSFP Connector



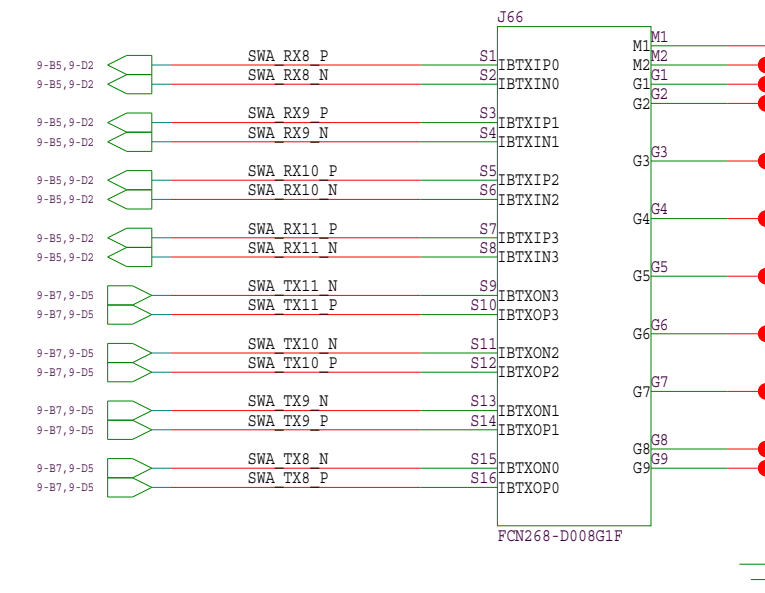
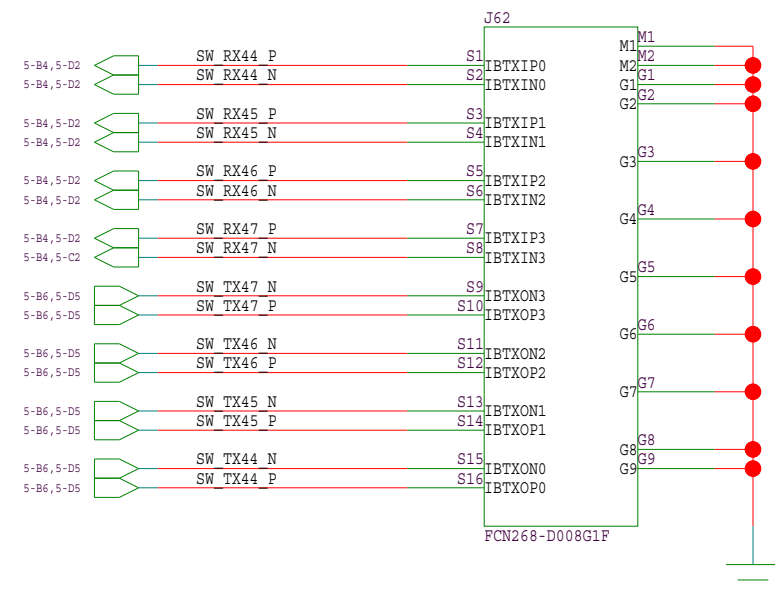
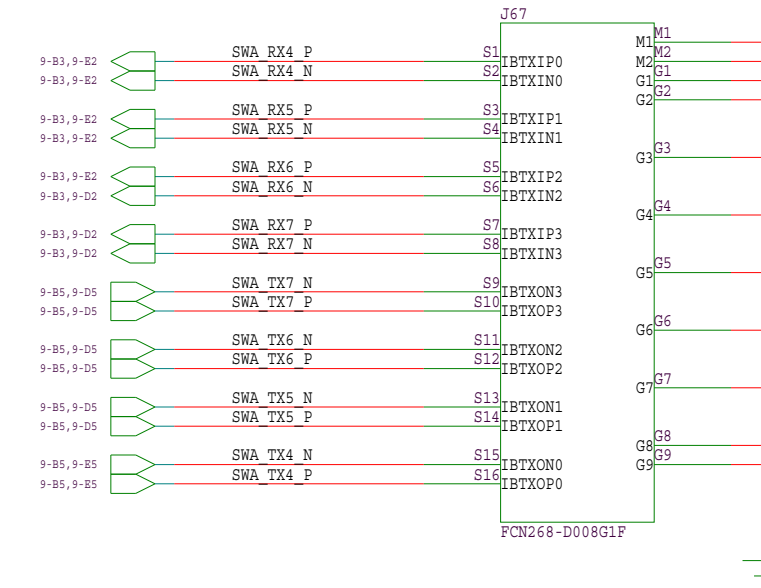
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SIZE : C	DRAWING NUMBER :	Version :	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:45		SHEET 19 OF 25	

INFINIBAND Connectors

80HCPS1848 Connectors



80HSPS1616 Connectors

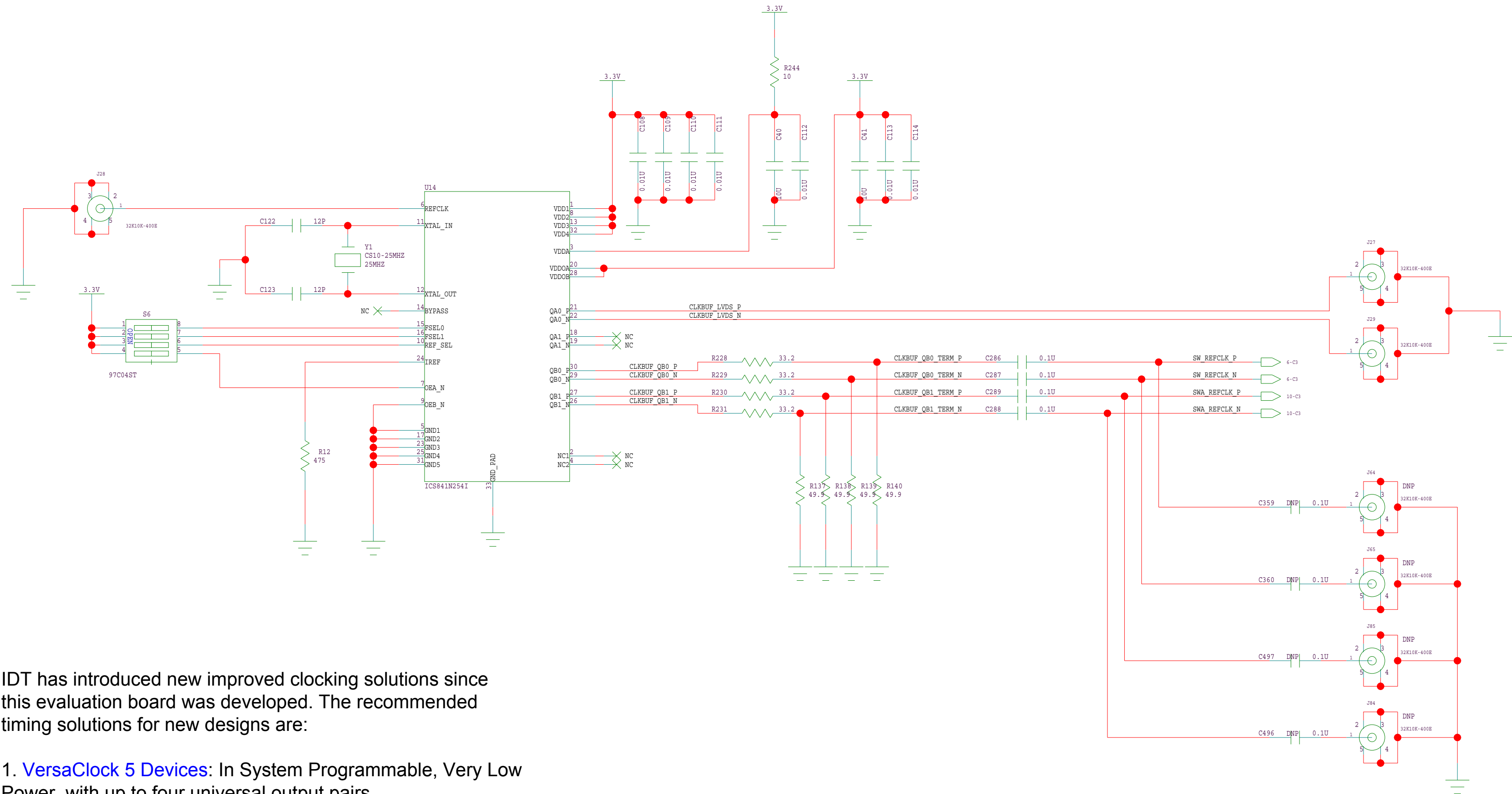


TITLE : INFINIBAND CONNECTORS

SIZE : C DRAWING NUMBER : Version: DESIGNER :

LAST MODIFIED DATE : 7-22-2010_16:45 SHEET 20 OF 25

Clocking



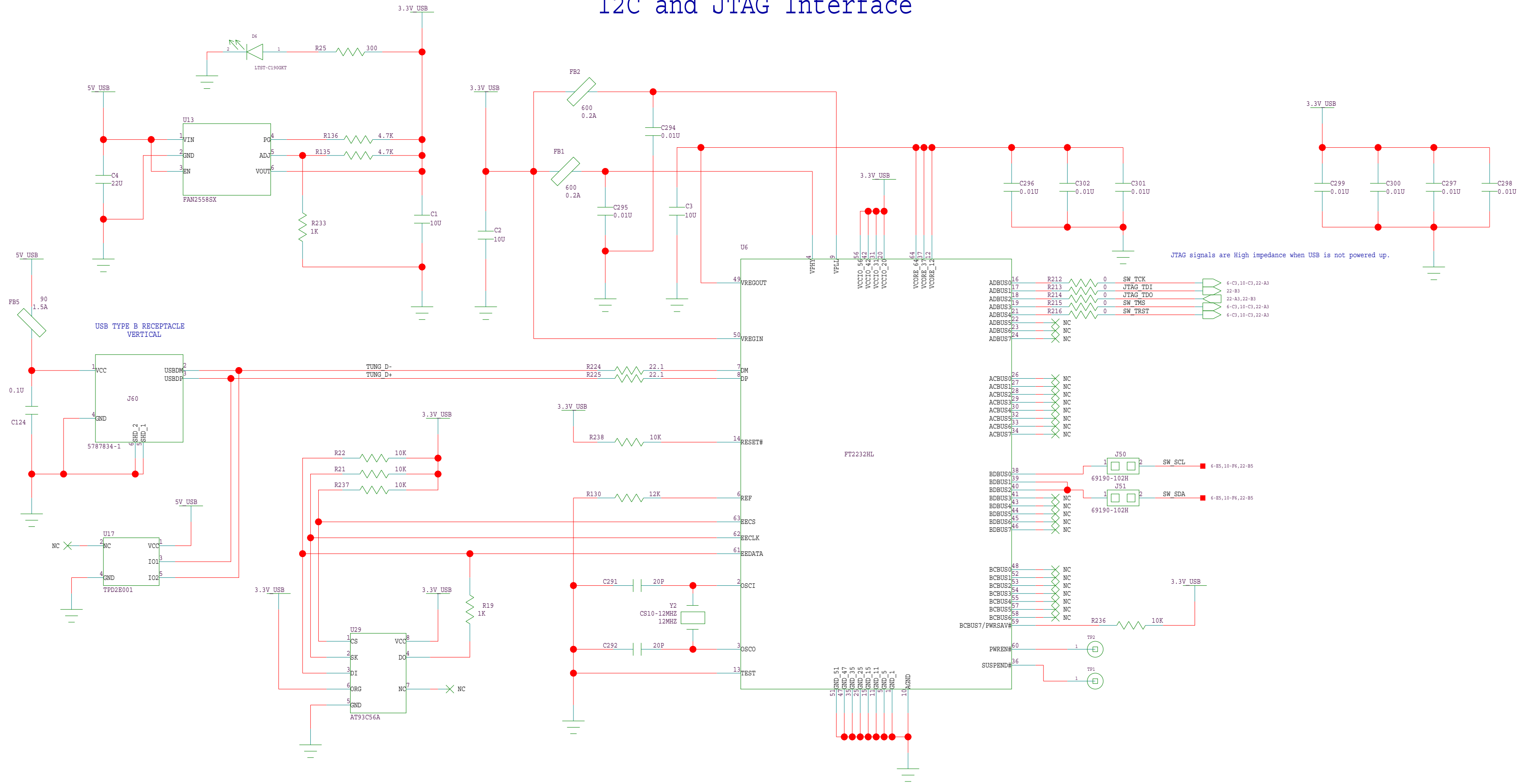
IDT has introduced new improved clocking solutions since this evaluation board was developed. The recommended timing solutions for new designs are:

1. **VersaClock 5 Devices:** In System Programmable, Very Low Power, with up to four universal output pairs.
2. **XUM LVDS Crystal Oscillator:** Ultra precise with only 300fs typical phase jitter. If using a 156.25 MHz clock source then the applicable part number is XUM535156.250JS618.

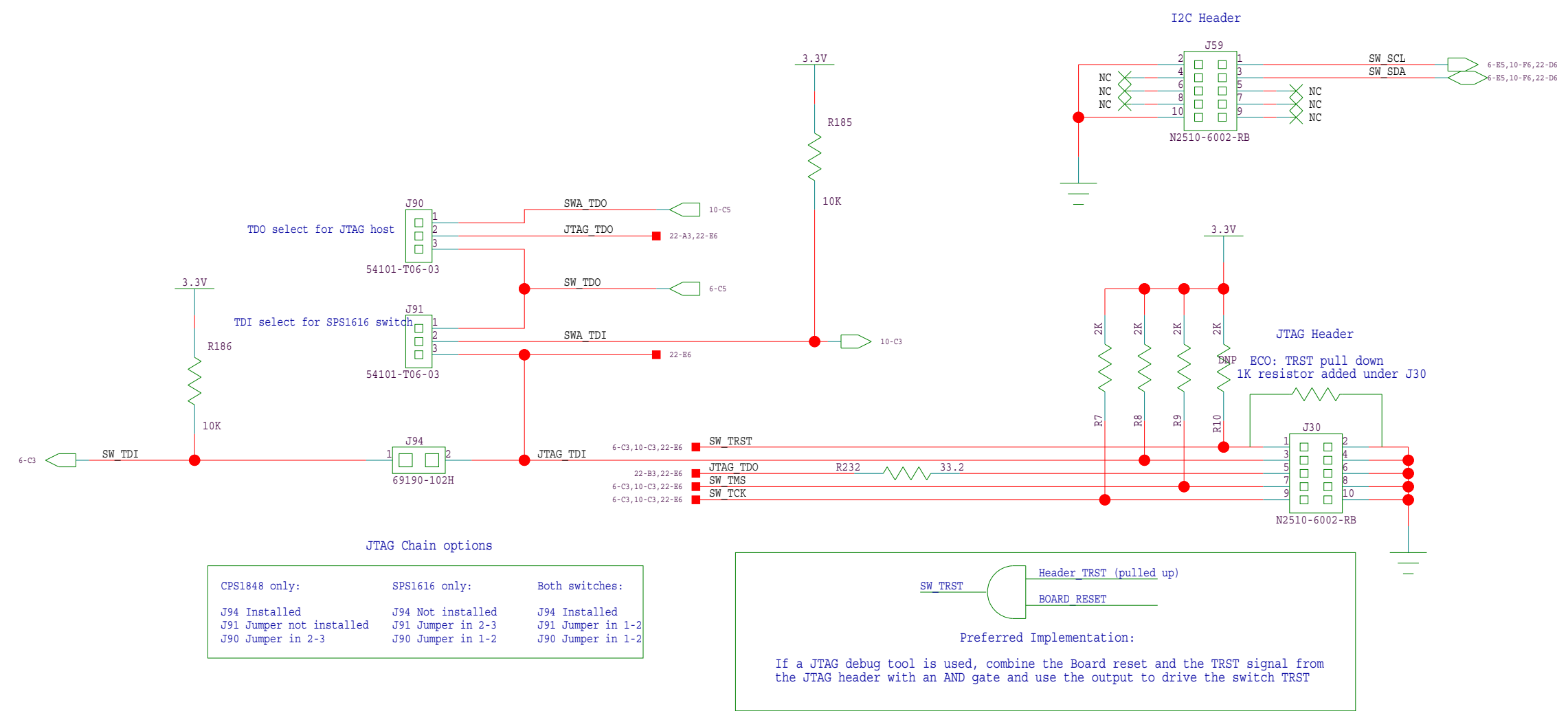


TITLE : CLOCKING			
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LAST MODIFIED DATE : 7-22-2010_16:45		SHEET 21 OF 25	

I2C and JTAG Interface

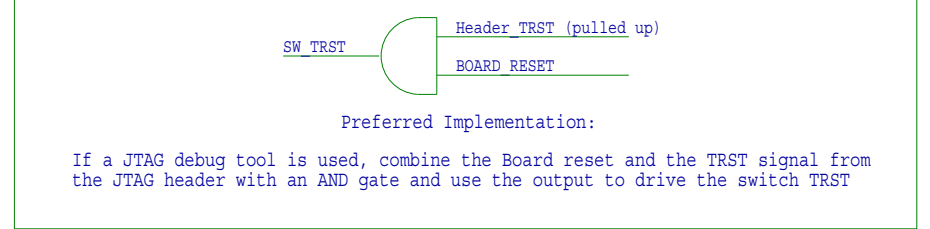



JTAG signals are High impedance when USB is not powered up.



JTAG Chain options

CPS1848 only:	SPS1616 only:	Both switches:
J94 Installed	J94 Not installed	J94 Installed
J91 Jumper not installed	J91 Jumper in 2-3	J91 Jumper in 1-2
J90 Jumper in 2-3	J90 Jumper in 1-2	J90 Jumper in 1-2





IDT

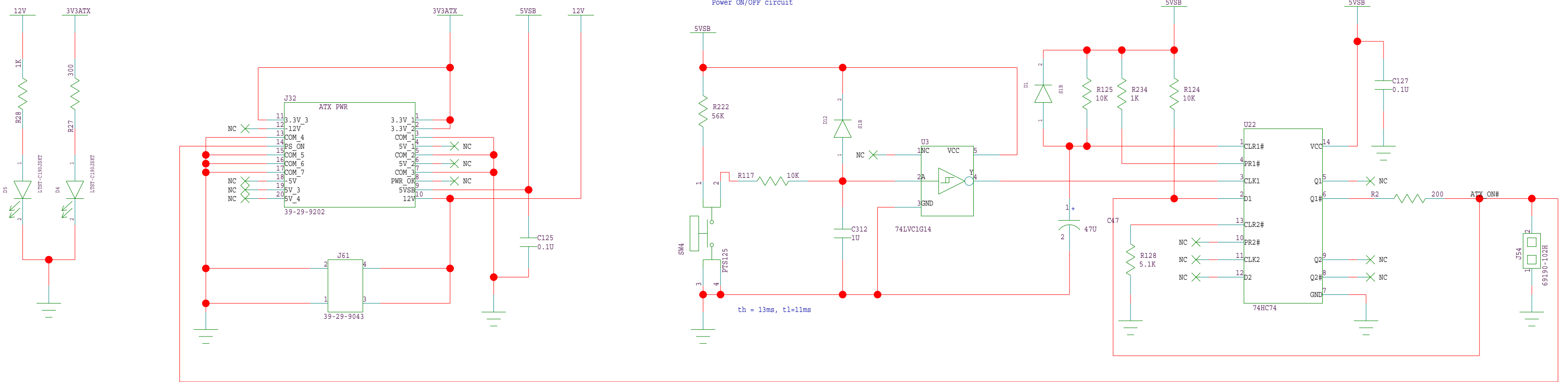
TITLE : I2C AND JTAG INTERFACE

SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			

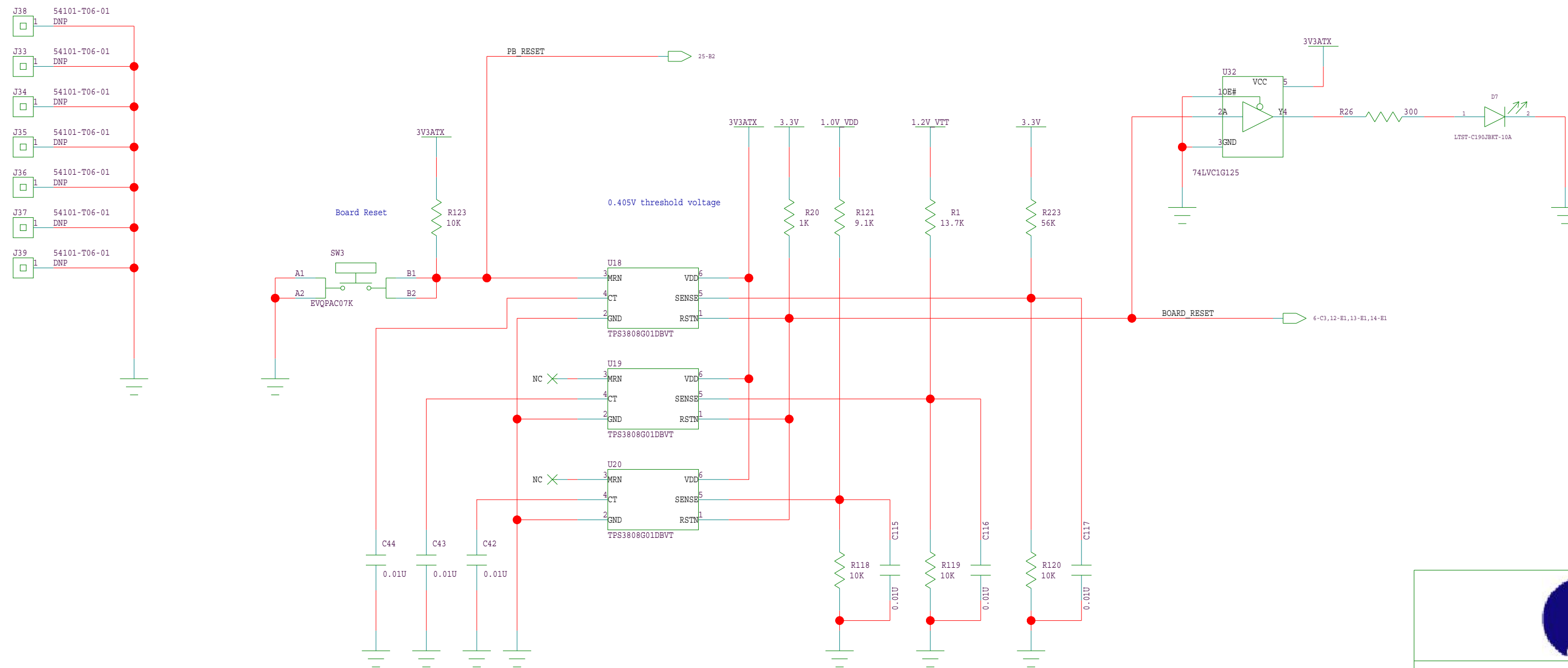
LAST MODIFIED DATE : 1-26-2011_14:53

SHEET 22 OF 25

ATX Power



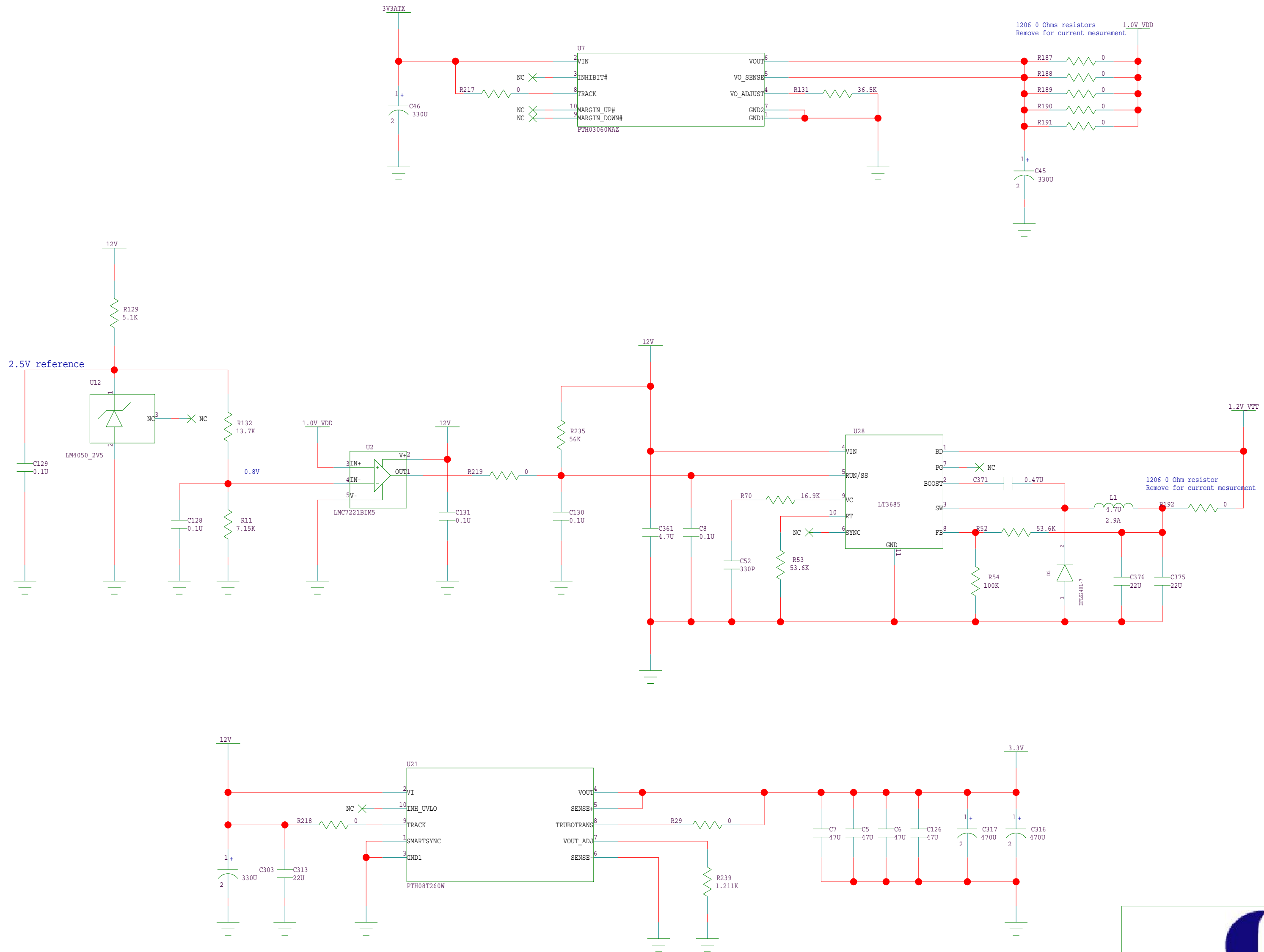
Voltage Monitors Board Reset




TITLE : ATX POWER			
SIZE : C	DRAWING NUMBER :	Version :	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:45		SHEET 23	OF 25

Voltage Regulators for 80HCPS1848

Following power-up sequence is necessary in order for the device to function properly: The serdes voltage (VDDS) needs to power-up first followed by serdes voltage (VDDT). The voltages on any Input or I/O pins cannot exceed its corresponding supply voltage during power supply ramp up.



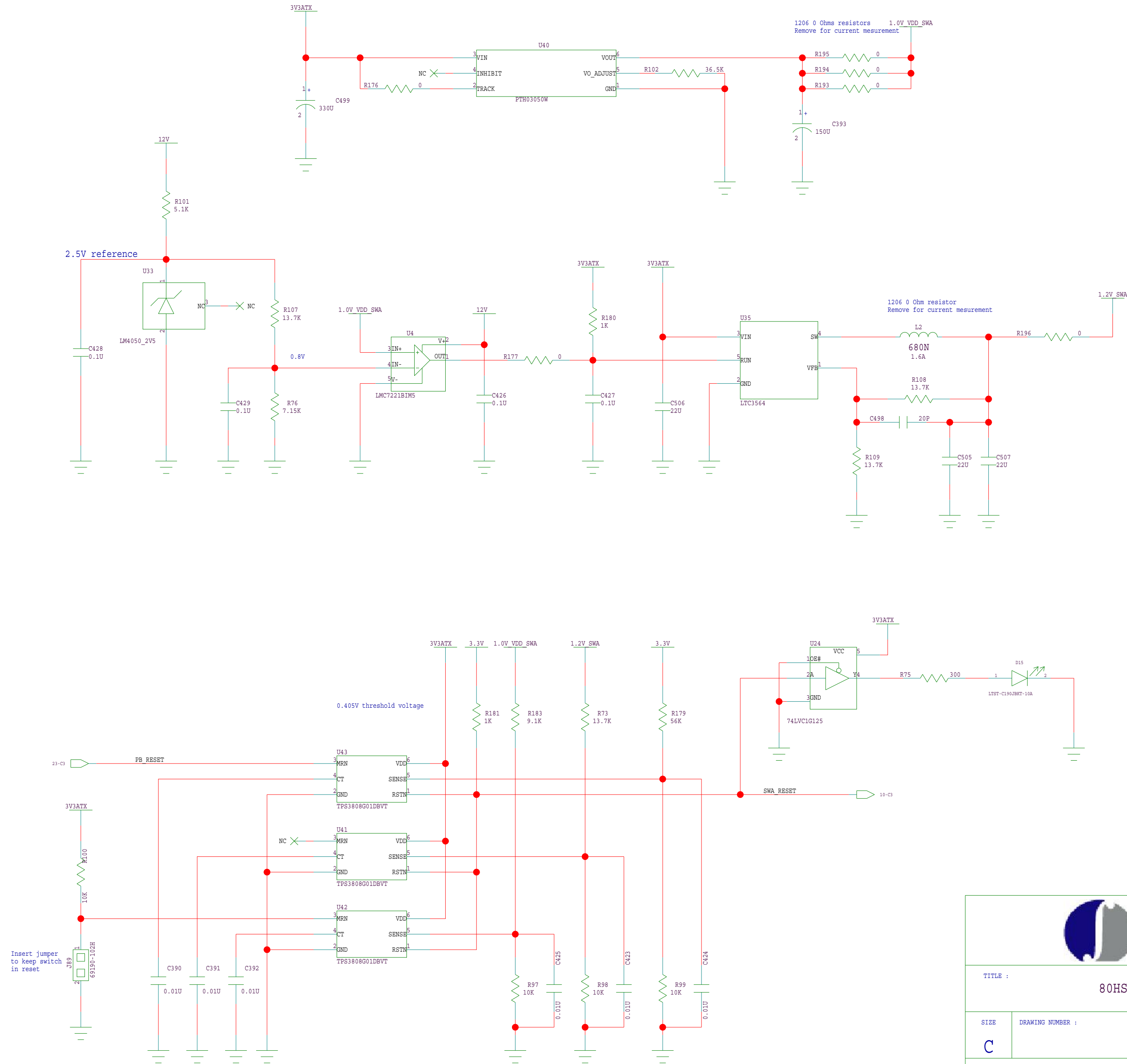


IDT

TITLE : 80HCPS1848 REGULATORS			
SIZE	DRAWING NUMBER :	Version:	DESIGNER :
C			
LAST MODIFIED DATE :		SHEET	
7-22-2010_16:45		24	OF 25

Voltage Regulators for 80HSPS1616

Following power-up sequence is necessary in order for the device to function properly: The serdes voltage (VDDS) needs to power-up first followed by serdes voltage (VDDT). The voltages on any Input or I/O pins cannot exceed its corresponding supply voltage during power supply ramp up.



TITLE : 80HSPS1616 REGULATORS			
SIZE : C	DRAWING NUMBER :	Version :	DESIGNER :
LAST MODIFIED DATE : 7-22-2010_16:45		SHEET 25 OF 25	

Revision History

April 7, 2015 -- Added a note on sheet 21 on improving clocking solutions for S-RIO components.

April 1, 2011 -- Changed FB3/FB4 on sheet 7, and FB6 on sheet 11, to 60 Ohms 3A.

January 26, 2011 -- Added a JTAG TRST implementation note on sheet 22.

September 13, 2010 -- Updated the JTAG Header resistor on sheet 22.

July 26, 2010 -- First release of document.



TITLE : Revision History			
SIZE C	DRAWING NUMBER :	Version:	DESIGNER :
LAST MODIFIED DATE :			SHEET