REV	COMMENT	DATE	DRAWN BY
1.00	Release	22/12/2016	M.Rafenne
2.00	Update V1.10 / V2.00 (mod1)	13th,Feb 2017	R.Romes

Preliminary

CONFIDENTIAL

RENESAS Electronics Europe GmbH

Title: y_ask_rcar_v3m_ws10

Size: A2 | Document Number: EESS-0400-133-01

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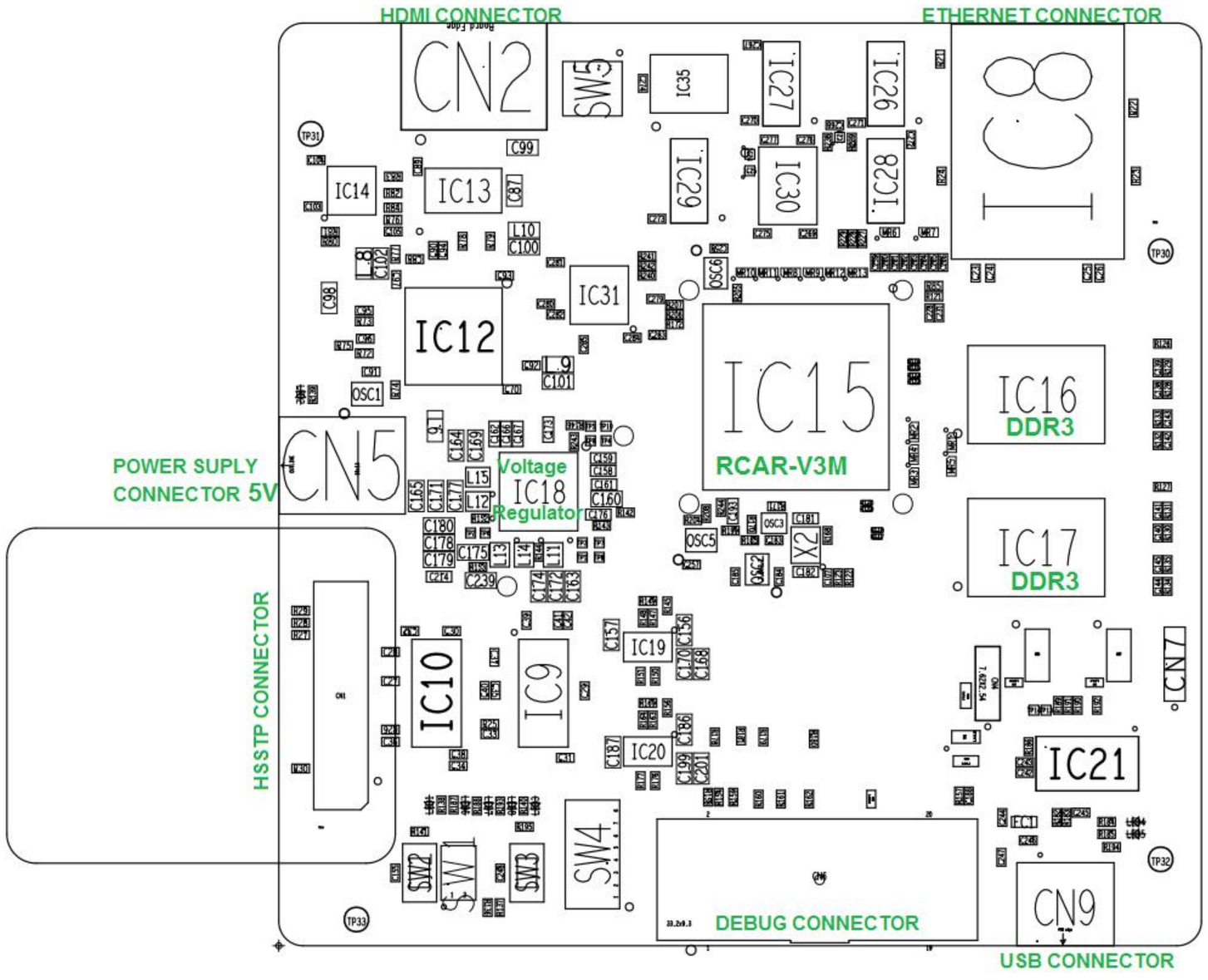
P02: Placement



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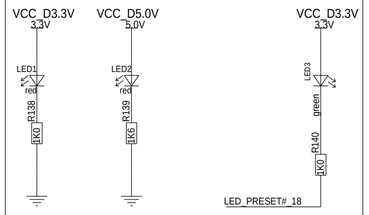
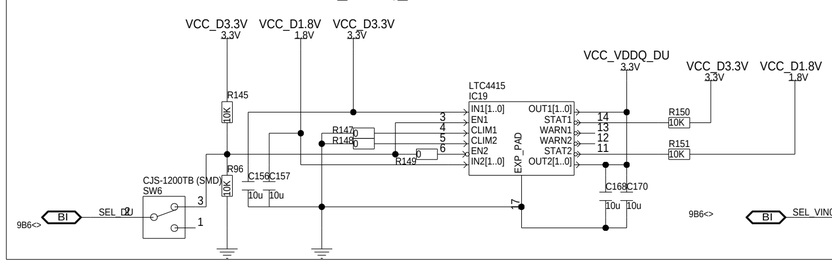
P03: R-CarV3M _POWER

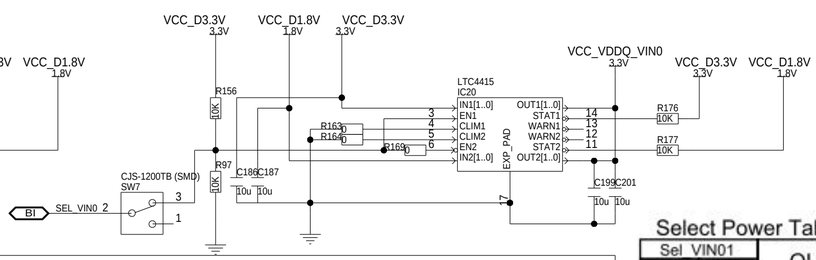
POWER LED's / SYSTEM Reset LED



VCC_VDDQ_DU SELECT



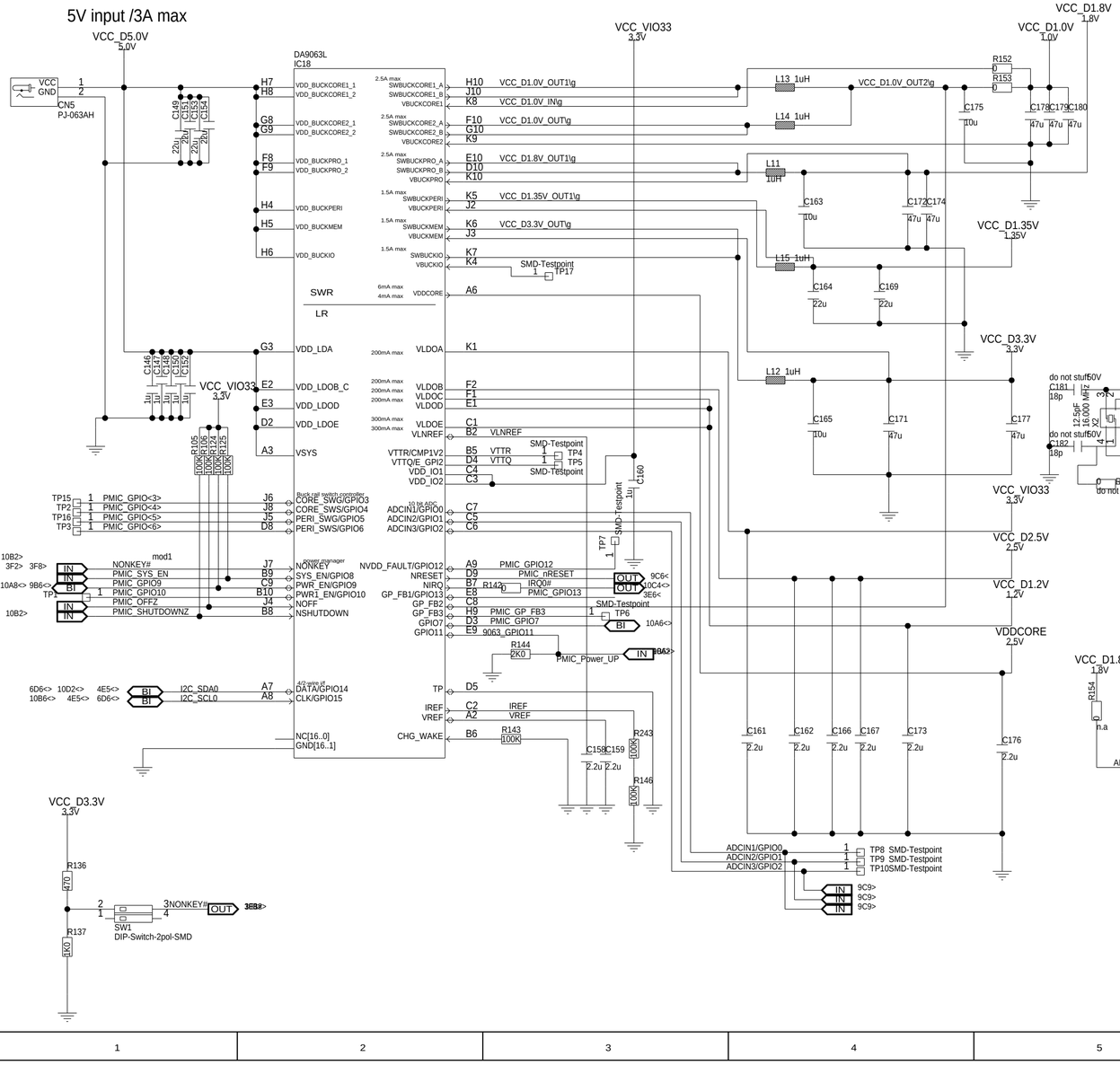
VCC_VDDQ_VIN0 SELECT



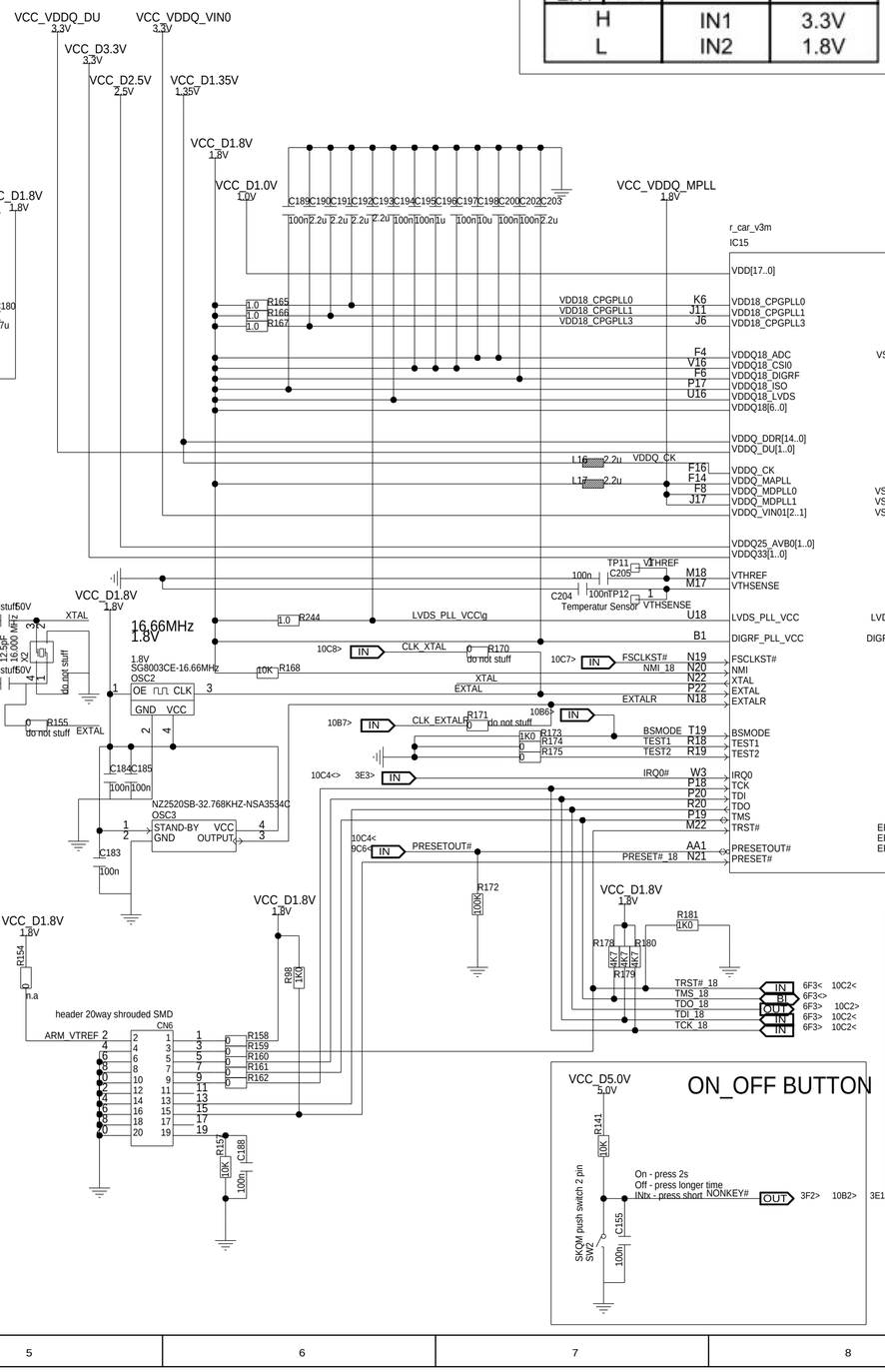
Select Power Table

Sel_VIN01		OUT	Voltage
EN1	EN2		
H		IN1	3.3V
L		IN2	1.8V

5V input /3A max

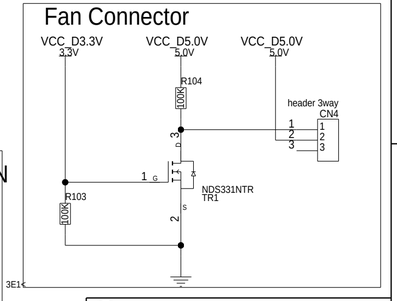


VCC_D1.8V / VCC_D1.0V / VCC_D1.35V / VCC_D2.5V / VCC_D3.3V



ON_OFF BUTTON

Fan Connector



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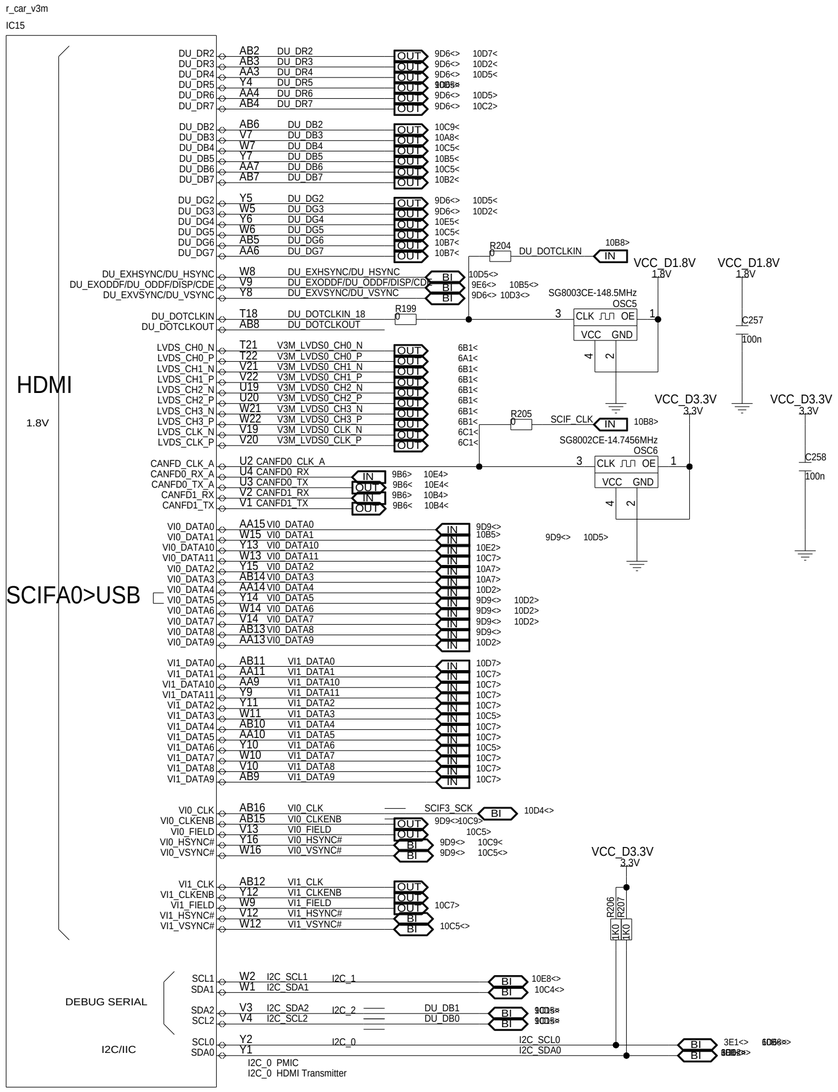
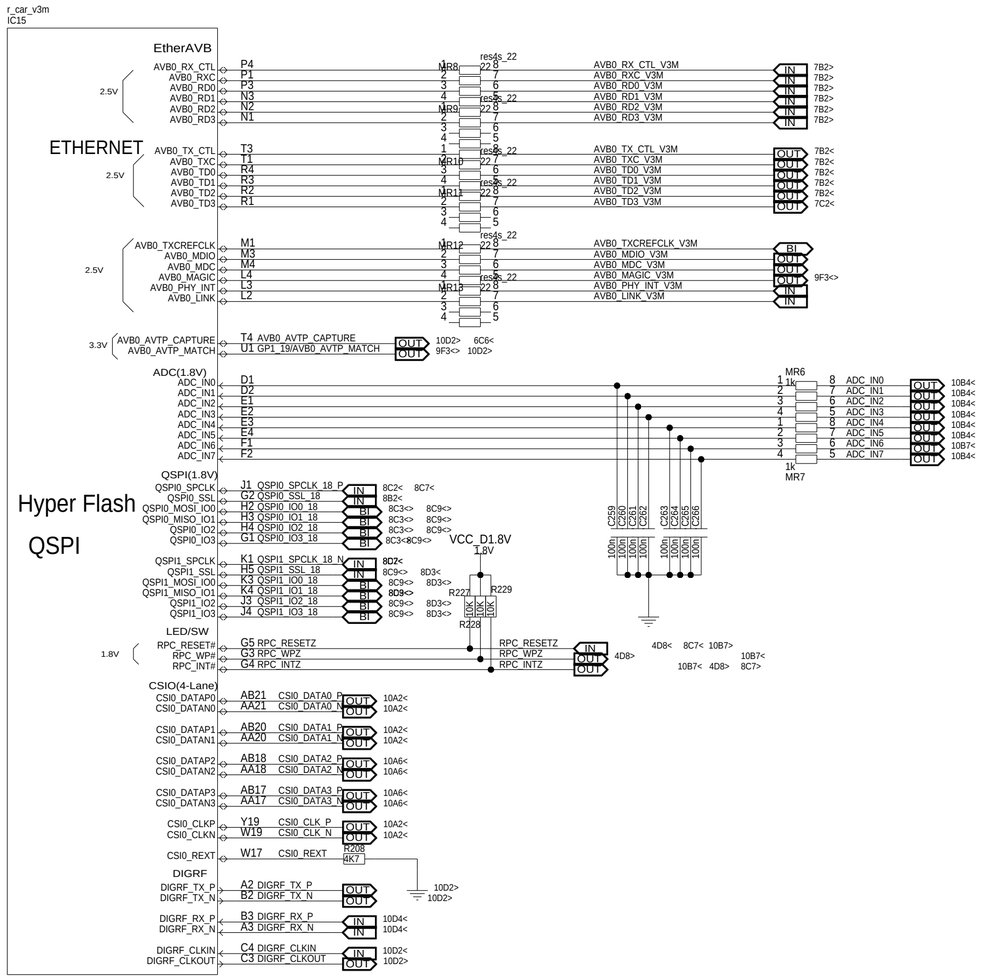
P04: R-CarV3M





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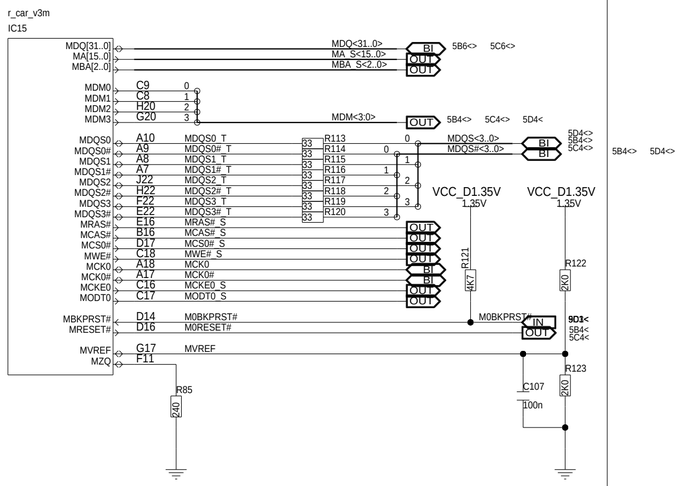
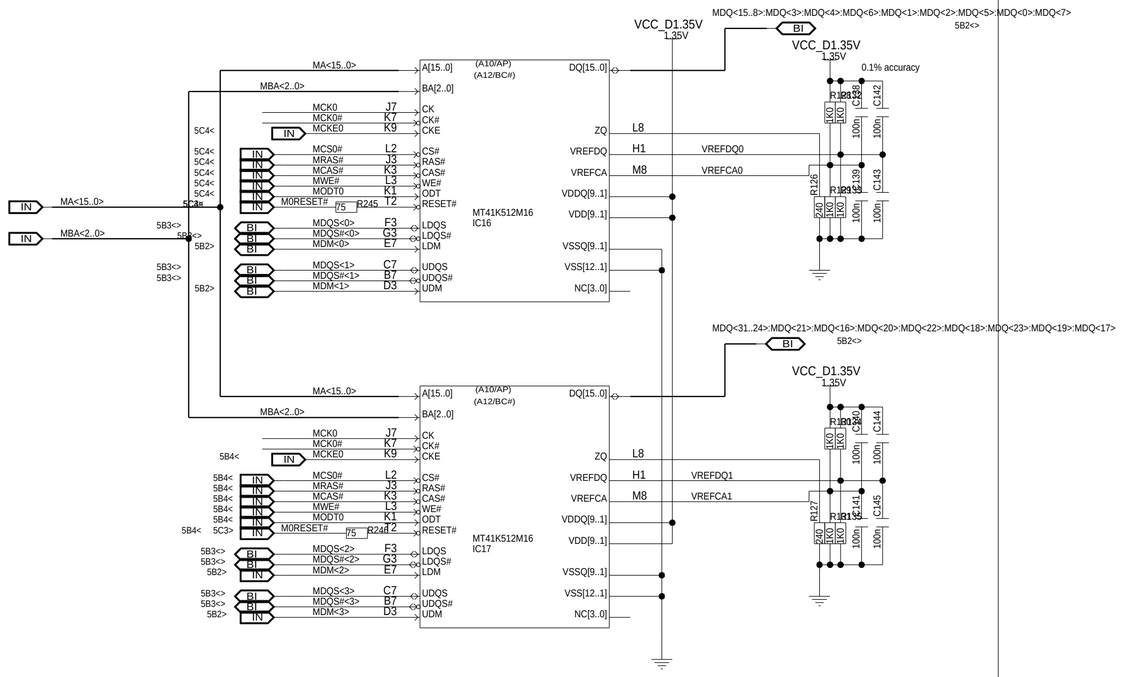
P05: R-CarV3M DDR3L

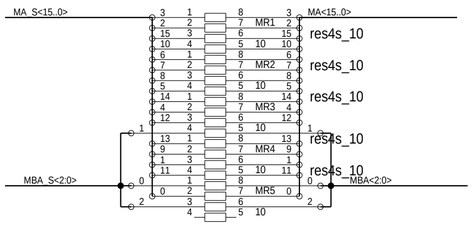
V3M DDR3L

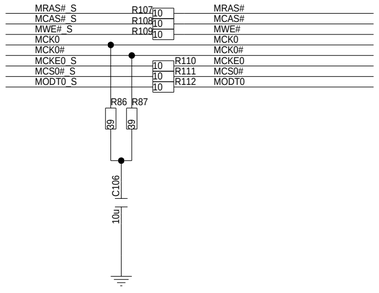


2 x DDR3 = 1Gbyte

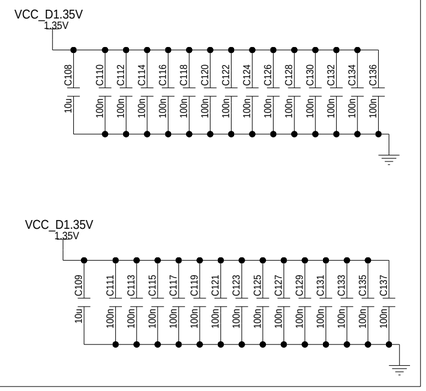


Signals Termination





DDRs Decoupling



1GBx2 = 2GByte

Layout Note:

Following signals need Ground guard.

MCK0, MCK0#

RENESAS Electronics Europe GmbH			
Title: y_ask_rcar_v3m_ws10			
DDR3 2x32bit (2GByte)			
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P06: R-CarV3M HDMI

HDMI

REV	COMMENT	DATE	DRAWN BY
1.00	Release	22/12/2016	M.Rafenne

LAYOUT!
LVDS(V3M_LVDS_CLK,V3M_LVDS[3:0])
(1)Matched trace length from V3M
until IC9 (LVDS Receiver)
and HSSTP Connector
(2) Differential Impedance= 100 ohm

LAYOUT!
LVDS(SK_LVDS_CLK,SK_LVDS[3:0])
(1)Matched trace length from IC9
until IC10 (LVDS Receiver)
(2) Differential Impedance= 100 ohm

LAYOUT!
LVDS(LVDS_CLK ,LVDS[3:0])
(1)Matched trace length from IC9
until comexpress connector
(2) Differential Impedance= 100 ohm

LAYOUT!
B_HDMI_ signals
(1)Matched trace length from IC12
until IC14
(2) Differential Impedance= 100 ohm

LAYOUT!
HDMI_ signals
(1)Matched trace length from IC12
until IC14
(2) Differential Impedance= 100 ohm

[Design Note]
LVDS_SEL _SK- ON: Selects HDMI output side.
LVDS_SEL _SK- OFF: Selects HSSTP Connector side.

LAYOUT!
LVDS(TH63_LVDS_CLK,,TH63_LVDS[3:0])
(1)Matched trace length from IC10
until IC11 (LVDS Receiver)
(2) Differential Impedance= 100 ohm

TH63_DK level can be HI or LOW !?

#[HSSTP 40pin] HSSTP Connector

LAYOUT!
LVDS(HSSTP_LVDS_CLK, HSSTP_LVDS[3:0])
(1)Matched trace length from IC10
until IC11 (LVDS Receiver)
(2) Differential Impedance= 100 ohm

RENESAS Electronics Europe GmbH

Title: y_ask_rcar_v3m_ws10
DU (YCbC3/LVDS), SDx,USBx,..

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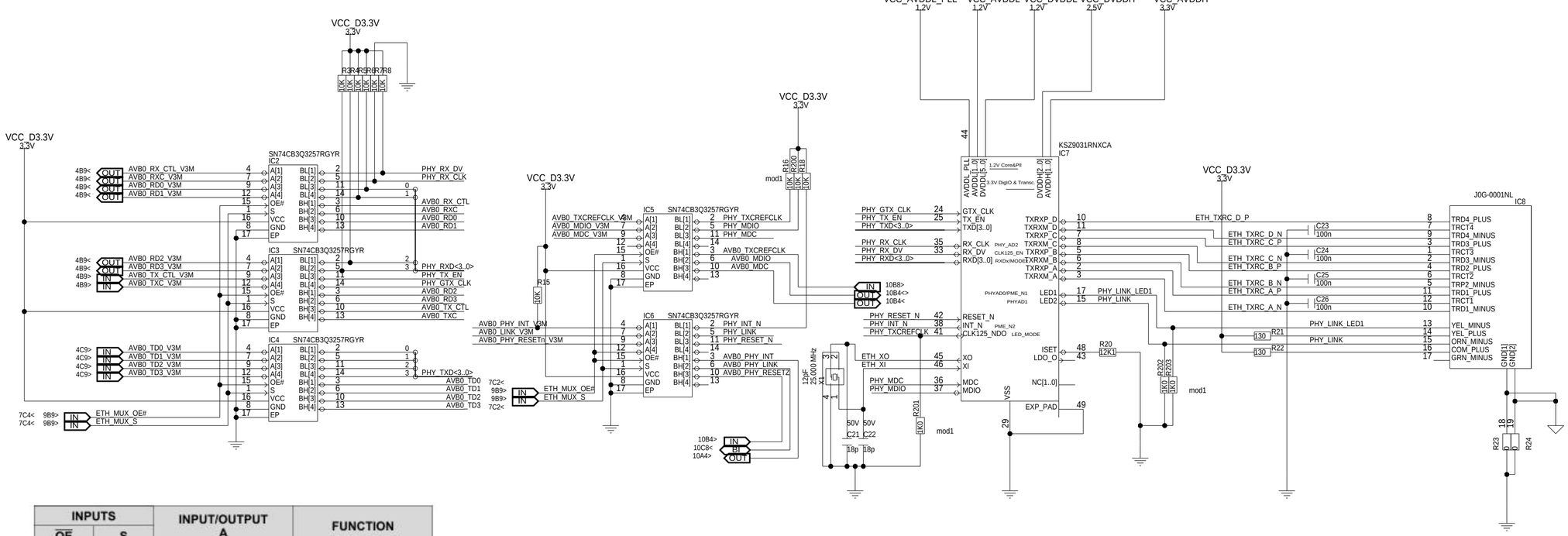
P07: R-CarV3M ETHERNET

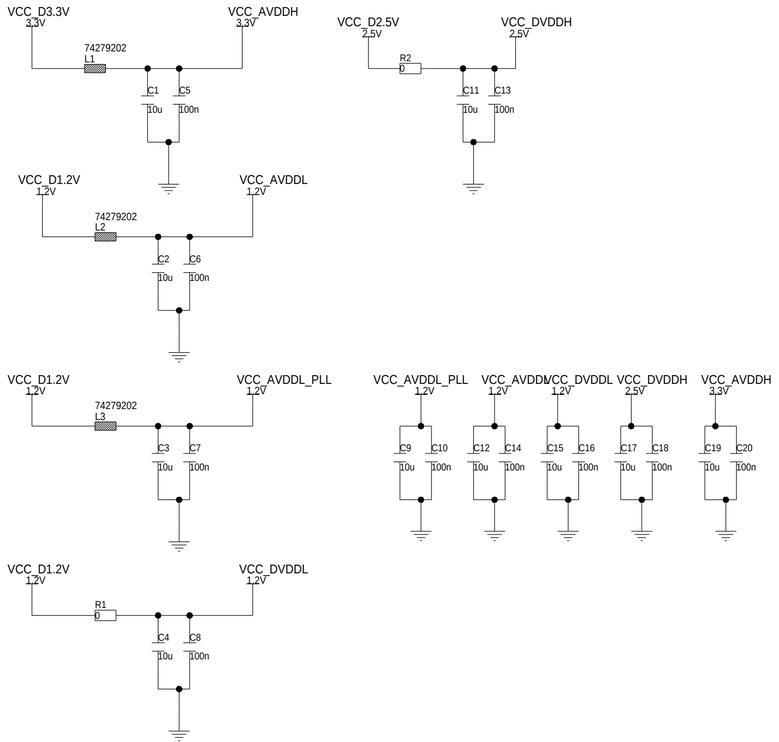
Group 1
AVB_TXC _V3M
AVB_TX_CTL_V3M
AVB_TD[3:0] _V3M
Group 2
AVB_RXC _V3M
AVB_RX_CTL _V3M
AVB_RD[3:0] _V3M
Layout Note:
Matched Trace Length from R-CarV3M to KSZ9031.
(max 250Mbps/pin)

CPLD configuratrion

IF	and	Then
AVB0_MAGIC_V3M	PRESETOUT#	AVB0_PHY_PRESETn_V3M
0	0	0
0	1	0
1	0	0
1	1	1

INPUTS		INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S		
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect





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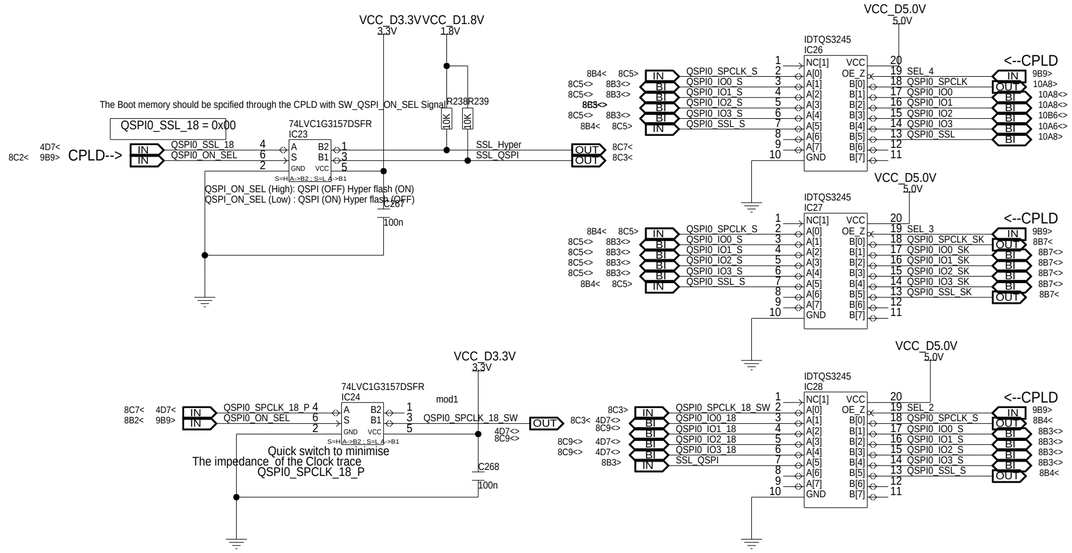
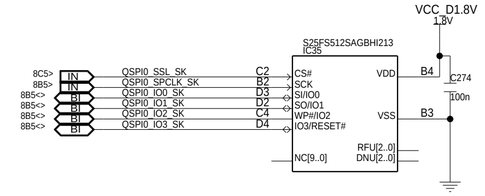
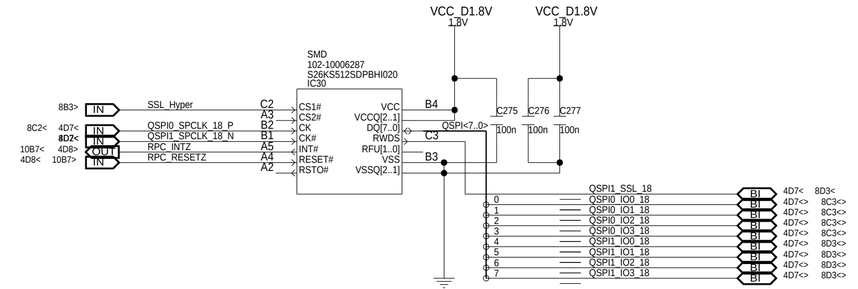
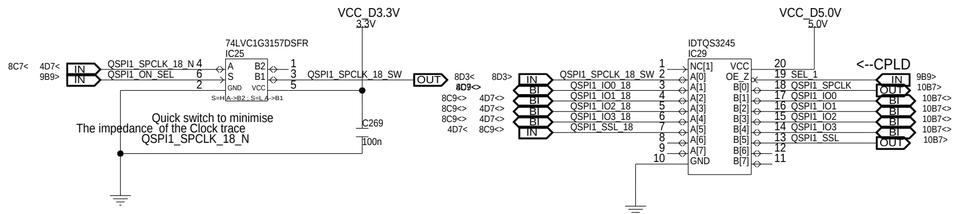
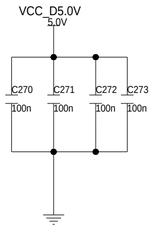
P08: QSPI_Hyper_FLASH











CPLD signals configuration						
	QSPI0_ON_SEL	QSPI1_ON_SEL	SEL_1	SEL_2	SEL_3	SEL_4
Hyper_Flash	1	1	1	1	1	1
QSPI0_on_board	1	0	1	0	0	1
QSPI0_Base	0	0	1	0	1	0
QSPI1_Base	0	0	0	1	1	1

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Title: y_ask_rcar_v3m_ws10

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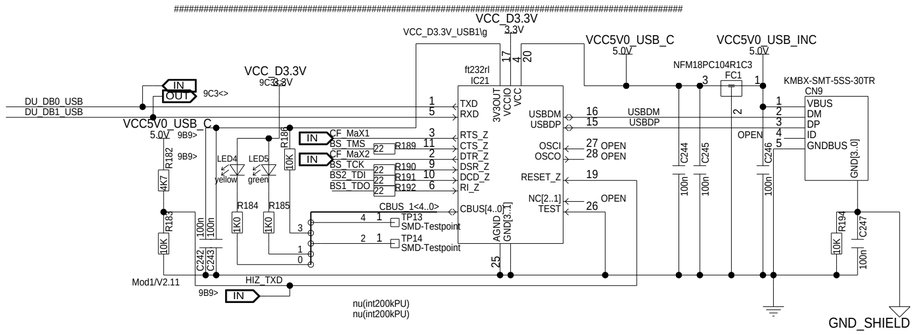
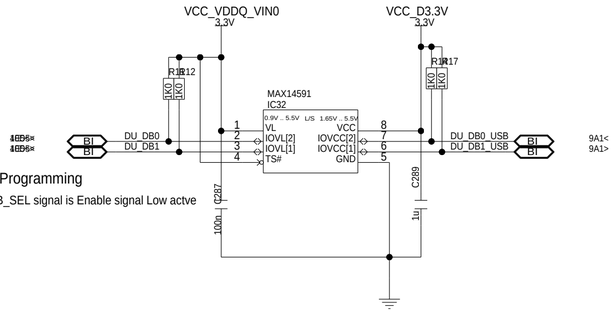
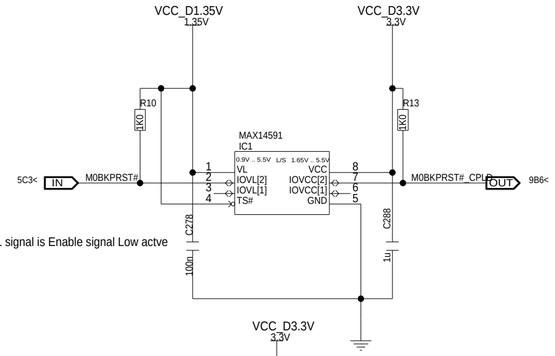
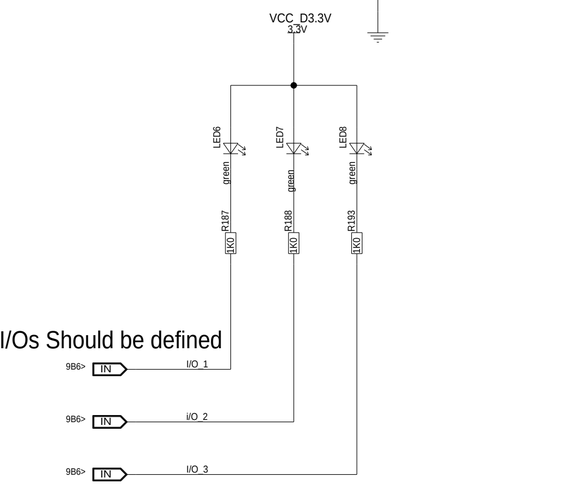
P09: MODE_SWITCH / SCIF to USB/ HMI

SCIF0>USB

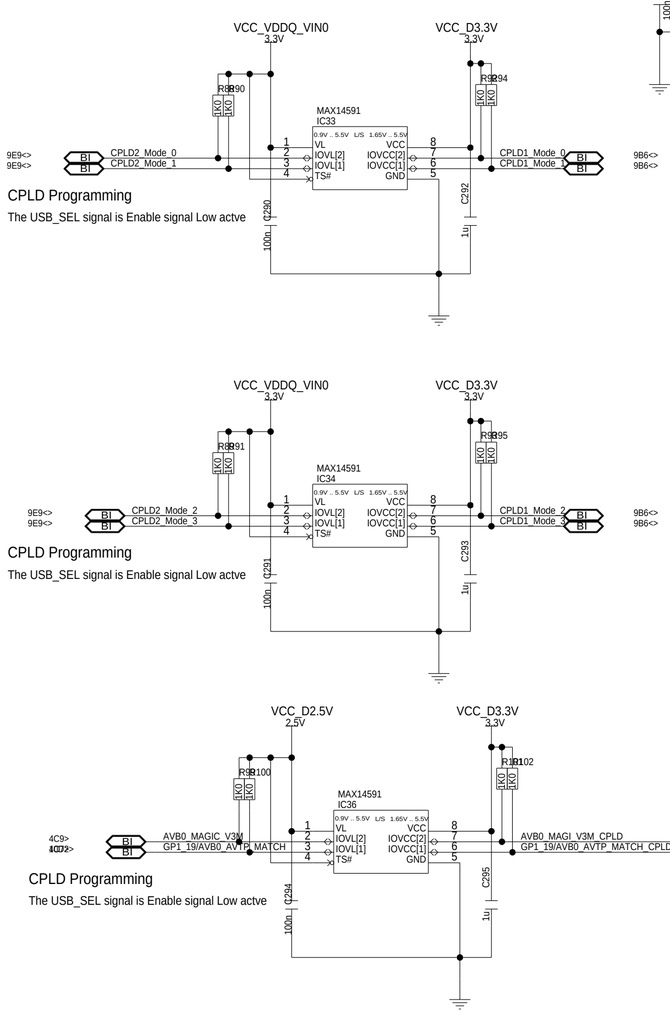






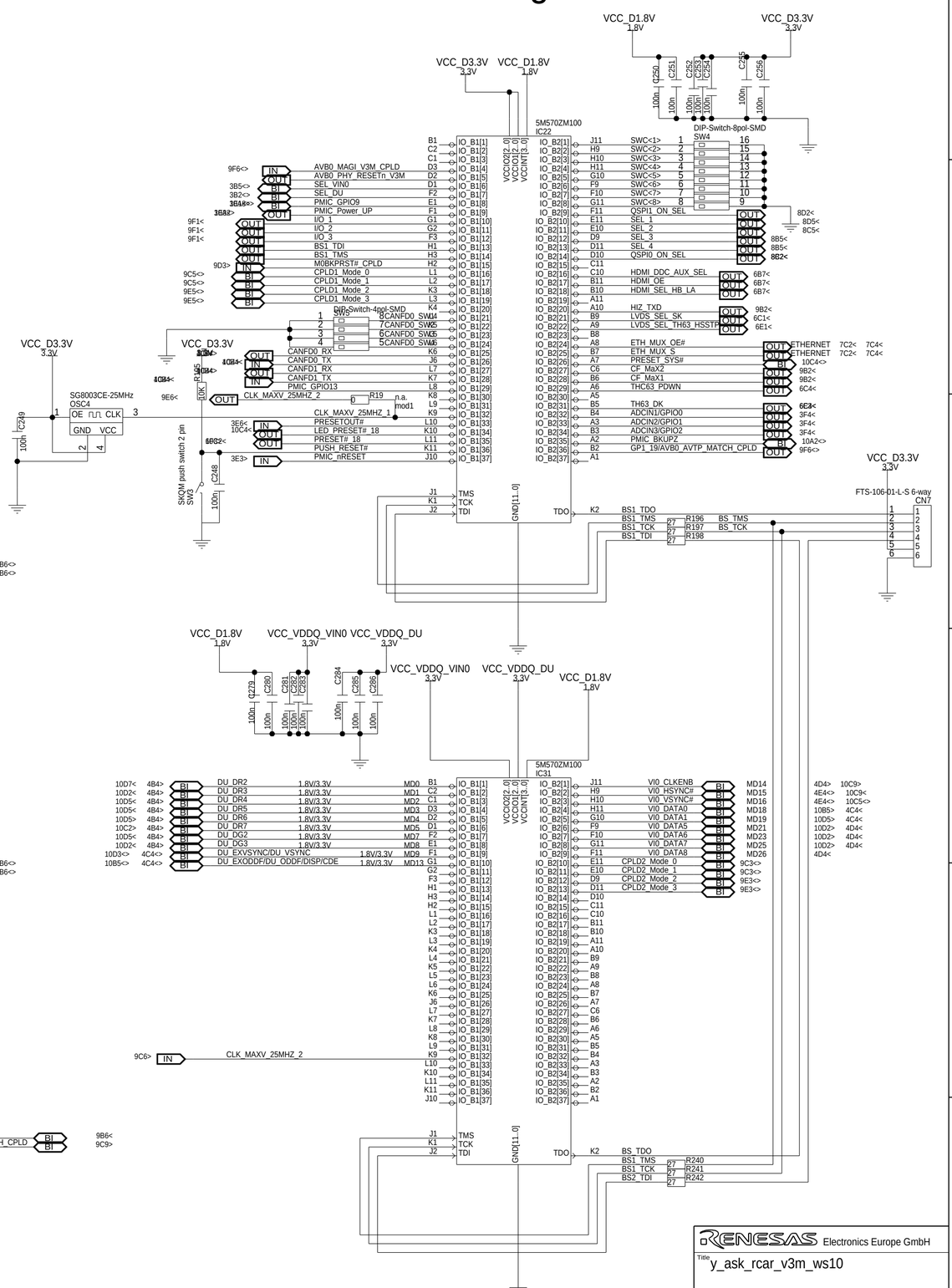


HMI OUTPUT/INPUT



Mode Pin setting via CPLD

After RESET# release High Z



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P10: R-CarV3M Connectors to Base Board

COMExpress440pin
CN3

H3 Signals

GND	A[1]	A1					
CSI2_DATAP0	A[2]	A2	CSI0_DATA0_P	IN	4D7>		
CSI2_DATAN0	A[3]	A3	CSI0_DATA0_N	IN	4D7>		
BKUP_TRG	A[4]	A4					
BKUP_REQB	A[5]	A5	PMIC_BKUPZ				
DVFS_PGD	A[6]	A6	PMIC_POWER_UP	BI	9C9<>		
CSI2_CLKN	A[7]	A7	CSI0_CLK_N	OUT	9B8<		
CSI2_CLKP	A[8]	A8	CSI0_CLK_P	IN	4E7>		
CSI2_DATAP1	A[9]	A9	CSI0_DATA1_P	IN	4E7>		
CSI2_DATAN1	A[10]	A10	CSI0_DATA1_N	IN	4E7>		
GND	A[11]	A11					
CSI3_DATAN0	A[12]	A12					
CSI3_DATAP0	A[13]	A13					
PWM2	A[14]	A14	GP0_17		DU_DB7		
EX_PWRONn	A[15]	A15	PMIC_ON_BTNZ		NONKEY#	IN	4B4>
CSI3_CLKN	A[16]	A16				OUT	3E1<
CSI3_CLKP	A[17]	A17					
RSTMODE_SW	A[18]	A18	PMIC_SHUTDOWNZ			OUT	3E1<
LVDS0_CLK_P	A[19]	A19	LVDS0_CLK_P			IN	
LVDS0_CLK_N	A[20]	A20	LVDS0_CLK_N			IN	
GND	A[21]	A21					
CSI1_DATAN1	A[22]	A22					
CSI1_DATAP1	A[23]	A23					
CSI1_CLKP	A[24]	A24					
CSI1_CLKN	A[25]	A25					
CSI1_DATAN0	A[26]	A26					
CSI1_DATAP0	A[27]	A27					
SCIF0_RX/SD0_VL	A[28]	A28					
LVDS0_CH1_P	A[29]	A29	LVDS0_CH1_P	IN			
LVDS0_CH1_N	A[30]	A30	LVDS0_CH1_N	IN			
GND	A[31]	A31					
LVDS0_CH3_P	A[32]	A32	LVDS0_CH3_P	IN			
LVDS0_CH3_N	A[33]	A33	LVDS0_CH3_N	IN			
LVDS0_CH0_P	A[34]	A34	LVDS0_CH0_P	IN			
LVDS0_CH0_N	A[35]	A35	LVDS0_CH0_N	IN			
LVDS0_CH2_P	A[36]	A36	LVDS0_CH2_P	IN			
LVDS0_CH2_N	A[37]	A37	LVDS0_CH2_N	IN			
HDMI1_CEC	A[38]	A38	HDMI_CEC	BI			
HDMI1_HPD	A[39]	A39	HDMI_HPD	BI			
AVS2/GP7_01/PMIC	A[40]	A40					
GND	A[41]	A41					
TDO_18	A[42]	A42	TDO_18			OUT	3E8> 6F3>
PRESETn_18	A[43]	A43	PRESET#_18			IN	6F3> 9C6>
NMIn_18	A[44]	A44	NMI_18			OUT	
TDI_18	A[45]	A45	TDI_18			IN	6F3> 3E8<
TRSTn_18	A[46]	A46	TRST#_18			IN	3E8< 6F3<
	A[47]	A47					
TCK_18	A[48]	A48	TCK_18			IN	6F3> 3E8<
AVS1/GP7_00/PMIC	A[49]	A49					
MSIOF1_TXD/LVDS_BKEN	A[50]	A50	MSIOF3_TXD		DU_DR7	OUT	4B4> 9D6<
GND	A[51]	A51					
MSIOF0_SCK	A[52]	A52	MSIOF1_SCK		VI1_HSYNC#		
USB22_ID2	A[53]	A53					
TMS_18	A[54]	A54	TMS_18				
USB31_VBUS	A[55]	A55					
USB30_VBUS	A[56]	A56					
GND	A[57]	A57					
MSIOF0_TXD	A[58]	A58	MSIOF1_TXD		VI1_CLKENB		
MSIOF0_RXD	A[59]	A59	MSIOF1_RXD		VI1_CLK		
GND	A[60]	A60					
USB31_ID	A[61]	A61					
USB30_ID	A[62]	A62					
SDIF1_SCK	A[63]	A63					
PCIE1_TX_P	A[64]	A64					
PCIE1_TX_M	A[65]	A65					
GND	A[66]	A66					
GP6_06/OTG_STAT2/MSIOF1_SS2	A[67]	A67	MSIOF3_SS2		DU_DG3	IN	4B4> 9D6<
PCIE0_TX_P	A[68]	A68	DIGRF_TX_N		4E7>		
PCIE0_TX_M	A[69]	A69	DIGRF_TX_P		4E7>	OUT	
GND	A[70]	A70				OUT	
HSCIF2_HRTSZ/SSI_SDATA8	A[71]	A71	HSCIF1_RTSZ		VI0_DATA4	OUT	4D4<
HSCIF2_HRX/SSI_SCK9	A[72]	A72	HSCIF1_RX		VI0_DATA7	OUT	9D9> 4D4<
HSCIF2_HTX/SSI_WS9	A[73]	A73	HSCIF1_TX		VI0_DATA6	OUT	9D9> 4D4<
HSCIF2_HCTSZ/SSI_SDATA7	A[74]	A74	HSCIF1_CTSZ		VI0_DATA5	OUT	9D9> 4D4<
USB31_OVC	A[75]	A75	PWM1		VI0_DATA9	OUT	4D4<
HSCIF0_HRTSZ	A[76]	A76	HSCIF0_RTSZ		DU_DR3	OUT	4B4> 9D6<
USB22_PWEN	A[77]	A77	GP1_19/AVB0_AVTP_MATCH			IN	9C8<
SDA0/SD3_PWEN	A[78]	A78	I2C_SDA0			OUT	3E1<> 6D5<>
MSIOF1_SCK/SSI_SCK4	A[79]	A79	MSIOF3_SCK		DU_EXVSYNC/DU_VSYNC	BI	9D6<>
GND	A[80]	A80					
USB31_DP	A[81]	A81					
USB31_DM	A[82]	A82					
USB30_DM	A[83]	A83					
USB30_DP	A[84]	A84					
D5.0V	A[85]	A85					
D5.0V	A[86]	A86					
EX_AUDIO_CLKA	A[87]	A87	AVB0_AVTP_CAPTURE			OUT	6C8<
PCIE0_CN_CLK_P	A[88]	A88	DIGRF_CLKOUT			OUT	4E7>
PCIE0_CN_CLK_M	A[89]	A89	DIGRF_CLKIN			IN	4E7<
GND	A[90]	A90					
D5.0V	A[91]	A91	VCC_D5.0V 5.0V				
D5.0V	A[92]	A92					
D5.0V	A[93]	A93					
D5.0V	A[94]	A94					
D5.0V	A[95]	A95					
USB31_PWEN	A[96]	A96	PWM2		VI0_DATA10	OUT	4D4<
USB30_OVC	A[97]	A97					
USB30_PWEN	A[98]	A98					
USB20_VBUS0	A[99]	A99					
GND	A[100]	A100					
USB20_ID0	A[101]	A101					
USB20_DM0	A[102]	A102					
USB20_DP0	A[103]	A103					
	A[104]	A104					
	A[105]	A105					
	A[106]	A106					
	A[107]	A107					
	A[108]	A108					
	A[109]	A109					
GND	A[110]	A110					

COMExpress440pin
CN3

GND	B[1]	B1					
AVB_PHY_INT	B[2]	B3	AVB0_PHY_INT			OUT	7C5>
AVB_RD0	B[3]	B4	AVB0_RD0			OUT	
AVB_RD1	B[4]	B5	AVB0_RD1			OUT	
AVB_RD2	B[5]	B6	AVB0_RD2			OUT	
AVB_RD3	B[6]	B7	AVB0_RD3			OUT	
AVB_RXC	B[7]	B8	AVB0_RXC			OUT	
AVB_RX_CTL	B[8]	B9	AVB0_RX_CTL			OUT	
AVB_TD0	B[9]	B10	AVB0_TD0			OUT	
AVB_TD1	B[10]	B11	AVB0_TD1			IN	
GND	B[11]	B12					
AVB_TD2	B[12]	B13	AVB0_TD2			IN	
AVB_TD3	B[13]	B14	AVB0_TD3			IN	
AVB_TXC	B[14]	B15	AVB0_TXC			IN	
AVB_TX_CTL	B[15]	B16	AVB0_TX_CTL			IN	
AVB_MDIO	B[16]	B17	AVB0_MDIO	BI	7B6>		
AVB_MDC/MSIOF2_SS2	B[17]	B18	AVB0_MDC	BI	7B6>		
	B[18]	B19	AVB0_PHY_RESETZ	OUT	7C5<		
MDT0/BSn/GP1_22/CAN1_TX	B[19]	B20	CANFD1_TX	IN	4C4> 9B6<		
WE1n/GP1_26/CAN1_RX	B[20]	B21	CANFD1_RX	OUT	9B6> 4C4<		
GND	B[21]	B22					
VI5_DATA7(ExD7)	B[22]	B23	ADC_IN7			IN	4D9>
VI5_DATA4(ExD4)	B[23]	B24	ADC_IN4			IN	4C9>
VI5_DATA5(ExD5)	B[24]	B25	ADC_IN5			IN	4C9>
VI5_DATA0(ExD0)	B[25]	B26	ADC_IN0			IN	4C9>
VI5_DATA3(ExD3)	B[26]	B27	ADC_IN3			IN	4C9>
VI5_DATA2(ExD2)	B[27]	B28	ADC_IN2			IN	4C9>
VI5_DATA1(ExD1)	B[28]	B29	ADC_IN1			IN	4C9>
GP4_14	B[29]	B30	GP0_15		DU_DB5	IN	4B4>
	B[30]	B31					
GND	B[31]	B32					
D1.8V (current tbd)	B[32]	B33					
D1.8V (current tbd)	B[33]	B34					
	B[34]	B35					
	B[35]	B36					
MSIOF1_SYNC/SSI_WS4	B[36]	B37	MSIOF3_SYNC		DU_EXODDF/DU_ODDF/DISP/CDE	BI	9E8<>
	B[37]	B38					
SCIF0_SCK/I2C2_SDA	B[38]	B39					
PWM3/IRQ2n/DU_DISP	B[39]	B40	GP2_04		VI0_DATA0	OUT	9D9> 4C4<
GND	B[40]	B41					
WE0n/GP1_25/CAN_CLK	B[41]	B42	GP0_18		DU_DOTCLKOUT		
SD3_PWR_SEL	B[42]	B43	GP0_14		DU_DB4	BI	4B4>
ExA20/PWM2	B[43]	B44	GP2_03		VI0_VSYNC#	BI	9E8<>
SD3_DAT1_V	B[44]	B45	MMC_D1		VI1_DATA3	OUT	4D4<
VI5_CLKENB(CS0n)	B[45]	B46					
SD3_PWR_EN	B[46]	B47	GP0_16		DU_DB6	IN	4B4>
ExA22/PWM0	B[47]	B48	PWM0		VI0_DATA8		
PRESET_SYSZ	B[48]	B49	PRESET_SYS#			BI	9B9<>
PRESET_CBZ(PRESETOUTn)	B[49]	B50	PRESETOUT#			IN	3E6< 9C6<
GND	B[50]	B51					
SD3_CLK_V	B[51]	B52	MMC_CLK		VI1_DATA6	OUT	4D4<
*GP2_00/IRQ0n	B[52]	B53	IRQ0#				
#SDA5	B[53]	B54				BI	3E3> 3E6<
#SCL5	B[54]	B55					
SDA1	B[55]	B56	I2C_SDA1				
GP5_25/MLB/IOEX_INT	B[56]	B57	GP0_09			BI	4E5<>
	B[57]	B58			DU_DG5	IN	4B4>
	B[58]	B59					
GND	B[59]	B60					
	B[60]	B61					
ExA25/PWM4	B[61]	B62	PWM4		VI0_FIELD	OUT	4E4>
MSIOF0_SS2/AUDIO_CLKC	B[62]	B63	MSIOF1_SYNC		VI1_VSYNC#	BI	4E4<
PCIE1_RX_P	B[63]	B64					
PCIE1_RX_M	B[64]	B65					
VI5_CLK(CS1n/A26)	B[65]	B66					
MSIOF0_SS2/AUDIO_CLKA	B[66]	B67	GP2_05		VI0_DATA1	OUT	9D9> 4C4<
PCIE0_RX_P	B[67]	B68	DIGRF_RX_N		4E7<		
PCIE0_RX_M	B[68]	B69	DIGRF_RX_P		4E7<	IN	
GND	B[69]	B70				IN	
SATA_RX_M	B[70]	B71					
SATA_RX_P	B[71]	B72					
SDIF2_SCK/SD2_VL	B[72]	B73	SCIF3_SCK				
GP5_06/TX1/HTX1	B[73]	B74	SCIF0_TX			BI	4D5<>
SATA_TX_P	B[74]	B75			DU_DB1	IN	9E5<>
SATA_TX_M	B[75]	B76					
GP5_05/OTG_STAT1/MSIOF1_SS1	B[76]	B77	MSIOF3_SS1		DU_DG2	IN	4B4> 9D6<
MSIOF1_RXD/SSI_SDATA4	B[77]	B78	MSIOF3_RXD		DU_DR6	OUT	4B4> 9D6<
GP5_05/RX1/HRX1	B[78]	B79	SCIF0_RX		DU_DB0	IN	9E5<>
GND	B[79]	B80					
HSCIF0_HCTSZ	B[80]	B81	HSCIF0_CTSZ		DU_DR4	IN	9D6<>
	B[81]	B82					
D3.3V	B[82]	B83					
D3.3V	B[83]	B84					
D3.3V	B[84]	B85					
D3.3V	B[85]	B86					
D3.3V	B[86]	B87					
HSCIF0_HTX	B[87]	B88	HSCIF0_TX		DU_DR5	IN	4B4> 9D6<
HSCIF0_HRX	B[88]	B89	HSCIF0_RX		DU_EXHSYNC/DU_HSYNC	BI	4C4<>
GND	B[89]	B90					
D5.0V	B[90]	B91					
D5.0V	B[91]	B92					
D5.0V	B[92]	B93					
D5.0V	B[93]	B94					
D5.0V	B[94]	B95					
D5.0V	B[95]	B96					
D5.0V	B[96]	B97					
SCIF0_CTSZ/SD1_VL	B[97]	B98	GP0_08		DU_DG4	IN	4B4>
MDT1/RDn/GP1_23/CAN0_TX	B[98]	B99	CANFD0_TX	IN	4C4> 9B6<		
RD/WR#/GP1_24/CANFD0_RX	B[99]	B100	CANFD0_RX	OUT	9B6> 4C4<		
GND	B[100]	B101					
D5.0V	B[101]	B102					
D5.0V	B[102]	B103					
D5.0V	B[103]	B104					
NC(VCC12V0)	B[104]	B105					
NC(VCC12V0)	B[105]	B106					
NC(VCC12V0)	B[106]	B107					
NC(VCC12V0)	B[107]	B108					
NC(VCC12V0)	B[108]	B109					
NC(VCC12V0)	B[109]	B109					
GND	B[110]	B110					

VCC_D1.8V 1.8V

VCC_D3.3V 3.3V

VCC_D5.0V 5.0V

COMExpress440pin
CN3

GND	C[1]	C1					
GND	C[2]	C2					
CSI2_DATAN2	C[3]	C3	CSI0_DATA2_N	IN	4E7>		
CSI2_DATAP2	C[4]	C4	CSI0_DATA2_P	IN	4E7>		
GND	C[5]	C5					
CSI2_DATAN3	C[6]	C6	CSI0_DATA3_N	IN	4E7>		
CSI2_DATAP3	C[7]	C7	CSI0_DATA3_P	IN	4E7>		
GND	C[8]	C8					
PMIC_GPIO7	C[9]	C9	PMIC_GPIO7	BI	3E3<>		
I2C4_SDA	C[10]	C10	I2C_SDA3		VI0_DATA2	OUT	4D4<
GND	C[11]	C11					
QSPI0_IO3	C[12]	C12	QSPI0_IO3	BI	8B5<>		
I2C4_SCL	C[13]	C13	I2C_SCL3		VI0_DATA3	OUT	4D4<
GND	C[14]	C14					
QSPI0_IO2	C[15]	C15	QSPI0_IO2	BI	8B5<>		
DDR0_1.8V (probe only)	C[16]	C16					
WE1n/GP1_26/CAN1_RX	C[17]	C17					
SCIF0_RTSZ/I2C2_SCL	C[18]	C18					
SCL0/SD3_VL	C[19]	C19	I2C_SCL0	BI	3E1<> 4E5<> 6D6<>		
BSMODE_18	C[20]	C20	BSMODE	OUT	3D7<		
GND	C[21]	C21					
GP6_16/OTG_EXTLPn	C[22]	C22	GP0_11		DU_DG7	IN	4B4>
VI4_DATA4(ExD12)	C[23]	C23					
GP6_04	C[24]	C24	GP0_10		DU_DG6	IN	4B4>
VI4_DATA5(ExD13)	C[25]	C25					
VI4_DATA2(ExD10)	C[26]	C26					
VI4_DATA3(ExD11)	C[27]	C27	RPC_RESETZ	OUT	8D3<		
VI4_DATA0(ExD8)	C[28]	C28	RPC_INTZ	IN	4D8> 8C7>		
VI4_DATA1(ExD9)	C[29]	C29	RPC_WPZ	IN	4D8>		
VI5_DATA6(ExD6)	C[30]	C30	ADC_IN6	IN	4D9>		
GND	C[31]	C31					
-	C[32]	C32					
EXT_LPO	C[33]	C33	CLK_EXTALR			OUT	3D6<
VI4_DATA6(ExD14)	C[34]	C34	QSPI1_IO0			BI	8D5<>
VI4_DATA7(ExD15)	C[35]	C35	QSPI1_IO1			BI	8D5<>
VI4_DATA8(ExA0)	C[36]	C36	QSPI1_SPCLK			OUT	8D5>
VI4_DATA9(ExA1)	C[37]	C37	QSPI1_SSL			OUT	8D5>
VI4_DATA10(ExA2)	C[38]	C38	QSPI1_IO2			BI	8D5<>
VI4_DATA11(ExA3)	C[39]	C39	QSPI1_IO3			BI	8D5<>
-	C[40]	C40					
GND	C[41]	C41					
VI4_DATA12(ExA4)	C[42]	C42					
VI4_DATA13(ExA5)	C[43]	C43					
PWM1	C[44]	C44	PWM3		VI0_DATA11	OUT	4D4<
FSCLKST	C[45]	C45	FSCLKST#			OUT	3D7<
SD0_CD	C[46]	C46	MMC_D4		VI1_DATA7	OUT	4D4<
SD0_SYS_TRG	C[47]	C47	MMC_D5		VI1_DATA8	OUT	4D4<
EX_AUDIO_CLKB	C[48]	C48	MMC_D6		VI1_DATA9	OUT	4D4<
SD0_WP	C[49]	C49	MMC_D7		VI1_DATA10	OUT	4D4<
SD3_DAT3_V	C[50]	C50	MMC_D3		VI1_DATA5	OUT	4D4<
GND	C[51]	C51					
VLDO_SD3 (1.6A)	C[52]	C52				3.3V	VCC_VDDQ_VIN0
VLDO_SD3 (1.6A)	C[53]	C53					
VLDO_SD3 (1.6A)	C[54]	C54				3.3V	VCC_VDDQ_DU
VLDO_SD3 (1.6A)	C[55]	C55					
VLDO_SD0 (probe only)	C[56]	C56					
SD3_DAT0_V	C[57]	C57	MMC_D0		VI1_DATA2	OUT	4D4<
SD3_CD_V	C[58]	C58	MMC_CD		VI1_FIELD	OUT	4E4>
SD3_DAT2_V	C[59]	C59	MMC_D2		VI1_DATA4	OUT	4D4<
GND	C[60]	C60					
CSI0_CLKP	C[61]	C61					
CSI0_CLKN	C[62]	C62					
SD3_WP_V	C[63]	C63	MMC_WP		VI1_DATA11	OUT	4D4<
SD3_CMD_V	C[64]	C64	MMC_CMD		VI1_DATA1	OUT	4D4<
CSI0_DATAP0	C[65]	C65					
CSI0_DATAN0	C[66]	C66					
MSIOF0_SS1	C[67]	C67	MSIOF1_SS1		VI1_DATA0	OUT	4D4<
CSI0_DATAP1	C[68]	C68					
HSCIF0_HSCK	C[69]	C69	HSCIF0_SCK		DU_DR2	IN	4B4> 9D6<
GND	C[70]	C70					
CSI0_DATAN1	C[71]	C71					
CSI0_DATAP2	C[72]	C72					
GND	C[73]	C73					
CSI0_DATAN2	C[74]	C74					
CSI0_DATAP3	C[75]	C75					
GND	C[76]	C76					
USB20_OVC	C[77]	C77					
CSI0_DATAN3	C[78]	C78					
USB20_PWEN	C[79]	C79					
GND	C[80]	C80					
VI5_FIELD(ExA11)	C[81]	C81					
DU_DR0(ExD8)	C[82]	C82					
DU_DR1(ExD9)	C[83]	C83					
GND	C[84]	C84					
DU_DR2(ExD10)	C[85]	C85					
DU_DR3(ExD11)	C[86]	C86					
GND	C[87]	C87					
DU_DR4(ExD12)	C[88]	C88					
DU_DR5(ExD13)	C[89]	C89					
GND	C[90]	C90					
DU_DR6(ExD14)	C[91]	C91					
DU_DR7(ExD15)	C[92]	C92					
GND	C[93]	C93					
DU_DB0(ExA0)	C[94]	C94					
DU_DB1(ExA1)	C[95]	C95					
GND	C[96]	C96					
DU_DB2(ExA2)	C[97]	C97					
DU_DB3(ExA3)	C[98]	C98					
DU_DB4(ExA4)	C[99]	C99					
GND	C[100]	C100					
DU_DB5(ExA5)	C[101]	C101					
VI5_HSYNCZ(ExA10)	C[102]	C102					
GND	C[103]	C103					
	C[104]	C104					
	C[105]	C105					
	C[106]	C106					
	C[107]	C107					
	C[108]	C108					
	C[109]	C109					
GND	C[110]	C110					

VCC_VDDQ_VIN0 3.3V

VCC_VDDQ_DU 3.3V

COMExpress440pin
CN3

GND	D[1]	D1					
GND	D[2]	D2					
PMIC_GPIO1	D[3]	D3	PMIC_GPIO9			BI	9E8<>
DDR1_1.8V (probe only)	D[4]	D4					
GND	D[5]	D5					
CLKOUT	D[6]	D6					
QSPI0_SPCLK	D[7]	D7	QSPI0_SPCLK			OUT	8B5>
GND	D[8]	D8					
QSPI0_SSL	D[9]	D9	QSPI0_SSL			OUT	8B5<
QSPI0_IO0	D[10]	D10	QSPI0_IO0			BI	8B5<>
GND	D[11]	D11					
QSPI0_IO1	D[12]	D12	QSPI0_IO1			BI	8B5<>
GP6_22	D[13]	D13	GP0_13		DU_DB3	IN	4B4>
GND	D[14]	D14					
-	D[15]	D15					
-	D[16]	D16					
-	D[17]	D17					
-	D[18]	D18					
-	D[19]	D19					
-	D[20]	D20					
GND	D[21]	D21					
VI5_DATA10(ExA14)	D[22]	D22					
VI5_DATA11(ExA15)	D[23]	D23					
HDMI1_SCL	D[24]	D24	HDMI_SCL			IN	
HDMI1_SDA	D[25]	D25	HDMI_SDA			BI	
HDMI1_TMDSDATA0_P	D[26]	D26	HDMI_TMDSDATA0_P			IN	6A9<>
HDMI1_TMDSDATA0_N	D[27]	D27	HDMI_TMDSDATA0_N			IN	6A9<
-	D[28]	D28					
HDMI1_TMDSDATA1_P	D[29]	D29	HDMI_TMDSDATA1_P				
HDMI1_TMDSDATA1_N	D[30]	D30	HDMI_TMDSDATA1_N				
GND	D[31]	D31					
HDMI1_TMDSDATA2_P	D[32]	D32	HDMI_TMDSDATA2_P				
HDMI1_TMDSDATA2_N	D[33]	D33	HDMI_TMDSDATA2_N				
-	D[34]	D34					
VI4_HSYNCZ(ExA18)	D[35]	D35	SCIF_CLK			OUT	4C5<
HDMI1_TMDSCLK_P	D[36]	D36	HDMI_TMDSCLK_P				
HDMI1_TMDSCLKN	D[37]	D37	HDMI_TMDSCLK_N				
VI4_VSYNCZ(ExA17)	D[38]	D38	AVB0_TXCREFCLK			OUT	7B6<
	D[39]	D39	DU_DOTCLKIN			OUT	4B5<
-	D[40]	D40					
GND	D[41]	D41					
-	D[42]	D42					
VI4_CLKENB(ExA19)	D[43]	D43	CLK_XTAL			OUT	3D6<
-	D[44]	D44					
-	D[45]	D45					
RD/WR#/GP1_24/CANDP0	D[46]	D46					
-	D[47]	D47					
-	D[48]	D48					
SCIF2_RXD_CN	D[49]	D49	SCIF3_RX		VI0_CLKENB	OUT	4D4> 9D9<
VI5_VSYNCZ(ExA9)	D[50]	D50					
GND	D[51]	D51					
ExA8	D[52]	D52	GP0_12		DU_DB2	IN	4B4>
VI4_FIELD(ExA16)	D[53]	D53					
GP2_10/MSIOF2_SS1/PRESET	D[54]	D54	AVB0_PHY_LINK			IN	7C5<>
VI5_DATA9(ExA13)	D[55]	D55					
USB22_OVC	D[56]	D56					
VI5_DATA8(ExA12)	D[57]	D57					
VI4_DATA14(ExA6)	D[58]	D58					
SCIF0_TX/SD0_PWEN	D[59]	D59					
GND	D[60]	D60					
VI4_DATA15(ExA7)	D[61]	D61					
USB31_TX_P	D[62]	D62					
USB31_TX_M	D[63]	D63					
SCIF2_TXD_CN	D[64]	D64	SCIF3_TX		VI0_HSYNC#	IN	4E4<> 9D9<
USB31_RX_P	D[65]	D65					
USB31_RX_M	D[66]	D66					
GND	D[67]	D67					
USB30_TX_P	D[68]	D68					
USB30_TX_M	D[69]	D69					
GND	D[70]	D70					
USB30_RX_P	D[71]	D71					
USB30_RX_M	D[72]	D72					
GND	D[73]	D73					
USB22_DP2	D[74]	D74					
USB22_DM2	D[75]	D75					
GND	D[76]	D76					
GP5_07/CTS1n/HCTS1n	D[77]	D77					
PCIE1_CN_CLK_P	D[78]	D78					
PCIE1_CN_CLK_M	D[79]	D79					
GND	D[80]	D80					
GP5_08/RTS1n/HRTS1n	D[81]	D81					
DU_DB6	D[82]	D82					
DU_DB7	D[83]	D83					
GND	D[84]	D84					
DU_DG0	D[85]	D85					
	D[86]	D86					
GND	D[87]	D87					
DU_DG2	D[88]	D88					
DU_DG3	D[89]	D89					
GND	D[90]	D90					
DU_DG4	D[91]	D91					
DU_DG5	D[92]	D92					
GND	D[93]	D93					
DU_DG6	D[94]	D94					
DU_DG7	D[95]	D95					
GND	D[96]	D96					
ExA24/DU_EXHSYNC_DU_HSYNC	D[97]	D97					
ExA23/DU_EXVSYNC_DU_VSYNC	D[98]	D98					
DU_DISP/IRQ1n	D[99]	D99					
GND	D[100]	D100					
EX_WAIT0n/IDU_DOTCLKOUT0	D[101]	D101					
GP5_23/MLB/SCL1	D[102]	D102	I2C_SCL1			BI	4E5<>
	D[103]	D103					
	D[104]	D104					
	D[105]	D105					
	D[106]	D106					
	D[107]	D107					
	D[108]	D108					
	D[109]	D109					
GND	D[110]	D110					

VCC_D1.2V 1.2V

TP30 GND-Testpoint
TP31 GND-Testpoint
TP32 GND-Testpoint
TP33 GND-Testpoint
TP34 Fiducial_1mm
TP35 Fiducial_1mm
TP36 Fiducial_1mm
TP37 Fiducial_1mm

RENESAS Electronics Europe GmbH

Title: y_ask_rcar_v3m_ws10
Module I/F (440pin like ComExpress type6)

Size	Document Number		
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