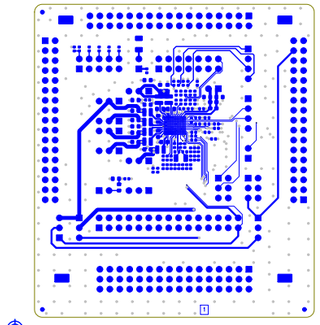
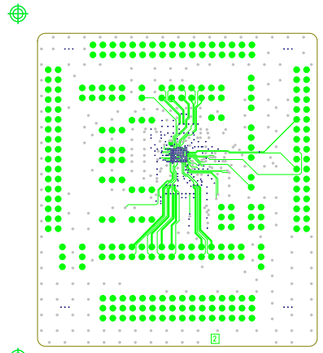
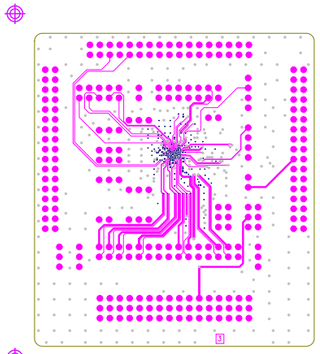


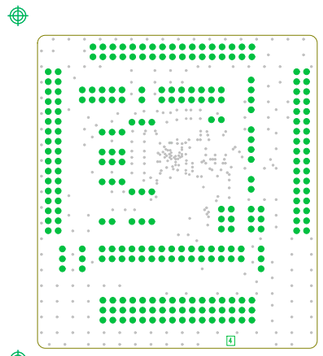
dialog SEMICONDUCTOR	PROJECT DA9066 EVAL. DB
DRAWING NUMBER	183-05-A_C1
LAYER	TOP SIDE TRACK



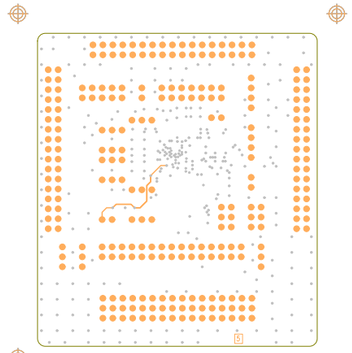
dialog SEMICONDUCTOR	PROJECT DA9066 EVAL. DB
DRAWING NUMBER	183-05-A_C2
LAYER	INNER LAYER 2



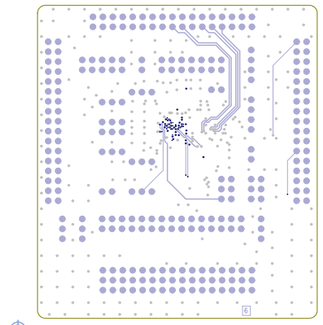
dialog SEMICONDUCTOR	PROJECT DA9066 EVAL. DB
DRAWING NUMBER	183-05-A_C3
LAYER	INNER LAYER 3



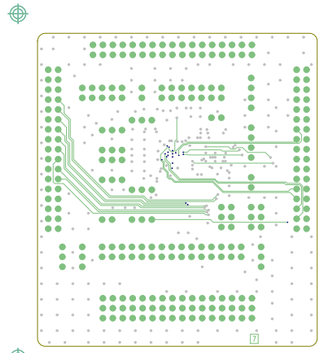
dialog SEMICONDUCTOR	PROJECT DA9066 EVAL. DB
DRAWING NUMBER	183-05-A_C4
LAYER	BOTTOM SIDE TRACK



dialog SEMICONDUCTOR	PROJECT DA9066 EVAL. DB
DRAWING NUMBER	183-05-A_
LAYER	



dialog SEMICONDUCTOR	PROJECT DA9066 EVAL. DB
DRAWING NUMBER	183-05-A_
LAYER	



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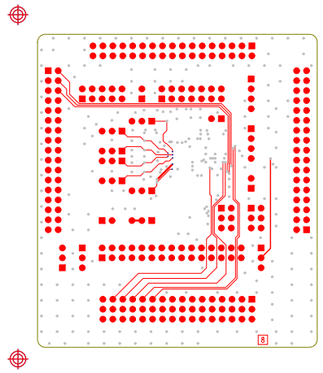
DRAWING NUMBER	183-05-A_
LAYER	



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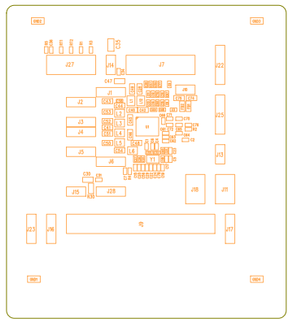
DRAWING NUMBER	183-05-A_
LAYER	



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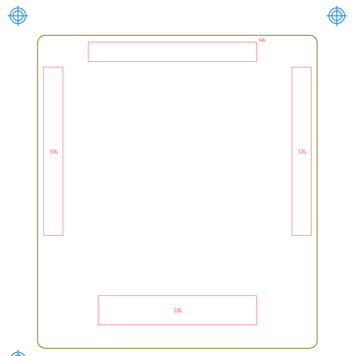
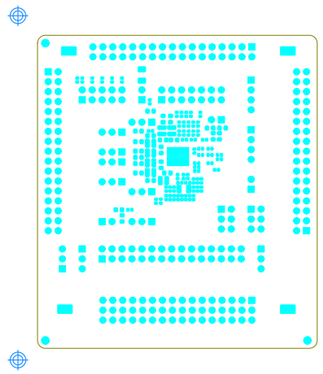
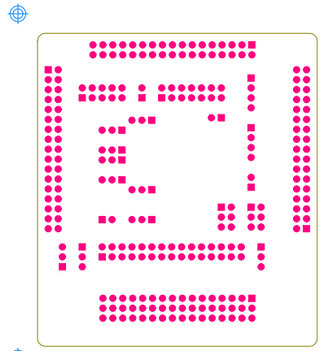
DRAWING NUMBER	183-05-A_
LAYER	



dialog SEMICONDUCTOR	PROJECT DA9066 EVAL. DB
DRAWING NUMBER	183-05-A_
LAYER	



dialog SEMICONDUCTOR	PROJECT DA9066 EVAL. DB
DRAWING NUMBER	183-05-A_
LAYER	



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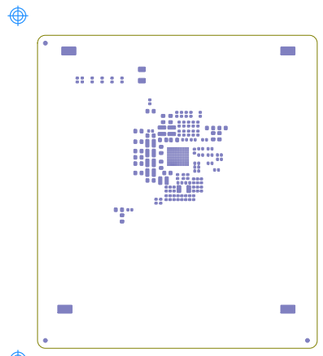
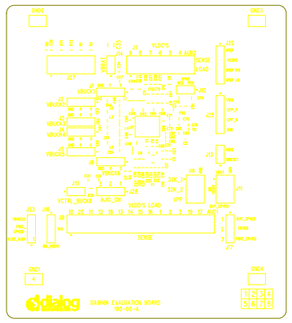
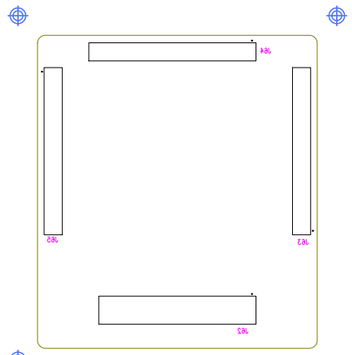
DRAWING NUMBER	183-05-A_
LAYER	



dialog SEMICONDUCTOR	PROJECT DA9066 EVAL. DB
DRAWING NUMBER	183-05-A_
LAYER	



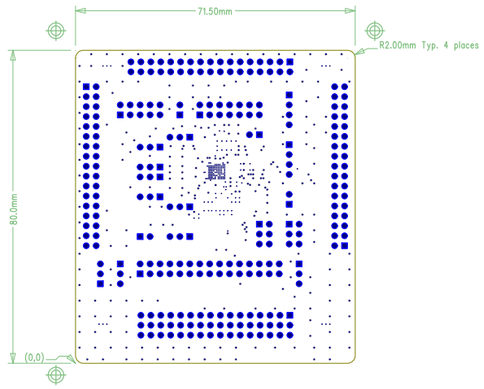
dialog SEMICONDUCTOR	PROJECT DA9066 EVAL. DB
DRAWING NUMBER	183-05-A_TS
LAYER	TOP SILKSCREEN



dialog SEMICONDUCTOR	PROJECT DA9066 EVAL. DB
DRAWING NUMBER	183-05-A_BS
LAYER	BOTTOM SILKSCREEN

IF IN DOUBT ASK!

NOTE:
BOARD FINISH TO INCORPORATE
COPPER FILLED FLAT PADS



MC

MANUFACTURE DETAIL

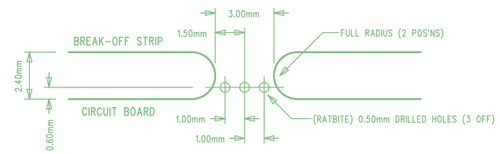
PREFERRED PANELISATION REQUIREMENTS

REFER TO THE PANEL DRAWING IF SUPPLIED OTHERWISE USE DETAILS BELOW

PRINTED CIRCUIT BOARDS THAT REQUIRE PANELISATION	
01	ANY PCB THAT DOES NOT HAVE A 5mm CLEARANCE FROM PCB EDGE TO COPPER/COMPONENTS ALONG THE LONGEST PARALLEL EDGES
02	ANY 'ODD' SHAPE PCB e.g. ROUND
PANEL SIZE, WASTE EDGE (BORDER) AND WEBBING	
01	PREFERRED PANEL SIZE TO BE 300mm X 230mm (MAXIMUM 450mm SQUARE)
02	PANEL BORDER TO BE 10mm ON ALL SIDES, FULLY CROSS HATCHED IN COPPER ON BOTH SIDES
03	BOARD EDGE TO BOARD EDGE INTERNAL WEBBING TO BE 10mm
TOOLING HOLES	
01	ADD 3 TOOLING HOLES 2.5mm +/-0.05 DIA. TO PANEL BORDER 5mm FROM BORDER EDGE
FIDUCIALS	
01	ADD 3 FIDUCIALS ON BOTH SIDES (1mm DIA./2mm DIA. CLEARANCE) 5mm FROM PANEL EDGE
RATBITES (FOR REFERENCE SEE ROUTING DETAIL BELOW)	
01	ADD RATBITES IN SAFE AREAS AWAY FROM TRACKS, TOOLING HOLES, SM PADS, VIAS, TEST PADS, GROUND PLANES, VITAL SILKSCREEN, THROUGH HOLES, OVERHANGING COMPONENTS ETC.
02	USE LOCATIONS SHOWN BY '**' IF PRESENT
03	THERE MUST BE SUFFICIENT RATBITES TO ENSURE PCB STABILITY
04	THE SPACING BETWEEN RATBITES SHOULD BE BETWEEN 40mm TO 50mm

PREFERRED ROUTING / V-SCORING REQUIREMENTS

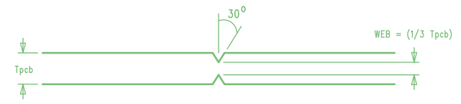
ROUTING	REQUIRED
01	USE A 2.40mm (+/-0.1mm) ROUT



V-SCORING	NOT REQUIRED

WHEN V-SCORING IS APPLIED TO THE BOARD AS A METHOD OF REMOVING THE BREAK-OFF STRIPS THE FOLLOWING RULES ARE TO BE APPLIED

01	SOLDER MASK TO EDGE CLEARANCE = 0.50mm (20thou)
02	COPPER TO EDGE CLEARANCE (ON ALL LAYERS) = 1.00mm (40thou)
03	SCORE ANGLE = 30 deg
04	REMAINING WEB AFTER SCORING IS AS ONE THIRD OF THE PCB NOMINAL THICKNESS



NOTES

01	BOARD TO BE MANUFACTURED TO IPC-A-600 CLASS 2	
02	BOARD IS TO MEET UL94V0 APPROVAL	
03	ALL BOARD'S MUST BE 100% TESTED FOR ELECTRICAL CONTINUITY AND ISOLATION	
04	NO REPAIRS MAY BE PERFORMED ON ANY IMPEDANCE CRITICAL TRACKS (WHERE APPLICABLE)	
05	ALIGNMENT OF ALL LAYERS TO BE SUCH THAT NO BREAKOUT OCCURS	
06	SUPPLIER'S UL IDENTIFICATION MARK, FLAMMABILITY RATING AND DATECODE MUST BE APPLIED TO THE BOARD	
07	VARIATION IN TRACK WIDTH AND GAP TO MEET IMPEDANCE REQUIREMENTS ARE PERMISSABLE, SO LONG AS THESE ARE MINIMAL, AND THE OVERALL BOARD THICKNESS IS NOT COMPROMISED.	
08	MATERIAL TO BE RoHS COMPLIANT HIGH Tg FR4, (e.g. VT47, TU768 or equivalent)	
09	BOW AND TWIST TO BE NO GREATER THAN 0.75% ACROSS DIAGONALS	
10	NON-FUNCTIONAL PADS MAY BE REMOVED FROM INTERNAL LAYERS (WHERE APPLICABLE)	
11	ALL STUBS MAY BE REMOVED	
12	REMOVE SILKSCREEN FROM EXPOSED COPPER (WHERE APPLICABLE)	
13	CHECK BUILD ORDER AGAINST PLOTS	
14	ALL DIMENSIONS IN mm (UNLESS STATED)	
15	FINISHED BOARD THICKNESS	1.60mm +/-10%
16	SURFACE FINISH	ELECTROLESS NICKEL/IMMERSION GOLD
17	SOLDER RESIST	BLUE PHOTO-IMAGABLE
18	SILKSCREEN COLOUR	WHITE
19	MINIMUM TRACK WIDTH	0.06mm
20	MINIMUM GAP	0.06mm
21	MINIMUM P.T.H. PAD SIZE	0.20mm
22	MINIMUM PITCH OF SURFACE MOUNT PADS	0.40mm
23	No. TOP SIDE SURFACE MOUNT PADS	363
24	No. BOTTOM SIDE SURFACE MOUNT PADS	0

ADDITIONAL NOTES

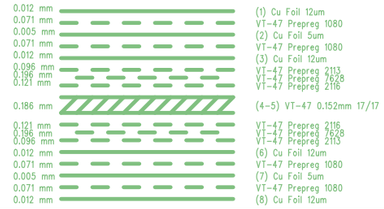
PCB LAYER	MANUFACTURING DETAIL	GERBER FILES
	TOP SILKSCREEN	183-05-A_TS.GER
	TOP RESIST	183-05-A_TR.GER
LAYER 1	TOP SIDE TRACK	183-05-A_C1.GER
LAYER 2	INNER LAYER 2	183-05-A_C2.GER
LAYER 3	INNER LAYER 3	183-05-A_C3.GER
LAYER 4	GROUND LAYER 4	183-05-A_C4.GER
LAYER 5	POWER LAYER 5	183-05-A_C5.GER
LAYER 6	INNER LAYER 6	183-05-A_C6.GER
LAYER 7	INNER LAYER 7	183-05-A_C7.GER
LAYER 8	BOTTOM SIDE TRACK	183-05-A_C8.GER
	BOTTOM RESIST	183-05-A_BR.GER
	BOTTOM SILKSCREEN	183-05-A_BS.GER
	CNC DRILL FILE (LAYERS 1-2)	183-05-A_L1-2.DRT
	CNC DRILL TOOLING (LAYERS 1-2)	183-05-A_L1-2.TOL
	CNC DRILL FILE (LAYERS 2-3)	183-05-A_L2-3.DRT
	CNC DRILL TOOLING (LAYERS 2-3)	183-05-A_L2-3.TOL
	CNC DRILL FILE (LAYERS 6-7)	183-05-A_L6-7.DRT
	CNC DRILL TOOLING (LAYERS 6-7)	183-05-A_L6-7.TOL
	CNC DRILL FILE (LAYERS 7-8)	183-05-A_L7-8.DRT
	CNC DRILL TOOLING (LAYERS 7-8)	183-05-A_L7-8.TOL
	CNC DRILL FILE (LAYERS 3-6)	183-05-A_L3-6.DRT
	CNC DRILL TOOLING (LAYERS 3-6)	183-05-A_L3-6.TOL
	CNC DRILL FILE (PLATED/NON-PLATED THROUGH HOLE)	183-05-A.DRT
	CNC DRILL TOOLING (PLATED/NON-PLATED THR'H HOLE)	183-05-A.TOL
	MANUFACTURE DETAIL	183-05-A_MC.GER

DRILL DETAIL NOTES		
ALL PLATED HOLES ARE FINISHED SIZES WITH +/-0.075mm TOLERANCE		
ALL NON-PLATED HOLES ARE FINISHED SIZES WITH +/-0.050mm TOLERANCE		
ALL VIAS ARE DRILLED SIZES WITH +0/-DRILL TOLERANCE		
TOTAL PLATED HOLE QTY	912	
TOTAL NON-PLATED HOLE QTY	0	

BOARD STACK

LAYER/ LAYER TYPE		COPPER WEIGHT
01	MIXED	305g/m
02	MIXED	152g/m
03	MIXED	152g/m
04	GROUND	152g/m
05	POWER	152g/m
06	MIXED	152g/m
07	MIXED	152g/m
08	MIXED	305g/m

TYP. BOARD CONSTUCTION



Pb Free

COMPANY CONFIDENTIAL

TOLERANCES UNLESS OTHERWISE STATED
0 PLACE DECIMALS +/- 1
1 PLACE DECIMALS +/- 0.5
2 PLACE DECIMALS +/- 0.1

DRAWN BY	DATE
IT/RJ	19/02/2013
CHK'D BY	DATE

DIALOG SEMICONDUCTOR UK LTD
DELTA 200, WELTON ROAD
SWINDON, WILTS.
SN5 7XB

REV A

TITLE MANUFACTURE DETAIL
DA9066 EVALUATION BOARD

DRAWING NUMBER
183-05-A