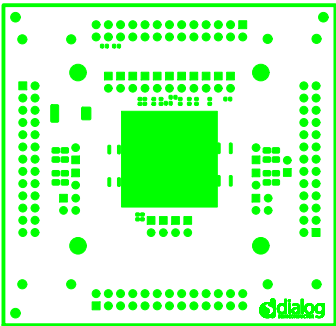

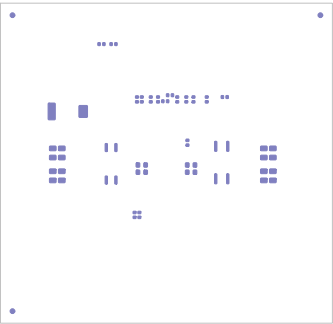

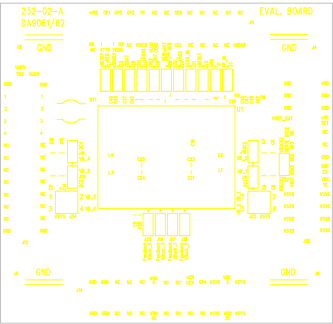
	PROJECT NUCLEUS-Eval. Board
DRAWING NUMBER	232-02-A-TA
LAYER	TOP ASSEMBLY DRAWING




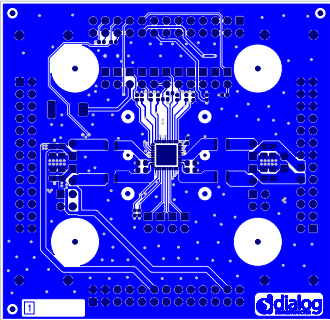
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	NUCLEUS-Eval. Board
DRAWING NUMBER	232-02-A-TR
LAYER	TOP SOLDER RESIST




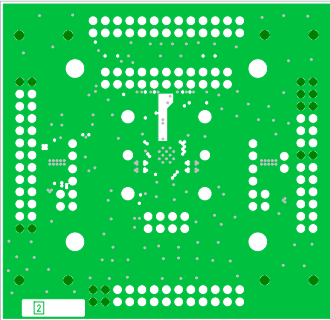
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DRAWING NUMBER	232-02-A-TP
LAYER	TOP SOLDER PASTE




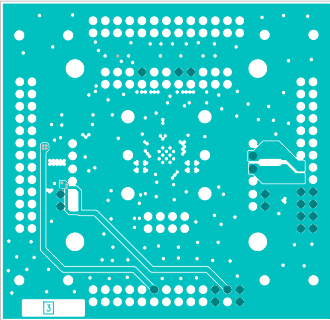
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DRAWING NUMBER	232-02-A-TS
LAYER	TOP SILKSCREEN



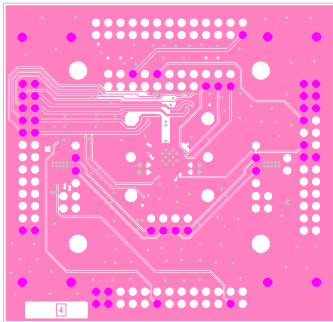
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DRAWING NUMBER		NUCLEUS-Eval. Board
LAYER		232-02-A-C1
		TOP SIDE TRACK



	PROJECT
	NUCLEUS-Eval. Board
	DRAWING NUMBER 232-02-A-C2
LAYER	INNER LAYER 2

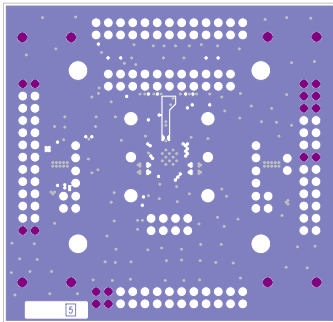



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DRAWING NUMBER		NUCLEUS-Eval. Board
LAYER		232-02-A-C3
		INNER LAYER 3

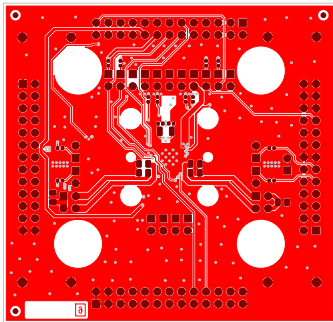



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		NUCLEUS-Eval. Board
DRAWING NUMBER	232-02-A-C4	
LAYER	INNER LAYER 4	

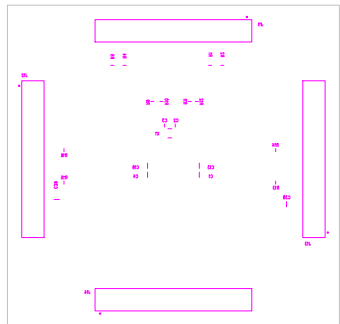




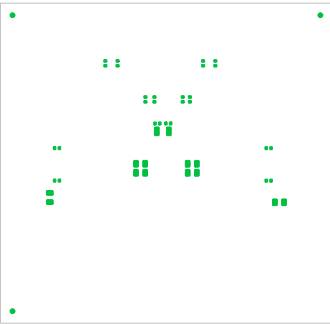
		PROJECT
DRAWING NUMBER		NUCLEUS-Eval. Board
232-02-A-C5		
LAYER	INNER LAYER 5	




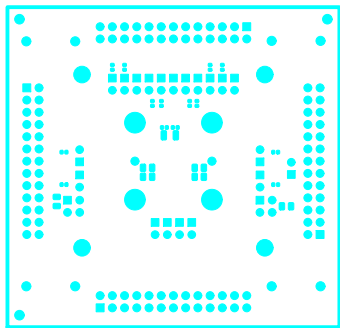
	PROJECT
	NUCLEUS-Eval. Board
	DRAWING NUMBER 232-02-A-C6
LAYER	BOTTOM SIDE TRACK



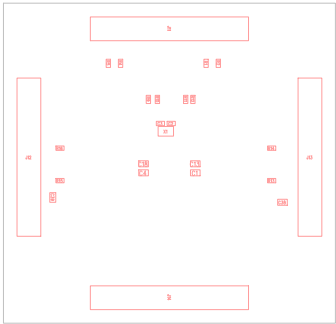
	PROJECT NUCLEUS-Eval. Board
DRAWING NUMBER	232-02-A-BS
LAYER	BOTTOM SILKSCREEN



		PROJECT
DRAWING NUMBER		NUCLEUS-Eval. Board
232-02-A-BP		
LAYER	BOTTOM	SOLDER PASTE



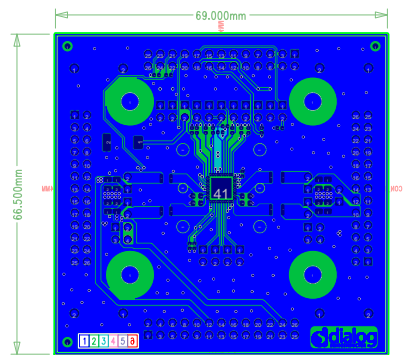
	PROJECT NUCLEUS-Eval. Board
DRAWING NUMBER	232-02-A-BR
LAYER	BOTTOM SOLDER RESIST



	PROJECT
	NUCLEUS-Eval. Board
	DRAWING NUMBER 232-02-A-BA
LAYER	BOTTOM ASSEMBLY DRAWING



IF IN DOUBT ASK!



Finished Thickness	Layer	Discription
0.0200 mm	(SM)	SunChemical (HF Green) XV501T Screen CAWN2619
0.0470 mm	(1)	Cu Cu Foil 12µm+23µm
0.0565 mm		R-1650V (x2) PP 2 x 1080 (0074)
0.0350 mm	(2)	Cu Cu 18µm
0.2675 mm		R-1755V CORE 0500
0.0150 mm	(3)	Cu Cu 18µm
0.7100 mm		R-1650V (x2) PP 2 x 1080 (0074)
0.0150 mm	(4)	Cu Cu 18µm
0.2675 mm		R-1755V CORE 0500
0.0350 mm	(5)	Cu Cu 18µm
0.0565 mm		R-1650V (x2) PP 2 x 1080 (0074)
0.0470 mm	(6)	Cu Cu Foil 12µm+23µm
0.0200 mm	(SM)	SunChemical (HF Green) XV501T Screen CAWN2619

DRILL DETAIL NOTES		
ALL PLATED HOLES ARE FINISHED SIZES WITH $\pm 0.075\text{mm}$ TOLERANCE		
ALL NON-PLATED HOLES ARE FINISHED SIZES WITH $\pm 0.050\text{mm}$ TOLERANCE		
ALL VIAS ARE DRILLED SIZES WITH $\pm 0$ -DRILL TOLERANCE		
TOTAL PLATED HOLE QTY	170	
TOTAL NON-PLATED HOLE QTY	4	

TOLERANCES UNLESS OTHERWISE STATED  
0 PLACE DECIMALS  $\pm 1$   
1 PLACE DECIMALS  $\pm 0.5$   
2 PLACE DECIMALS  $\pm 0.1$

DRAWN BY  
Daniel Ferreira

CHK'D BY  
Klaus Handke

DATE  
16-10-2014

DATE  
16-10-2014

DIALOG SEMICONDUCTOR GmbH  
Neue Straße 95  
73230 Kirchheim Unter Teck (Nabern)  
Deutschland

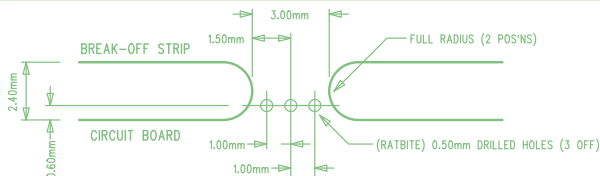
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TITLE      MANUFACTURE DETAIL  
             NUCLEUS Evaluation Board

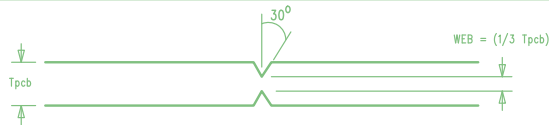
DRAWING NUMBER  
232-02-A













PREFERRED PANELISATION REQUIREMENTS	
REFER TO THE PANEL DRAWING IF SUPPLIED OTHERWISE USE DETAILS BELOW	
PRINTED CIRCUIT BOARDS THAT REQUIRE PANELISATION	
01	ANY PCB THAT DOES NOT HAVE A 5mm CLEARANCE FROM PCB EDGE TO COPPER/COMPONENTS ALONG THE LONGEST PARALLEL EDGES
02	ANY 'ODD' SHAPE PCB e.g. ROUND
PANEL SIZE, WASTE EDGE (BORDER) AND WEBBING	
01	ASSEMBLY PANEL TO BE A 2X2, 4 UP ARRAY
02	PANEL BORDER TO BE 10mm ON ALL SIDES, FULLY CROSS HATCHED IN COPPER ON BOTH SIDES
03	BOARD EDGE TO BOARD EDGE INTERNAL WEBBING TO BE 10mm
04	MAXIMUM PANEL SIZE NOT TO EXCEED 380mm X 440mm
TOOLING HOLES	
01	ADD 3 TOOLING HOLES 2.5mm +/-0.05 DIA. TO PANEL BORDER 5mm FROM BORDER EDGE
FIDUCIALS	
01	ADD 3 FIDUCIALS ON BOTH SIDES (1mm DIA./2mm DIA. CLEARANCE) 5mm FROM PANEL EDGE
BREAKOUTS (FOR REFERENCE SEE ROUTING DETAIL BELOW)	
01	ADD BREAKOUTS IN SAFE AREAS AWAY FROM TRACKS, TOOLING HOLES, SM PADS, VIAS, TEST PADS, GROUND PLANES, VITAL SILKSCREEN, THROUGH HOLES, OVERHANGING COMPONENTS ETC.
02	USE LOCATIONS SHOWN BY '+' IF PRESENT
03	AT LEAST TWO BREAKOUTS MUST BE ADDED ALONG THE EDGE OF A CIRCUIT IF GREATER THAN 75MM IN LENGTH
04	AT LEAST ONE BREAKOUT MUST BE ADDED ALONG THE EDGE OF A CIRCUIT IF LESS THAN 75MM IN LENGTH
05	THE SPACING BETWEEN BREAKOUTS SHOULD BE BETWEEN 40mm TO 50mm
06	BREAKOUTS TO BE POSITIONED AT LEAST 12MM FROM CIRCUIT CORNER TO ALLOW CUTOUT ACCESS
07	STEPPED GERBERS MUST BE SENT TO THE PCB DESIGNER FOR VERIFICATION BEFORE MANUFACTURE COMMENCES
08	IF ANY OF THIS SECTION CANNOT BE ADHERED TO THEN PLEASE CONSULT THE PCB DESIGNER

PREFERRED ROUTING / V-SCORING REQUIREMENTS	
ROUTING	REQUIRED
01	USE A 2.40mm (+/-0.1mm) ROUT



V-SCORING		NOT REQUIRED
WHEN V-SCORING IS APPLIED TO THE BOARD AS A METHOD OF REMOVING THE BREAK-OFF STRIPS THE FOLLOWING RULES ARE TO BE APPLIED		
01	SOLDER MASK TO EDGE CLEARANCE = 0.50mm (20thou)	
02	COPPER TO EDGE CLEARANCE (ON ALL LAYERS) = 1.00mm (40thou)	
03	SCORE ANGLE = 30 deg	
04	REMAINING WEB AFTER SCORING IS AS ONE THIRD OF THE PCB NOMINAL THICKNESS	



LAYER/ LAYER TYPE	BOARD STACK	VIA 0.4mm/0.2mm	COPPER WEIGHT
1			1
2			2
3			3
01 MIXED			4
02 MIXED			5
03 GND			6
04 PWR			7
05 MIXED			8
06 MIXED			9
10			10
11			11
12			12

[illegible]

NOTES

01	BOARD TO BE MANUFACTURED TO IPC-A-600 CLASS 2	
02	BOARD IS TO MEET UL94V0 APPROVAL	
03	ALL BOARD'S MUST BE 100% TESTED FOR ELECTRICAL CONTINUITY AND ISOLATION	
04	NO REPAIRS MAY BE PERFORMED ON ANY IMPEDANCE CRITICAL TRACKS (WHERE APPLICABLE)	
05	ALIGNMENT OF ALL LAYERS TO BE SUCH THAT NO BREAKOUT OCCURS	
06	SUPPLIER'S UL IDENTIFICATION MARK, FLAMMABILITY RATING AND DATECODE MUST BE APPLIED TO THE BOARD – BOTTOM SIDE	
07	VARIATION IN TRACK WIDTH AND GAP TO MEET IMPEDANCE REQUIREMENTS ARE PERMISSIBLE, SO LONG AS THEY ARE MINIMAL, AND THE OVERALL BOARD THICKNESS IS NOT COMPROMISED.	
08	MATERIAL– ROHS COMPLIANT HIGH Tg FR4 (VT47, TU768, 370HR, R1755V/1650V OR EQUIVALENT)	
09	BOW AND TWIST TO BE NO GREATER THAN 0.75% ACROSS DIAGONALS	
10	NON-FUNCTIONAL PADS MAY BE REMOVED FROM INTERNAL LAYERS (WHERE APPLICABLE)	
11	ALL STUBS MAY BE REMOVED	
12	SILKSCREEN SHOULD NOT BE ALTERED WITHOUT THE PCB DESIGNERS APPROVAL	
13	CHECK BUILD ORDER AGAINST PLOTS	
14	ALL DIMENSIONS IN mm (UNLESS STATED)	
15	FINISHED BOARD THICKNESS	1.60mm +/-10%
16	SURFACE FINISH	ELECTROLESS NICKEL/IMMERSION GOLD
17	SOLDER RESIST	GREEN PHOTO-IMAGABLE
18	SILKSCREEN COLOUR	WHITE
19	MINIMUM TRACK WIDTH	0.20mm
20	MINIMUM GAP	0.15mm
21	MINIMUM P.T.H. PAD SIZE	0.4mm
22	MINIMUM PITCH OF SURFACE MOUNT PADS	0.50mm
23	No. TOP SIDE SURFACE MOUNT PADS	110
24	No. BOTTOM SIDE SURFACE MOUNT PADS	45

ADDITIONAL NOTES	
25	VIAS UNDER U1 EXPOSED PAD NEED TO BE VIA PLUG TECHNOLOGY
26	SOCKET ALIGNMENT PINS, SHOULD BE DONE WITH SECOND STAGE DRILLING
27	VIAS UNDER (C1, C4, C13, C18, C21, C23, C24, C25) PADS SHOULD BE COPPER-FILLED
28	.

PCB LAYER	MANUFACTURING DETAIL	GERBER FILES
	TOP SILKSREEN	232-02-A_TS.GER
	TOP RESIST	232-02-A_TR.GER
LAYER 1	TOP SIDE TRACK	232-02-A_C1.GER
LAYER 2	INNER LAYER 2	232-02-A_C2.GER
LAYER 3	INNER LAYER 3	232-02-A_C3.GER
LAYER 4	INNER LAYER 4	232-02-A_C4.GER
LAYER 5	INNER LAYER 5	232-02-A_C5.GER
LAYER 6	BOTTOM SIDE TRACK	232-02-A_C6.GER

	1	2
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6

	BOTTOM RESIST	232-02-A_BR.GER
	BOTTOM SILKSCREEN	232-02-A_BS.GER
	MANUFACTURE DETAIL	232-02-A_MC.GER

CNC DRILL FILE (PLATED/NON-PLATED THROUGH HOLE)	232-02-A.DRT
CNC DRILL TOOLING (PLATED/NON-PLATED THR'H HOLE)	232-02-A.REP

[illegible]