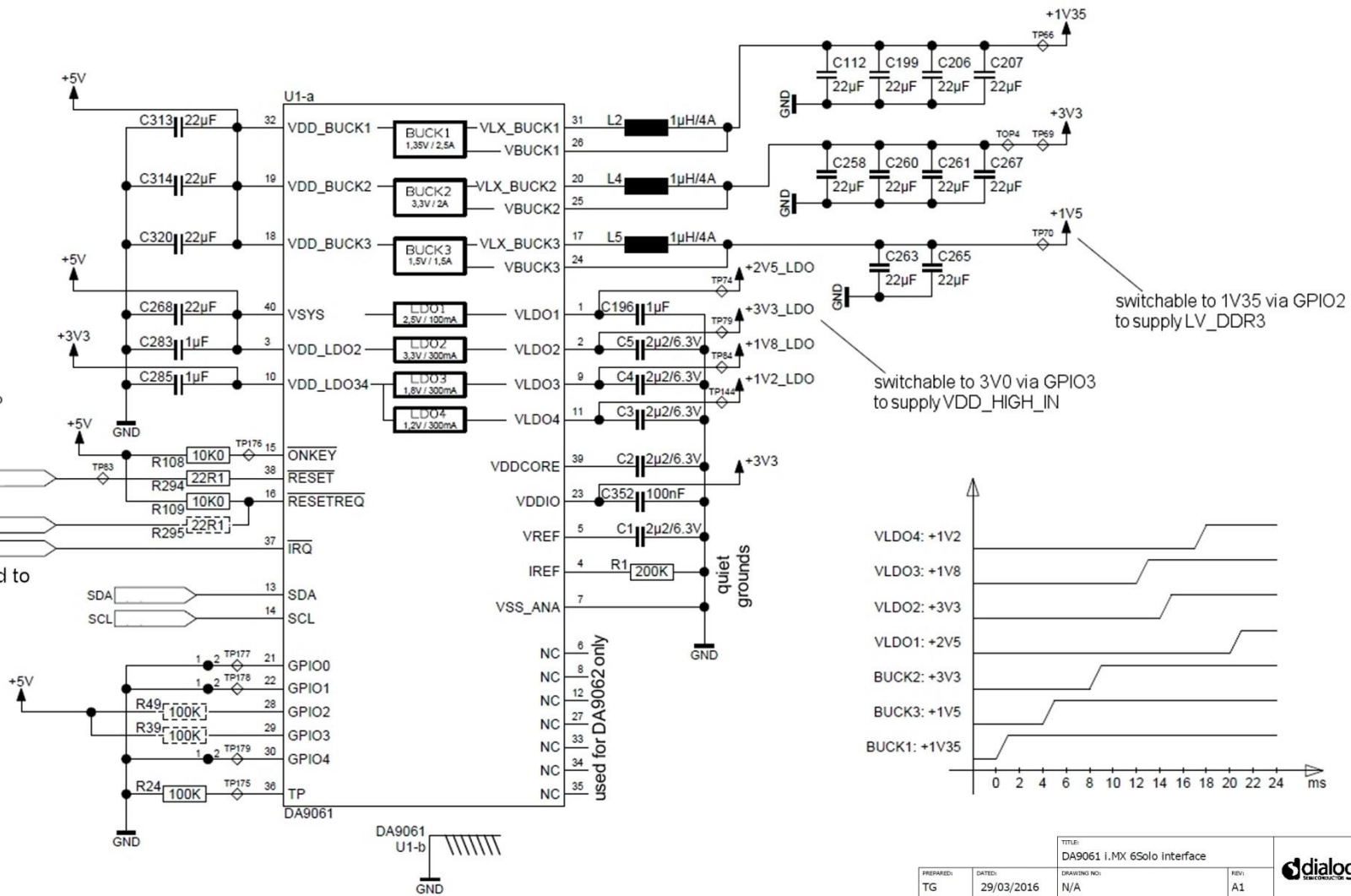


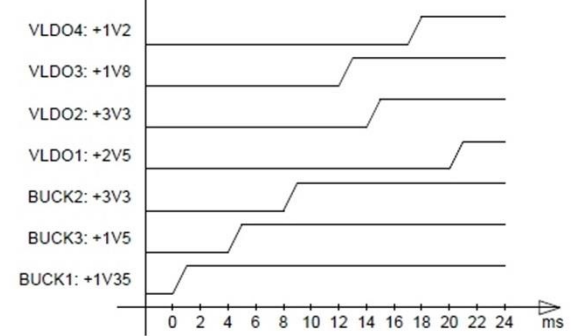
nRESET (open drain) has a 100 ms delay to ensure VDD\_SOC\_CAP and VDD\_ARM\_CAP are stable

nPMIC\_INT connected to i.MX 6S pin A[19].



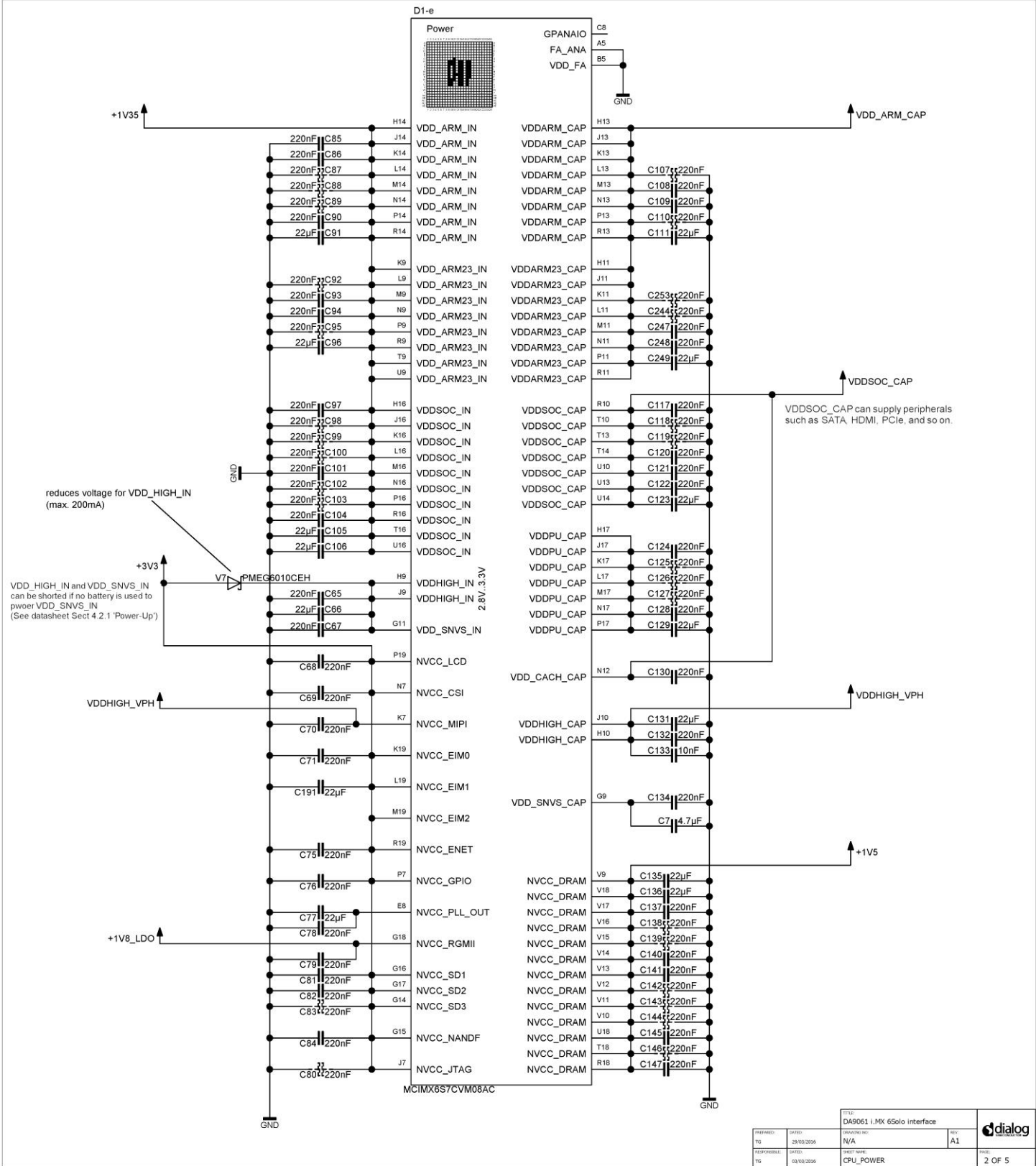
switchable to 3V0 via GPIO3 to supply VDD\_HIGH\_IN

switchable to 1V35 via GPIO2 to supply LV\_DDR3



PREPARED:		DATED:		DRAWING NO.:		REV.:	
TG		29/03/2016		N/A		A1	
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TG		03/03/2016		DA9061			1 OF 5

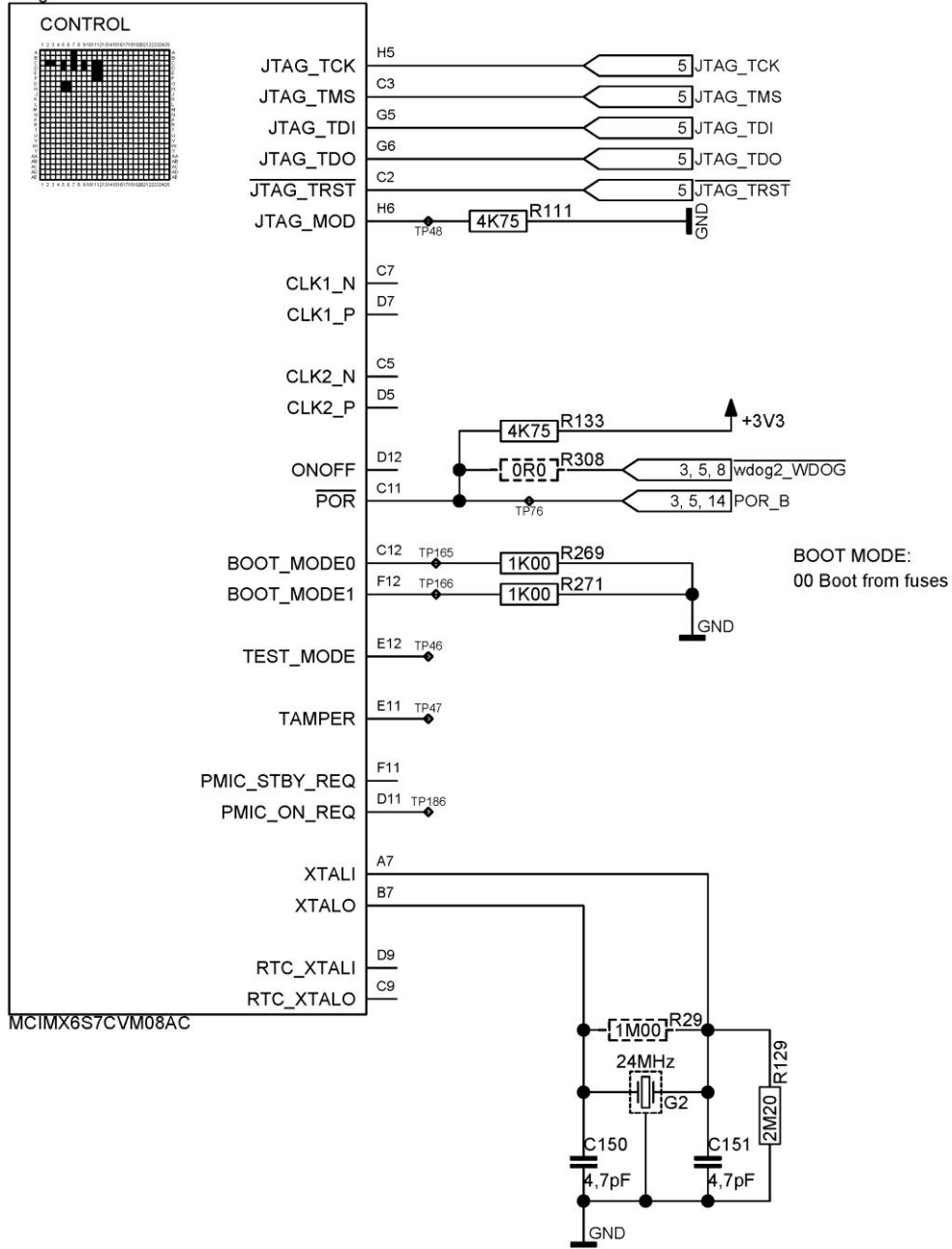




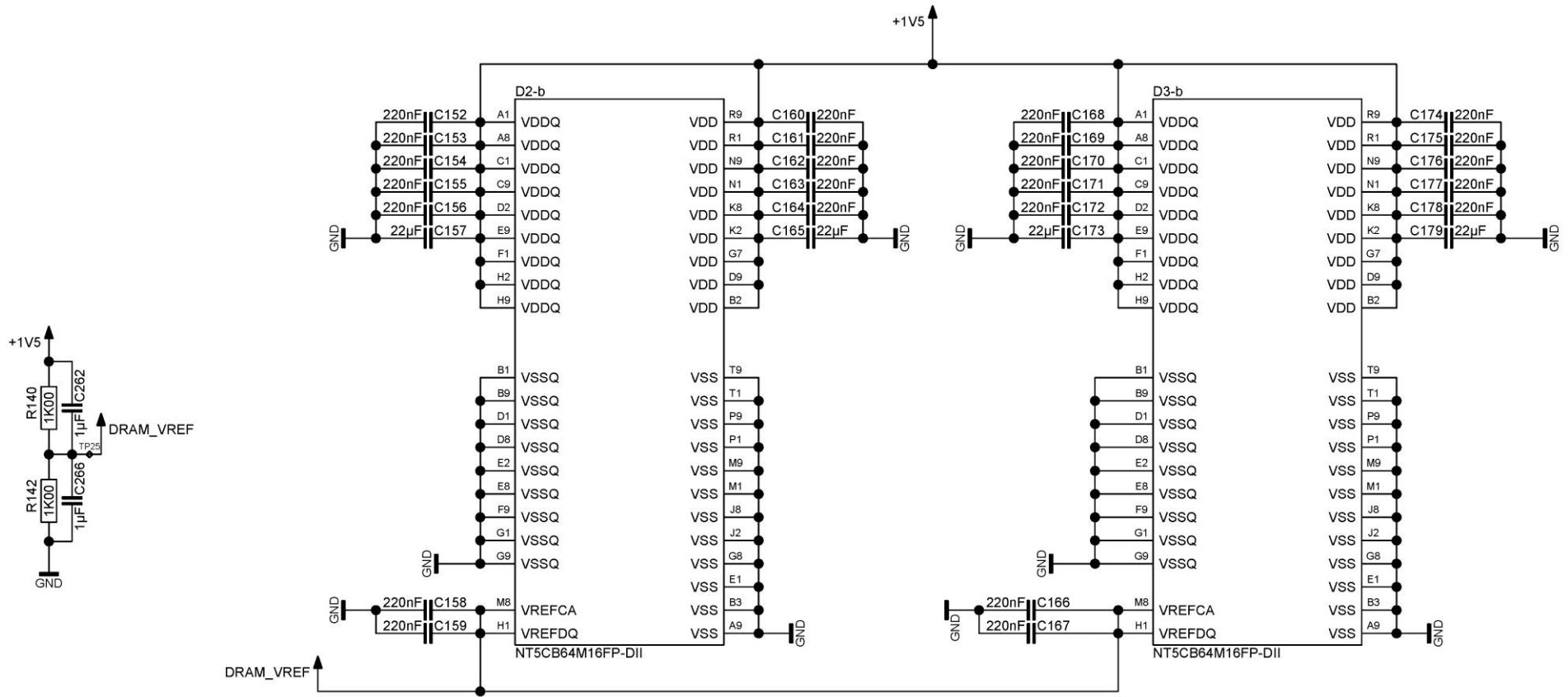
PREPARED		DATE		DRAWING NO.		REV.	
TG		28/03/2016		N/A		A1	
RESPONSIBLE		DATE		SHEET NAME		PAGE	
TG		03/03/2016		CPU_POWER		2	OF 5



D1-g



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REV	DATE	ENGINEER	NOTES
A1	29/03/2016	TG	First revision.

SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) (DIALOG DOCUMENT NUMBER: 24-400-02)

		TITLE: DA9061 i.MX 6Solo interface		
PREPARED: TG	DATED: 29/03/2016	DRAWING NO: N/A	REV: A1	
RESPONSIBLE: TG	DATED: 03/03/2016	SHEET NAME: REVISION/MECHANICAL		PAGE: 5 OF 5