IDT80KSW0002 (CPS-16)
IDT80KSW0004 (CPS-12)
IDT80KSW003 (CPS-8)

Evaluation Board
User Guide

Author: James An
Date: November 30, 2008
Revision: 3.0

Revision History

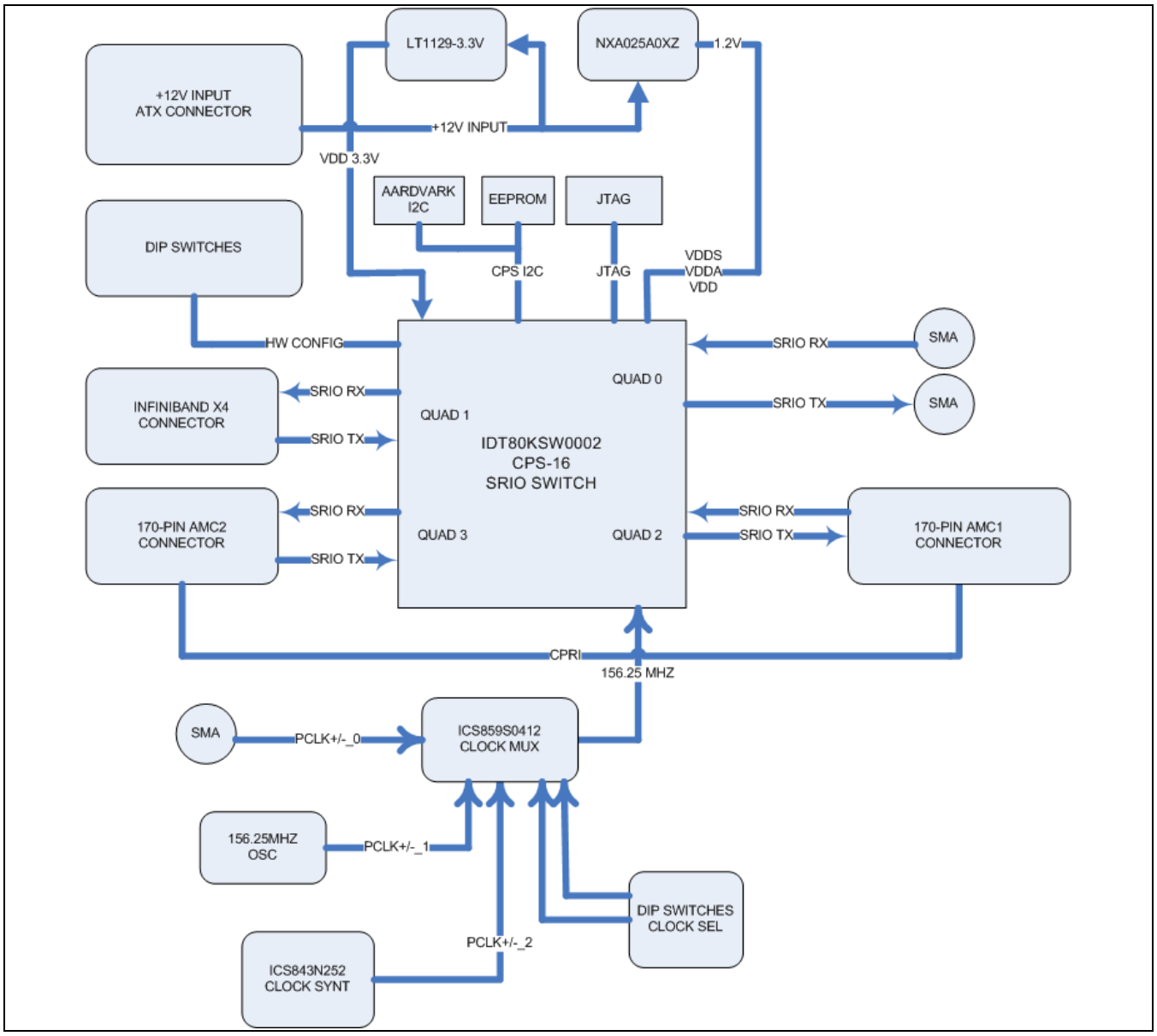
Revision	Date	Author	Comments
0.5	September 6, 2006	Ryan Morley	Initial Draft.
1.5	April 5, 2007	Ryan Morley	Updated for board revision 1.5
2.0	May 4, 2007	Ryan Morley	Updated for board revision 2.0 (19x19 mm package)
2.25	May 24, 2007	Ryan Morley	Updated to include I2C EEPROM addressing issues.
3.0	November 12, 2008	Quyen Nguyen	Updated to include rev 3.0 features.
3.0	November 30, 2008	James An	Updated to include AMC port mapping to support various platforms.

Table of Contents

Introduction

This document is intended to provide an overview of the IDT80KSW0002 (CPS-16), IDT80KSW0004 (CPS-12) and IDT80KSW0003 (CPS-8) Evaluation Board Rev 3.0. The information in this document applies to CPS Evaluation Board Rev 3.0, and is not necessarily compatible with PPS Evaluation Board Rev 1.0 or 1.5 or 2.0.

The CPS-16 Evaluation Board 3.0 is designed so that it can accommodate CPS Family of Switches; CPS-16, CPS-12 and CPS-8 as well as the IDT80KSW0001 (PPS Gen2) device.



CPS-16 Eval Board Block Diagram

CPS-16 Evaluation Board Sections	
1	ATX power supply input
2	Vdd3 Power Supply
3	1.2 V power supply (Vdd, Vdda, and Vdds)
4	I^2C input headers
5	SPEED Switches
6	Infiniband connector
7	I^2C Address Switches
8	JTAG Inputs
9	Reference Clock
10	AMC connectors
11	Reset Pushbutton
12	PPS/CPS
13	SRIO SMA connectors
14	Logic/Control Signal Headers
15	EEPROM
16	SRIO Logic analyzer connections

1. ATX Power Supply Input

The CPS Evaluation Board is designed for use with a standard 20-pin ATX power supply. The evaluation board is powered by the 12V source on the ATX supply. Other Voltages from the ATX supply are not used by the evaluation board; however, these voltages can be accessed through the 0.100" headers included on the board.

The ATX supply should be able to provide approximately 150 Watts at 12V. This will allow for power supply margin under full load (2 AMC modules) condition.

2. Vdd3 Power Supply

Component "Vdd3" is a 3.3V linear supply. Vdd3 is used to provide 3.3V power to the CPS, as well as to provide 3.3V management power to the AMC connectors. The output of Vdd3 is connected to the evaluation board by fuse F_Vdd3. Vdd3 can be powered-down by installing jumper Vdd3_Off.

3. 1.2V Power Supply (Vdd, Vdda, Vdds)

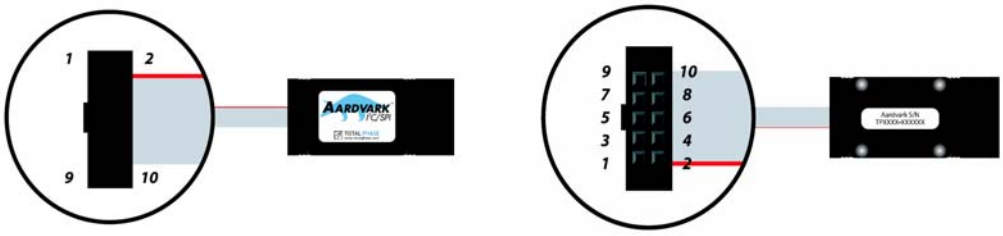
The Voltage regulator U1v2 is used to provide 1.2V to the CPS supplies. U1v2 powers Vdd, Vdds, and Vdda. However, each of these Voltage domains are individually fused (F_Vddx) and distributed to the CPS through separate planes.

The output Voltage level of U1v2 is controlled by Rtrim. The default value of Rtrim, 402 Ohms, should provide an output of 1.2V. This level can be adjusted by changing the value of Rtrim.

U1v2 can be powered down by installing jumper Vdd_off.

4. I²C Input Headers

The CPS I²C bus is connected to headers SDA_in and SCL_in. A 10-pin header AARD_IIC is provided for connection to the Totalphase Aardvark™ I²C/SPI adapter.



Aardvark I²C Adaptor

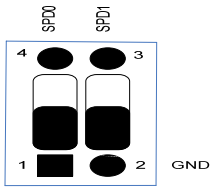
I2C Signal Interface on Aardvark AARD_IIC Connector

Signal	Description	AARD_IIC
SDA	Bi-directional data	3
SCL	I²C CLOCK: o Output when DUT configured as master	1

	o Input when DUT is configured as slave.	
NC	NC	4,6,5,7,8,9
GND	GROUND	2, 10

5. SPEED Switch SW_SPD

The CPS Speed pins, SPD [1:0], are connected to 2-POS DIP switch namely SW_SPD. It can be set to either 0 or 1. This controls the reset line rate of the CPS SRIO ports.



SW_SPD – DEV SPEED SETTING

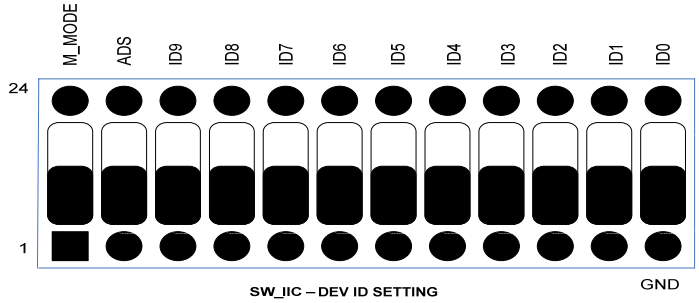
6. Infiniband Connector

One Infiniband 4x connector is provided on the evaluation board. This is to allow for the connection of multiple evaluation boards. Please refer to Appendix A: High Speed Lane Mapping for lane mapping of the Infiniband connector.

7. I²C Address Switches

SW_IIC is a 12-pos DIP switch for setting the CPS I²C address. Switch ADS selects 10-bit or 7-bit address mode. Switches ID9-ID0 set the I²C address.

For CPS applications, switch M_MODE enables I²C master mode.



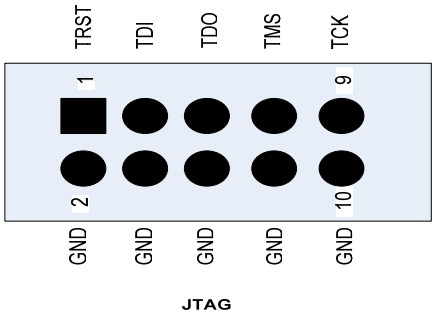
SW_IIC – DEV ID SETTING

SW1	SIGNALS	Description
24	M_MODE	Master Mode Select
23	ADS	7-bit or 10-bit I²C Addr Select
22	ID 9	Device ID Address bit 9
21	ID 8	Device ID Address bit 8
20	ID 7	Device ID Address bit 7

19	ID 6	Device ID Address bit 6
18	ID 5	Device ID Address bit 5
17	ID 4	Device ID Address bit 4
16	ID 3	Device ID Address bit 3
15	ID 2	Device ID Address bit 2
14	ID 1	Device ID Address bit 1
13	ID0	Device ID Address bit 0
1-12	GND	Ground or “0” Level

8. JTAG Inputs

Connector JTAG provides access to the CPS JTAG pins. Connector JTAG is a 10-pin, 100 mil IDC header, which can be used with the Corelis JTAG controller.



A 10-pin IDE header will be provided as follows:

JTAG	Description
1	TRST
2	GROUND
3	CPRI_TDI
4	GROUND
5	CPRI_TDO
6	GROUND
7	TMS
8	GROUND
9	TCK
10	GROUND

9. Reference Clock

The CPS is designed to operate with an AC coupled reference clock, at a frequency of 156.250 MHz. This can be implemented on the Evaluation Board using an external clock sources, onboard crystal oscillator or the PLL synthesizer.

To use one of these clock sources, please see the tables below to set SW2; output enable and output clock level interface:

SW2	SIGNALS	Description
1	CLK_SEL[0]	SELECT INPUT CLOCK BIT 0
2	SEL_OUT	CLOCK OUTPUT LEVEL
3	CLK_SEL[1]	SELECT INPUT CLOCK BIT 1
4	OE_Q	OUPUT ENABLE

SEL_OUT	Q[0:1]/nQ[0:1]
1	LVPECL
2	LVDS

CLK_SEL1	CLK_SEL0	INPUT CLOCK
0	0	FROM SMA CONNECTORS
0	1	FROM ON-BOARD OSCILLATOR
1	0	FROM CLOCK SYNTHESIZER
1	1	RESERVED

OE_Q	Q[0:1]/nQ[0:1]
1	NORMAL OPERATION (DEFAULT)
0	LOW/HIGH

The evaluation board is designed for use with PECL clock oscillators. For use of LVDS oscillators, remove Rdn_clk+/- and Rup_clk+/-, and replace 50 Ohm Rs_clk+/- with 0-Ohm resistors.

10. AMC Connectors

Two AMC B+ connectors are provided on the evaluation board for use with AMC modules. These connectors do not implement full AMC functionality.

PS1# and PS0# pins are tied to proper levels. However, they are not used to control ENABLE#.

ENABLE# is held low by jumper AMCx_en. To disable the AMC module, remove jumper AMCx_en.

GA0-2 pins are floating (NC).

AMC JTAG and I2C pins are floating; header access is provided to these pins, if needed.

CLK1-3 are not implemented.

Four ports of pass-through connectivity are provided as a direct high-speed connection between AMC1 and AMC2.

Please refer to Appendix A: High Speed Lane Mapping for lane mapping of the AMC connectors.

11. Reset Pushbutton

Pushbutton CPS_RST is used to hard-reset the CPS. Jumper J_Rst must be installed. Direct access to the CPS RST pin is available at the 'Local' pin of header J_Rst.

12. Socket

The CPS Evaluation Board is designed for either solder-down or socketed use of the CPS. For socketed applications, use Ironwood Electronics C7439 GHz BGA socket.

13. SRIO SMA Connectors

Lanes 0–3 of the CPS can be accessed through SMA connectors. AC-coupling capacitors are placed on the receiver paths.

If connecting the SMA outputs to test equipment (50 Ohm – GND termination), SMA – SMA DC – Blocks should be used.

14. Logic/Control Signal Headers

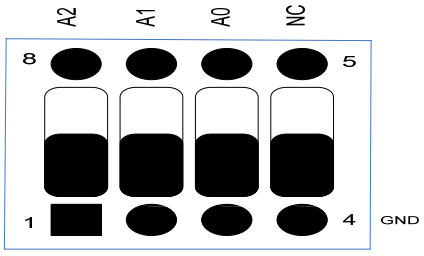
Access to the CPS logic and test pins is available at headers located near the CPS.

15. EEPROM

An I^2C EEPROM is included on the Evaluation Board for use in CPS Master Mode applications. The EEPROM I^2C address is 1010(ID2) (ID1) (ID0), where ID2:0 are the three LSBs of the CPS I^2C address.

To avoid I^2C bus contention, CPS signals ID6:3 should not be set to 1010.

Switch SW1 is used to set the EEPROM address as follows:



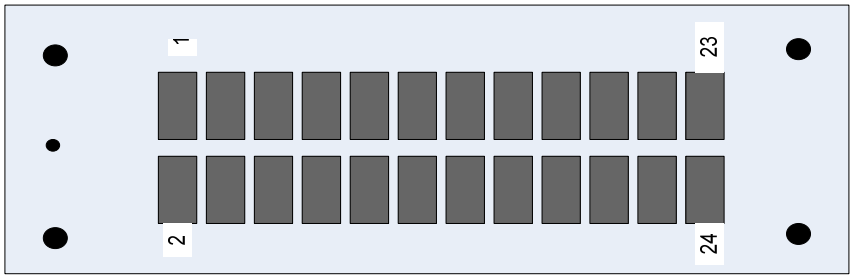
SW1 – EEPROM I2C ADDRESS SETTING

SW1	SIGNALS	Description
5	NC	No connect
6	ID 0	EEPROM ADDRESS BIT 0
7	ID 1	EEPROM ADDRESS BIT 1
8	ID 2	EEPROM ADDRESS BIT 2

16. SRIO LA Connections

Compression style logic analyzer connections are provided for functional probing of SRIO traffic. Please refer to Appendix A: High Speed Lane Mapping for signal availability on the SRIO LA connections.

LA_AMC1/2- FUTUREPLUS



Appendix A: High Speed Lane Mapping

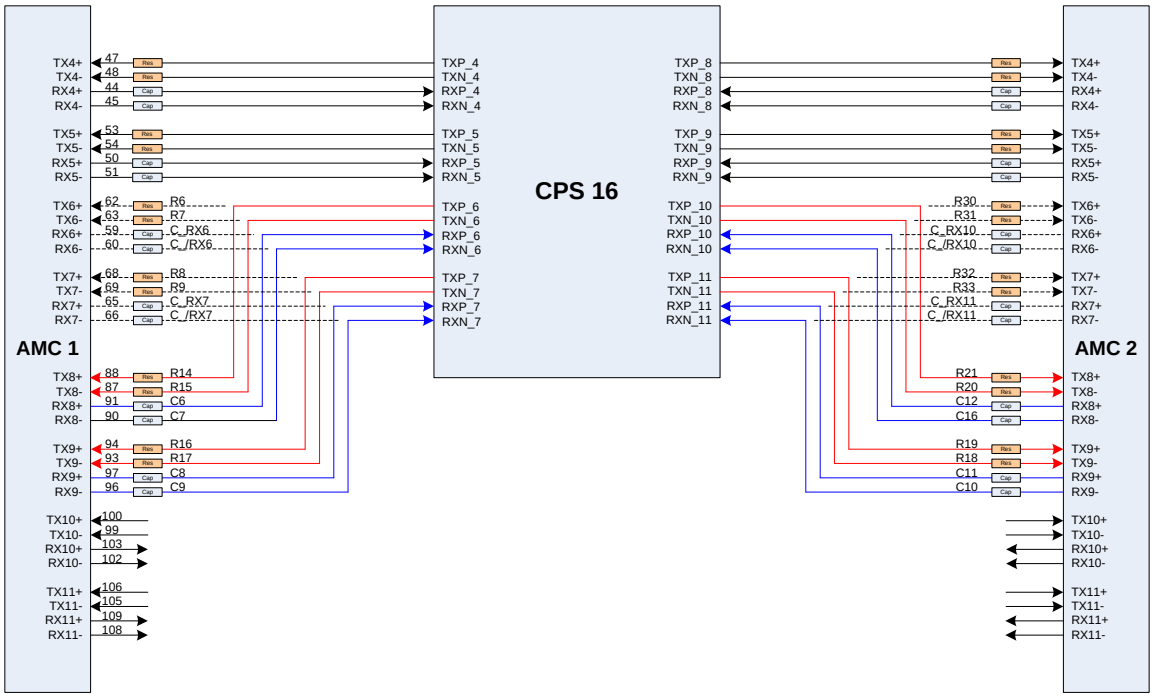
The following table outlines the high speed lane mapping of the CPS Evaluation Board Rev 3.0 applications.

CPS Lane number		Connections
0		SMA
1		SMA
2		SMA
3	Quad 0	SMA
4		AMC1 Port 4
5		AMC1 Port 5
6		AMC1 Port 6
7	Quad 1	AMC1 Port 7
8		AMC2 Port 4
9		AMC2 Port 5
10		AMC2 Port 6
11	Quad 2	AMC2 Port 7
12		Infiniband, Lane 0
13		Infiniband, Lane 1
14		Infiniband, Lane 2
15	Quad 3	Infiniband, Lane 3
	Pass Through 0	AMC1 Port 12 to AMC2 Port 12
	Pass Through 1	AMC1 Port 13 to AMC2 Port 13
	Pass Through 2	AMC1 Port 14 to AMC2 Port 14
	Pass Through 3	AMC1 Port 15 to AMC2 Port 15

TI Faraday EVM Mapping

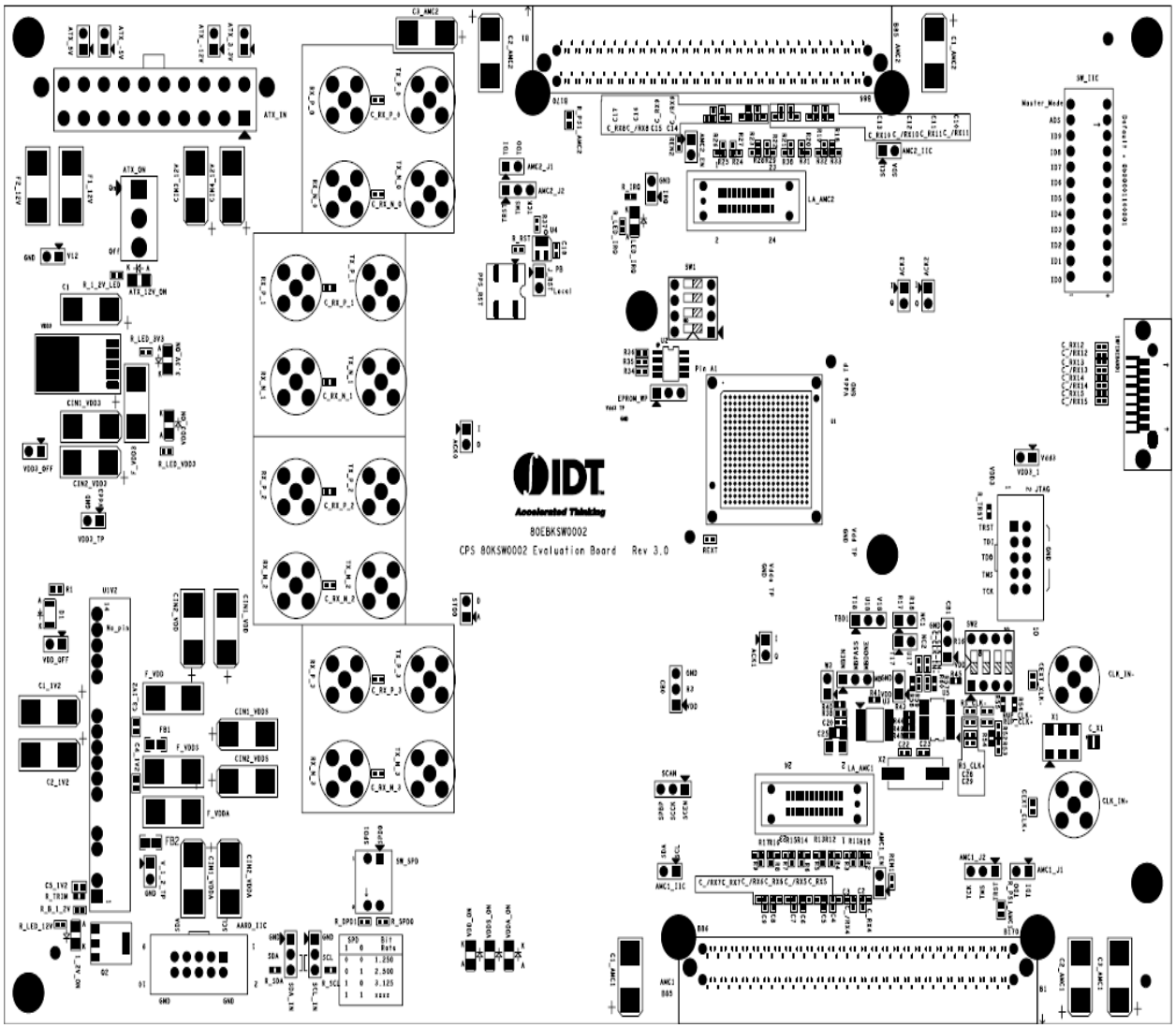
The CPS Evaluation Board provides stuffing option to accommodate TI TMS329TCI6488/87 (Faraday) Mezzanine EVM Board. By properly selecting the capacitors and resistors, the CPS16 can map its sRIO lanes to support both of the DSP core's 2 x1 lanes on AMC1 and AMC2.

Refer to below diagram for Faraday configuration. To configure for Faraday support, remove components outlined with dotted lines and place them to map to second pipe of the AMC connector (TX+/-8, TX+/-9, RX+/-8, RX+/-9) as directed in the below diagram.



CPS16 EVAL BOARD Rev 3.0 TI Faraday EVM Port Mapping

Appendix B: Assembly Drawing



All design files including the layout, BOM and Gerber files are available upon request. Contact IDT Communications Division's technical group at fcm-wireless-apps@idt.com.

Appendix C: Schematic Drawing

REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
PCB-00170R03	3.0	CPS 80KSW0002 EVAL BOARD	2008-09-19	QUYEN N.

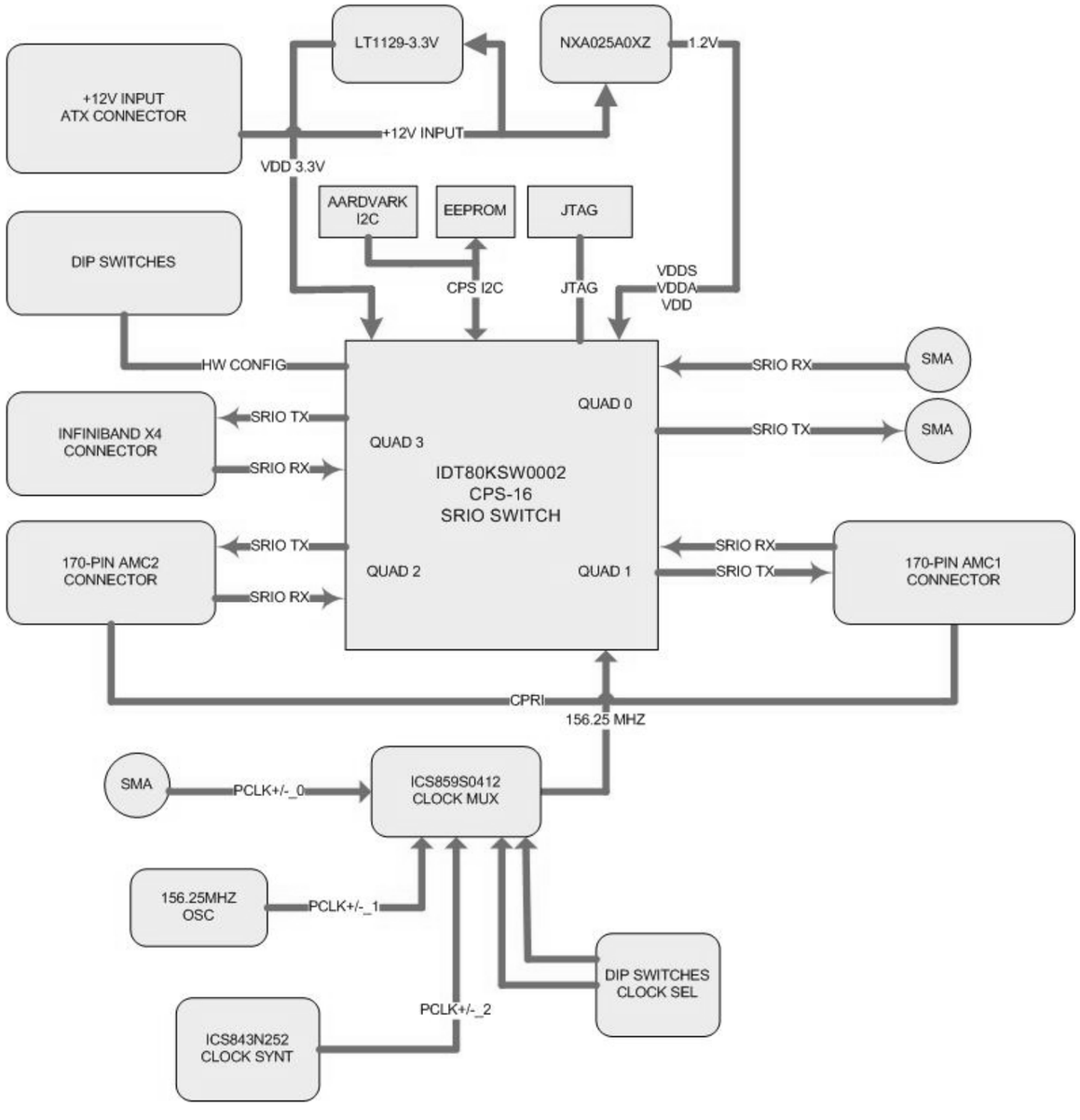


TABLE OF CONTENTS

TITLE: IDT80KSW0002-BGA324

SIZE	DRAWING NO.	FAB P/N	REV.
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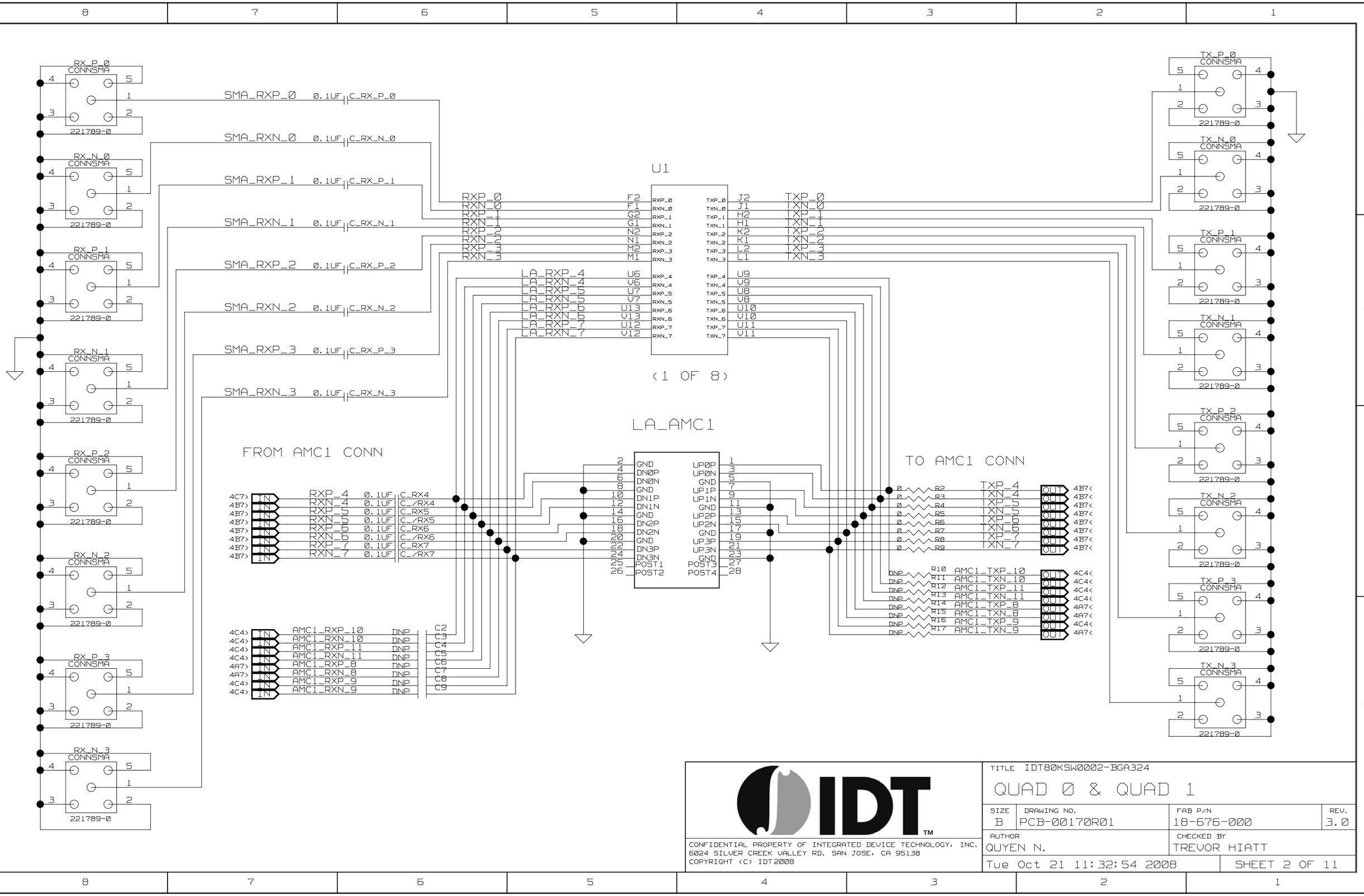
AUTHOR	CHECKED BY
QUYEN N.	TREVOR HIATT

Wed Oct 29 15:48:37 2008 | SHEET 1 OF 11



TITLE IDT80KSW0002-BGA324

QUAD 0 & QUAD 1

SIZE	DRAWING NO.	FAB P/N	REV.
B	PCB-00170R01	18-676-000	3.0

AUTHOR	CHECKED BY
QUYEN N.	TREVOR HIATT

Tue Oct 21 11:32:54 2008 — SHEET 2 OF 11

FROM AMC2 CONN

5C7> IN RXP_8 0.1UF C_RX8
5C7> IN RXN_8 0.1UF C_/RX8
5C7> IN RXP_9 0.1UF C_RX9
5B7> IN RXN_9 0.1UF C_/RX9
5B7> IN RXP_10 0.1UF C_RX10
5B7> IN RXN_10 0.1UF C_/RX10
5B7> IN RXP_11 0.1UF C_RX11
5B7> IN RXN_11 0.1UF C_/RX11

FROM INFINIBAND CONN

11B6> IN RXP_12 0.1UF C_RX12
11B6> IN RXN_12 0.1UF C_/RX12
11B6> IN RXP_13 0.1UF C_RX13
11B6> IN RXN_13 0.1UF C_/RX13
11B6> IN RXP_14 0.1UF C_RX14
11B6> IN RXN_14 0.1UF C_/RX14
11B6> IN RXP_15 0.1UF C_RX15
11B6> IN RXN_15 0.1UF C_/RX15

5D4> IN AMC2_RXN_9 DNP C10
5D4> IN AMC2_RXP_9 DNP C11
5B7> IN AMC2_RXN_8 DNP C12
5B7> IN AMC2_RXP_8 DNP C13
5C4> IN AMC2_RXN_11 DNP C14
5C4> IN AMC2_RXP_11 DNP C15
5C4> IN AMC2_RXN_10 DNP C16
5C4> IN AMC2_RXP_10 DNP C17

FROM AMC2 CONN

U1

B13	RXP_8	TXP_8	B10		
A13	RXN_8	TXN_8	A10		
B12	RXP_9	TXP_9	B11		
A12	RXN_9	TXN_9	A11		
B6	RXP_10	TXP_10	B9		
A6	RXN_10	TXN_10	A9		
B7	RXP_11	TXP_11	B8		
A7	RXN_11	TXN_11	A8		
N17	RXP_12	TXP_12	K17	TXP_12	
N18	RXN_12	TXN_12	K18	TXN_12	
M17	RXP_13	TXP_13	L17	TXP_13	
M18	RXN_13	TXN_13	L18	TXN_13	
F17	RXP_14	TXP_14	J17	TXP_14	
F18	RXN_14	TXN_14	J18	TXN_14	
G17	RXP_15	TXP_15	H17	TXP_15	
G18	RXN_15	TXN_15	H18	TXN_15	

(2 OF 8)

TO INFINIBAND CONN

OUT 11B6<
OUT 11B6<
OUT 11B6<
OUT 11B6<
OUT 11B6<
OUT 11B6<
OUT 11B6<
OUT 11B6<

LA_AMC2

2	GND	UP0P	1
4	DN0P	UP0N	3
6	DN0N	GND	5
8	GND	UP1P	7
10	DN1P	UP1N	9
12	DN1N	GND	11
14	GND	UP2P	13
16	DN2P	UP2N	15
18	DN2N	GND	17
20	GND	UP3P	19
22	DN3P	UP3N	21
24	DN3N	GND	23
25	POST1	POST3	27
26	POST2	POST4	28

TO AMC2 CONN

0 R26 TXP_8 OUT 5C7<
0 R27 TXN_8 OUT 5C7<
0 R28 TXP_9 OUT 5B7<
0 R29 TXN_9 OUT 5B7<
0 R30 TXP_10 OUT 5B7<
0 R31 TXN_10 OUT 5B7<
0 R32 TXP_11 OUT 5B7<
0 R33 TXN_11 OUT 5B7<
DNP R18 AMC2_TXN_9 OUT 5A7<
DNP R19 AMC2_TXP_9 OUT 5D4<
DNP R20 AMC2_TXN_8 OUT 5B7<
DNP R21 AMC2_TXP_8 OUT 5B7<
DNP R22 AMC2_TXN_11 OUT 5C4<
DNP R23 AMC2_TXP_11 OUT 5C4<
DNP R24 AMC2_TXN_10 OUT 5D4<
DNP R25 AMC2_TXP_10 OUT 5C4<

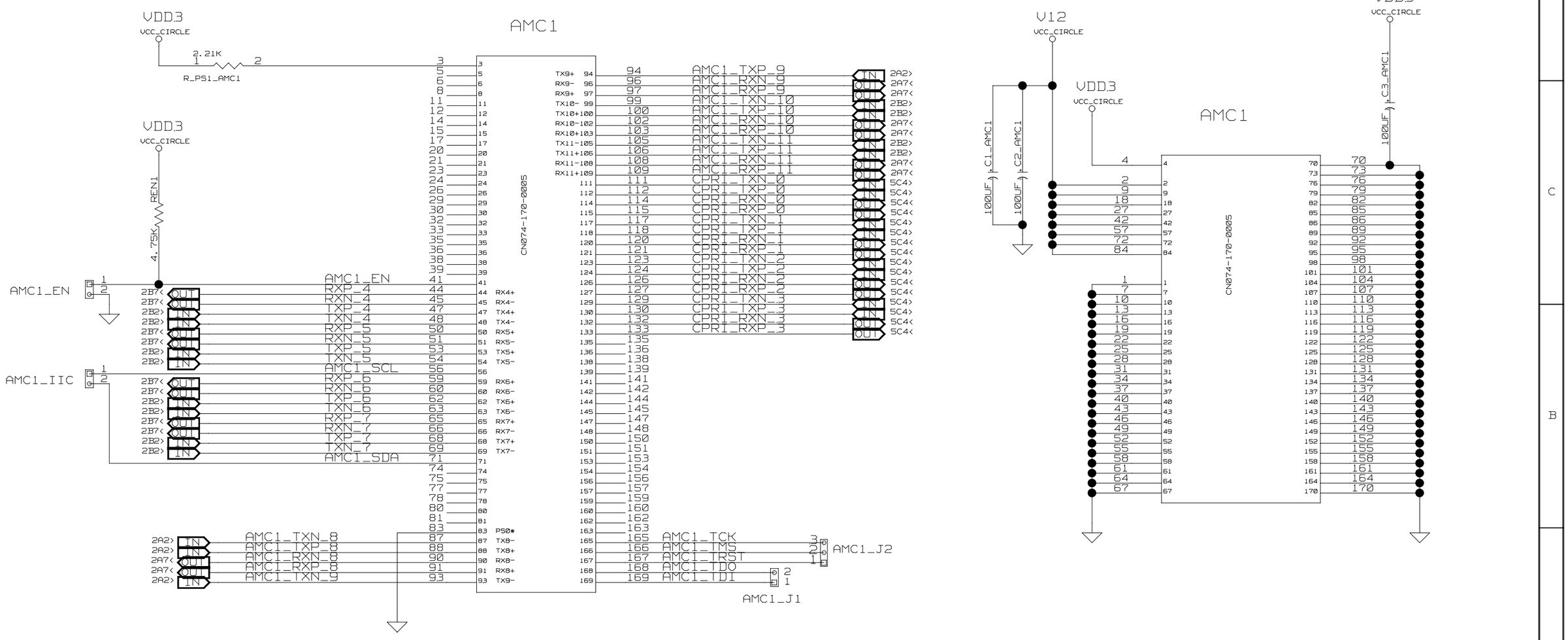
TITLE IDT80KSW0002-BGA324

QUAD 2 & QUAD 3

SIZE	DRAWING NO.	FAB P/N	REV.
B	PCB-00170R01	18-676-000	3.0

AUTHOR	CHECKED BY
QUYEN N.	TREVOR HIATT

Tue Oct 21 11:36:14 2008 SHEET 3 OF 11



TITLE IDT80KSW0002-BGA324

AMC CONNECTION # 1

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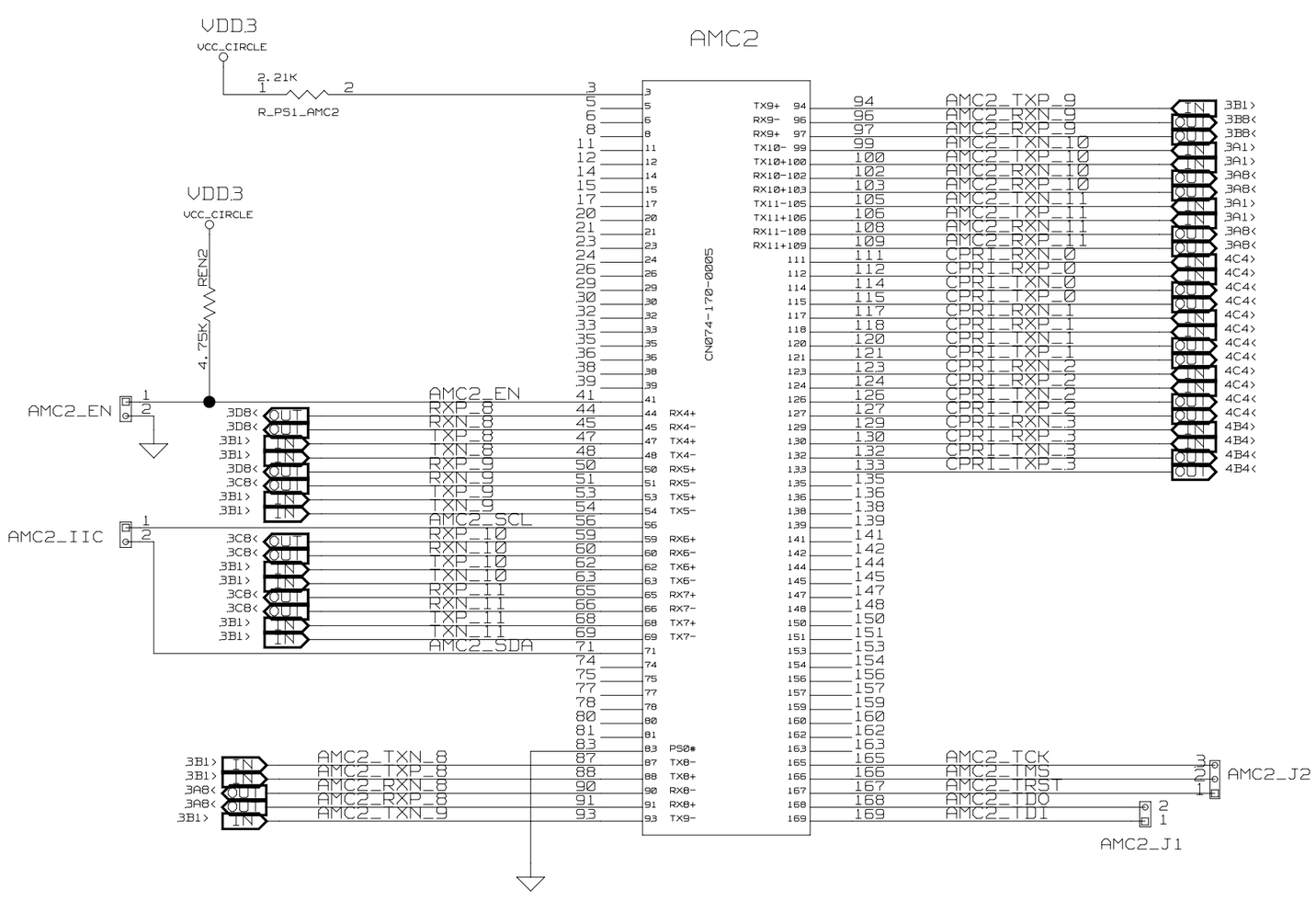
AUTHOR	CHECKED BY
QUYEN N.	TREVOR HIATT

Thu Oct 16 15:49:48 2008 — SHEET 4 OF 11



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TITLE IDT80KSW0002-BGA324

AMC CONNECTOR # 2

SIZE	DRAWING NO.	FAB P/N	REV.
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AUTHOR	CHECKED BY
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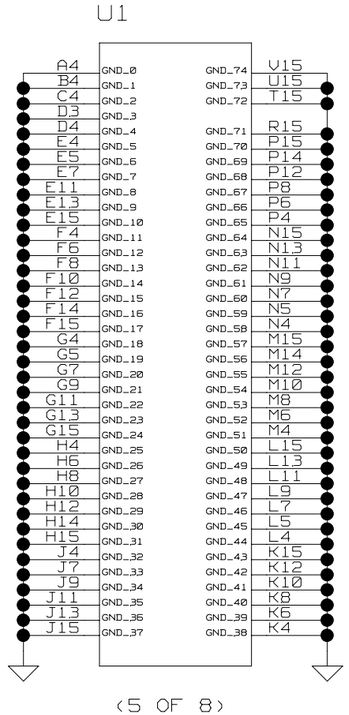

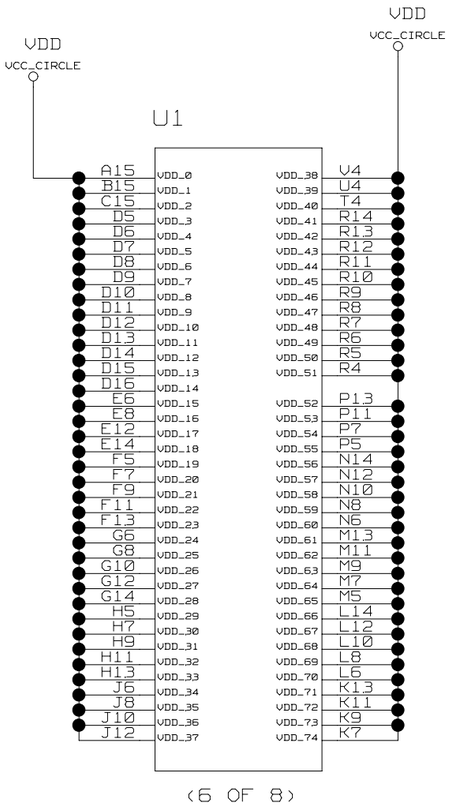

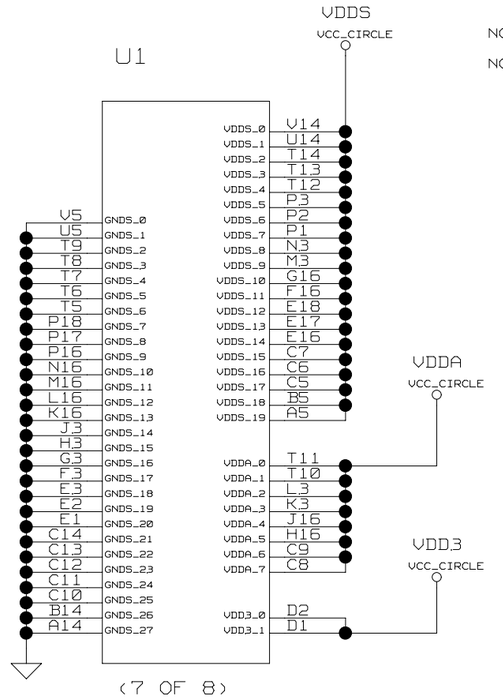

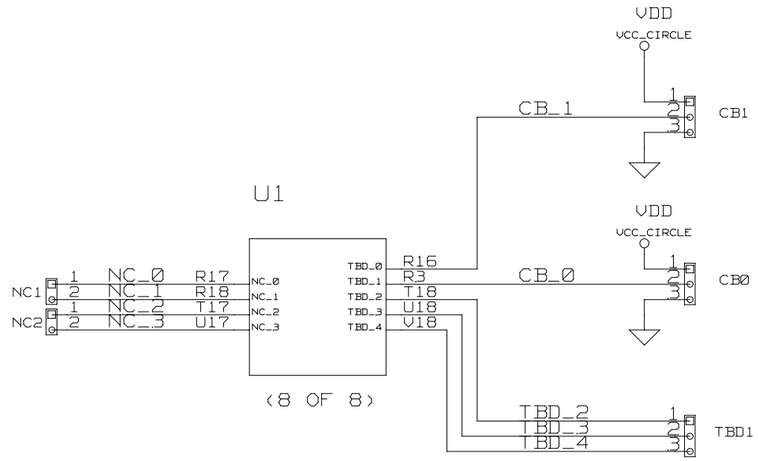

CPS CONFIGURATION

CB[1:0]	CONFIG
0 0	CPS-8
0 1	CPS-12
1 0	INTERNAL FUSE SETTING
1 1	CPS-16

TITLE IDT80KSW0002-BGA324

DEVICE POWERS/GND & NC

SIZE	DRAWING NO.	FAB P/N	REV.
B	PCB-00170R01	18-676-000	3.0

AUTHOR	CHECKED BY
QUYEN N.	TREVOR HIATT

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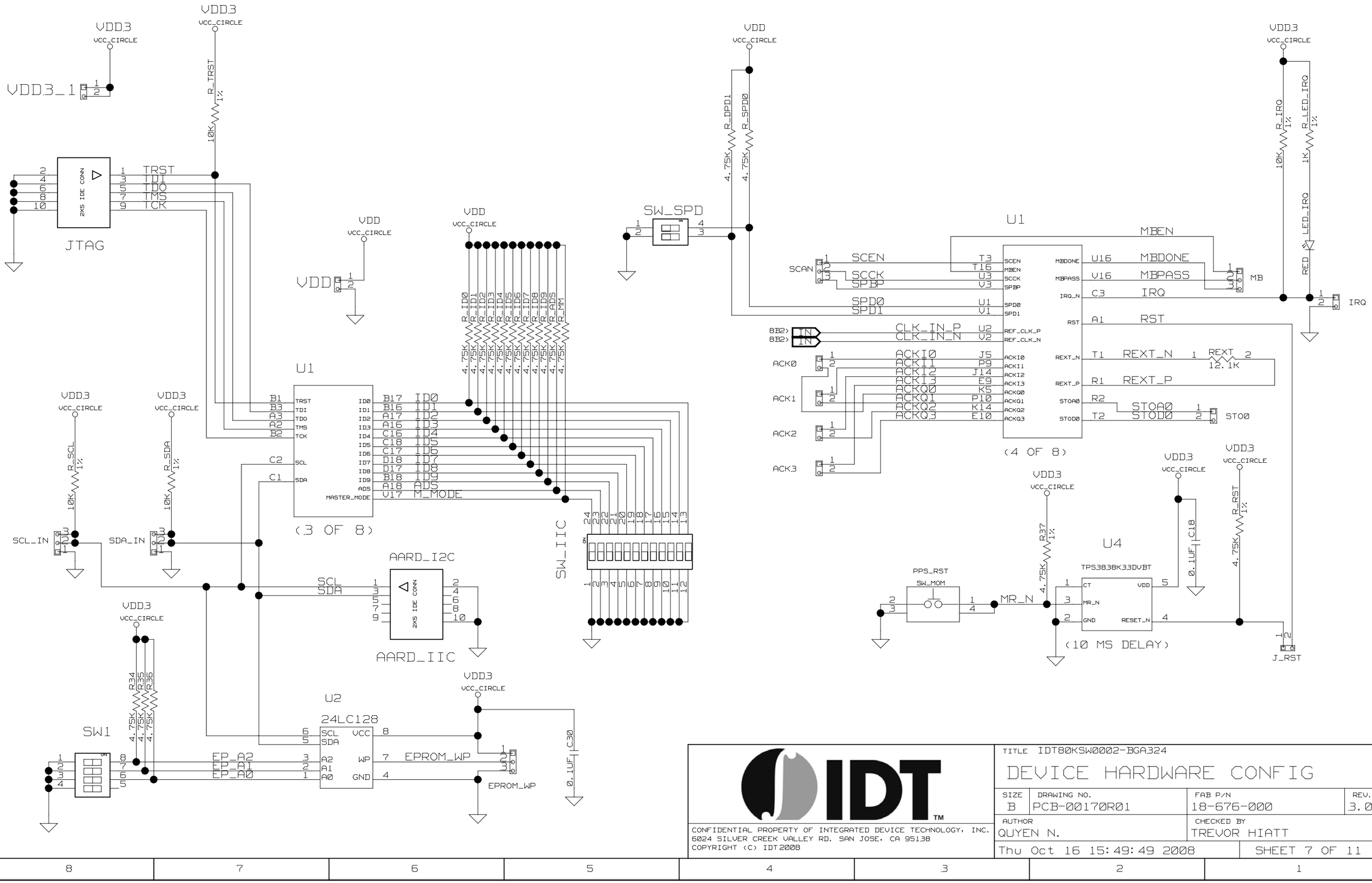

TITLE IDT80KSW0002-BGA324

DEVICE HARDWARE CONFIG

SIZE	DRAWING NO.	FAB P/N	REV.
B	PCB-00170R01	18-676-000	3.0

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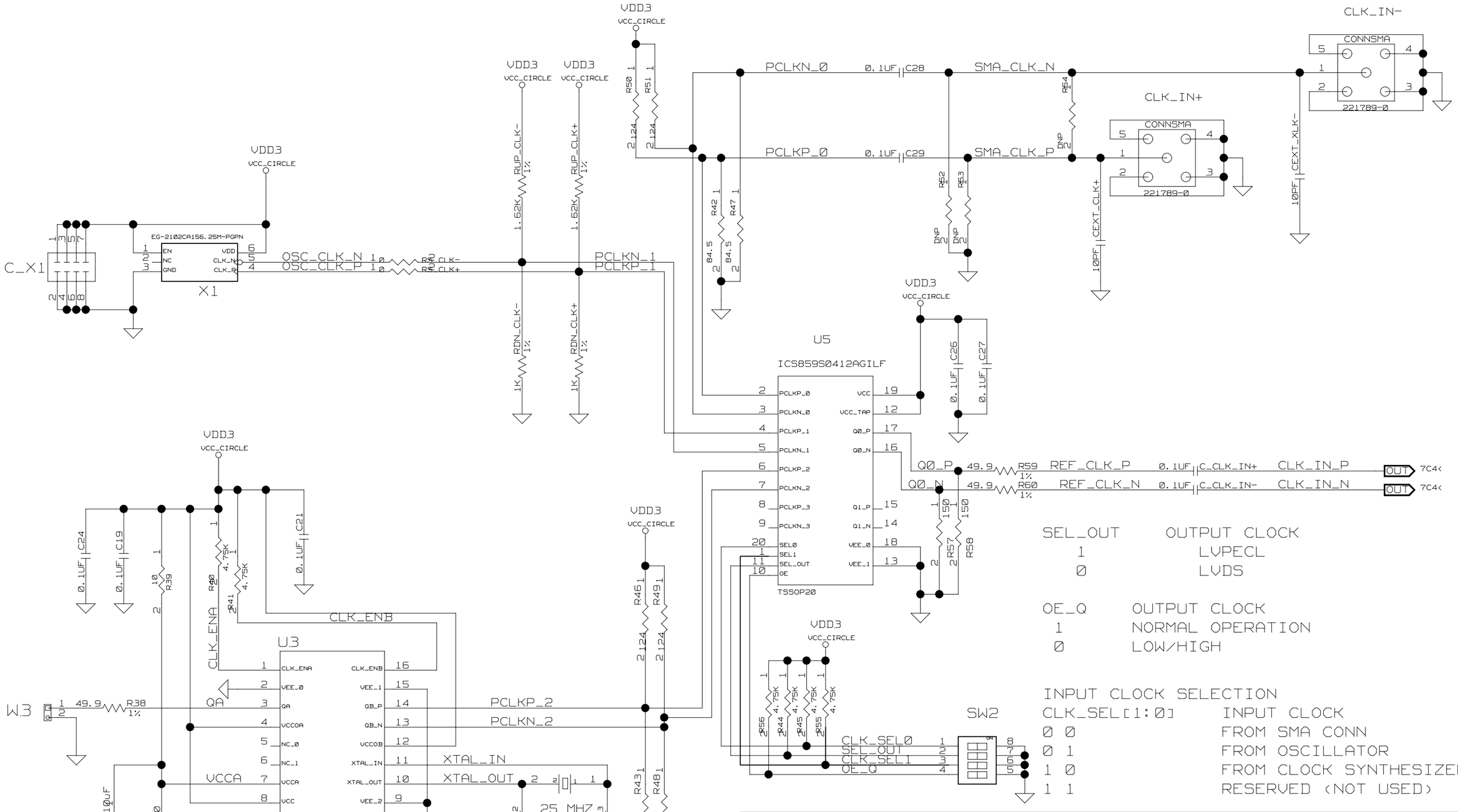
Thu Oct 16 15:49:49 2008 — SHEET 7 OF 11



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TITLE IDT80KSW0002-BGA324

REFERENCE CLOCK SOURCE

SIZE	DRAWING NO.	FAB P/N	REV.
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AUTHOR	CHECKED BY
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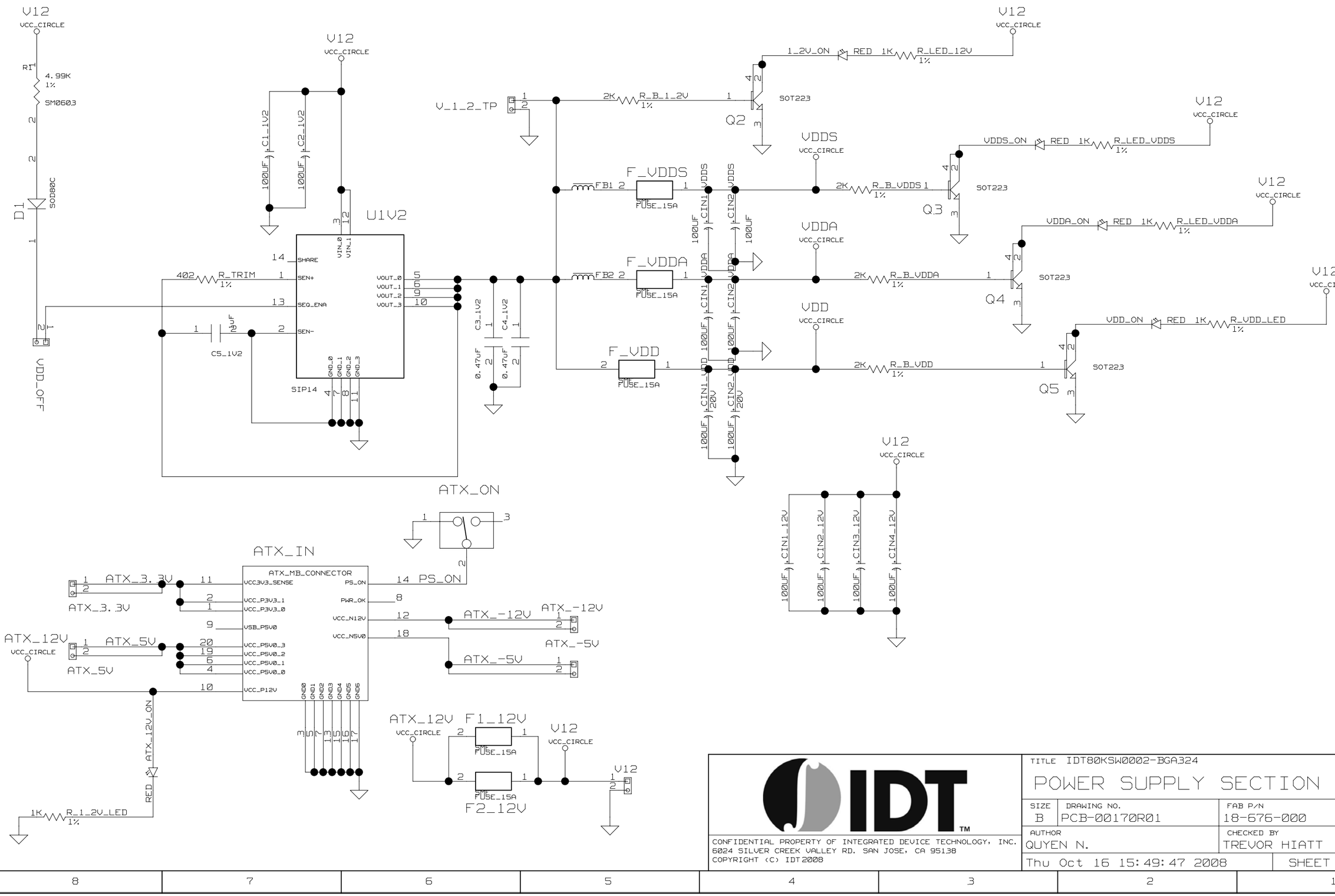
Thu Nov 13 16:00:27 2008 SHEET 8 OF 11



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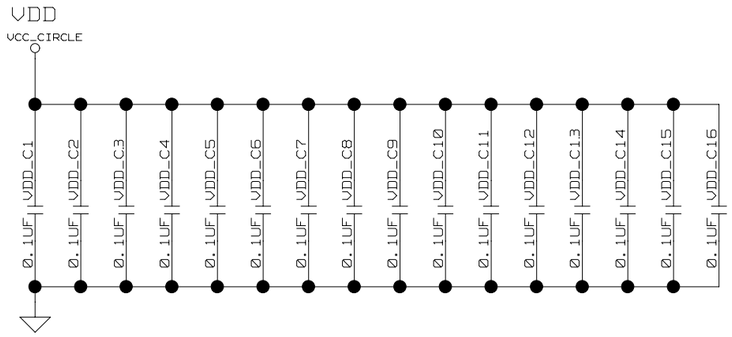
TITLE IDT80KSW0002-BGA324

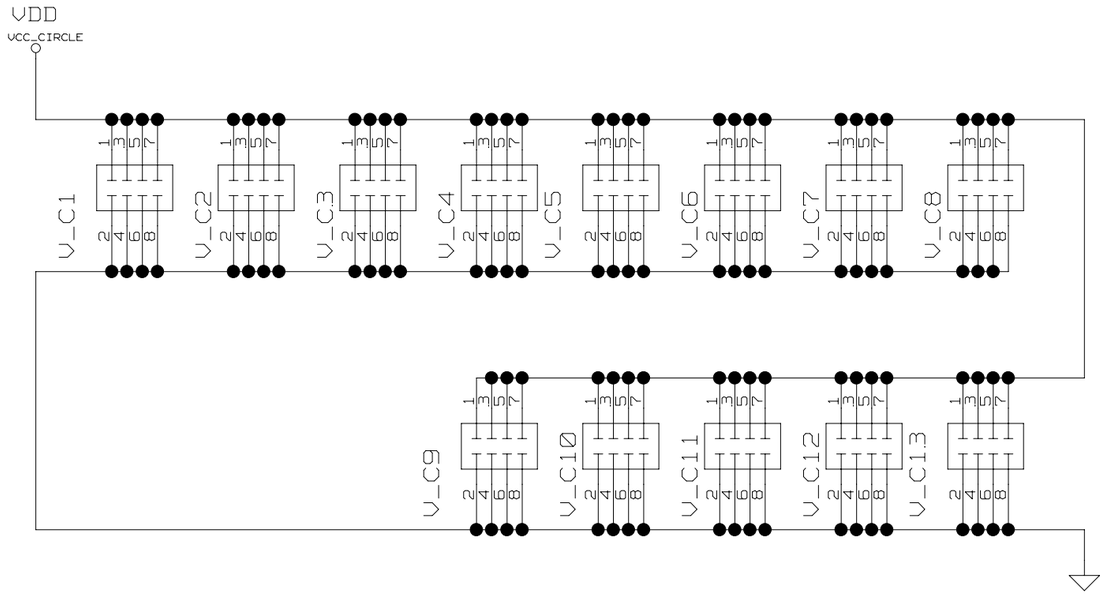
POWER SUPPLY SECTION

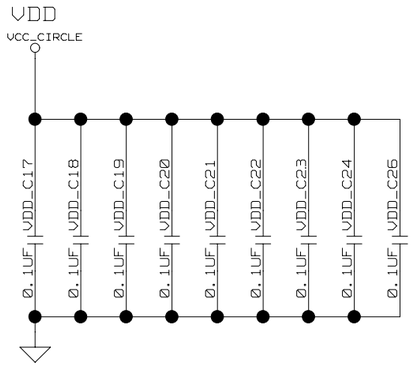
SIZE	DRAWING NO.	FAB P/N	REV.
B	PCB-00170R01	18-676-000	3.0

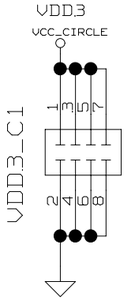
AUTHOR	CHECKED BY
QUYEN N.	TREVOR HIATT

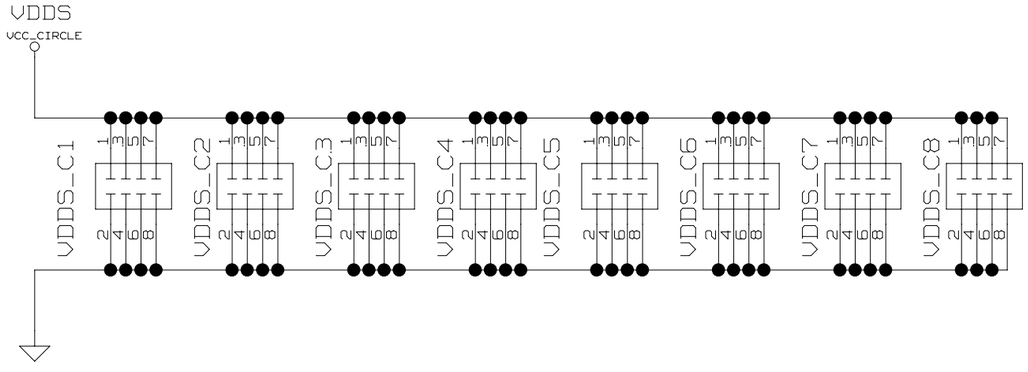
Thu Oct 16 15:49:47 2008 — SHEET 9 OF 11

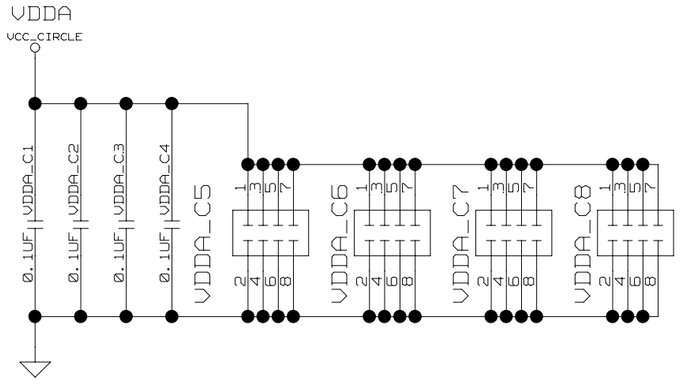












TITLE IDT80KSW0002-BGA324

DECOUPLING CAPS

SIZE	DRAWING NO.	FAB P/N	REV.
B	PCB-00170R01	18-676-000	3.0

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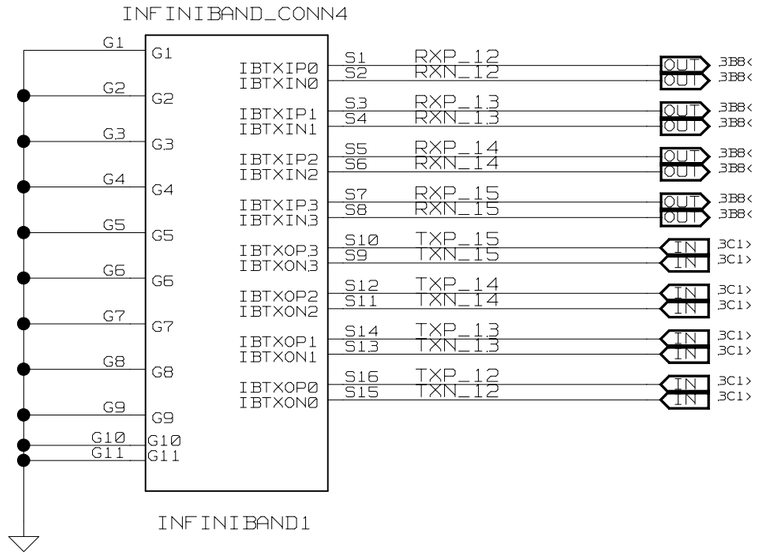
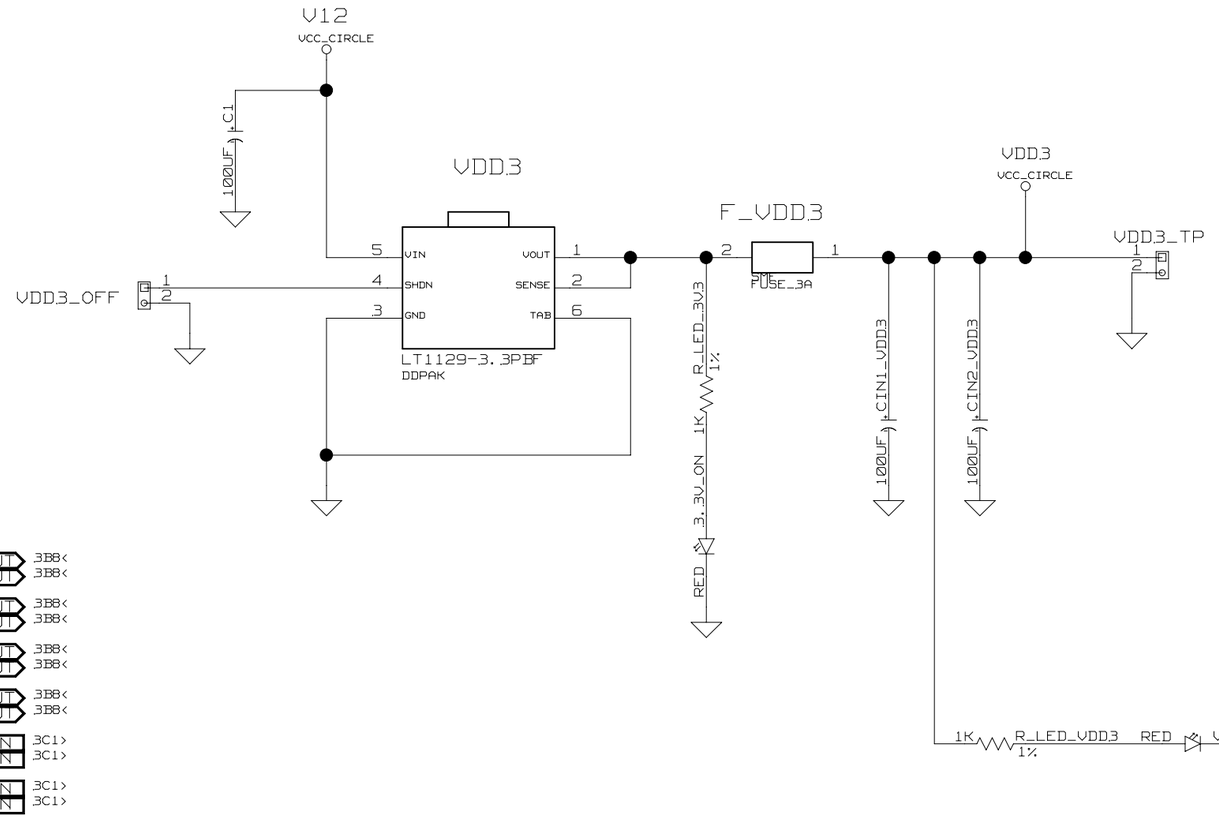
Thu Oct 16 15:49:50 2008 — SHEET 10 OF 11





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INFINIBAND CONNECTION

SIZE	DRAWING NO.	FAB P/N	REV.
B	PCB-00170R01	18-676-000	3.0

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