



<- Leave Feed Back out floating.

CONFIGURATION SHOWN = HIGH\_BANDWIDTH, 133 MHz, SMBus ADDRESS=0xC2

VDD\_IO May be 1.05 to 3.3 volts

<- Place at pin.

Place at pin.

<- VDD FOR PLL

<- VDD FOR INPUT RECEIVER

### 85 Ohm Differential

HiBW BypM\_LoBW# MODE  
 Low PLL Lo BW  
 Mid Bypass  
 High PLL Hi BW

NOTE: PLL is OFF in Bypass Mode

Tri-Level Inputs		
SMB_A1	SMB_A0	Add
0	0	D8
0	M	DA
0	1	DE
M	0	C2
M	M	C4
M	1	C6
1	0	CA
1	M	CC
1	1	CE

NOTE: FERRITE BEADS =

Manufacture	Part Number	Z@100MHz	PkgSz	DC_res.	Current (Ma)
muRata	BLM21A601R	600	0805	0.30	600
TDK	MMZ2012S601A	600	0805	0.30	600
STEWART	HZ0805E601R	600	0805	0.30	600
AssocCmpTch	CBG0805-600-50	600	0805	0.30	600

Revision history

Rev	Change
0.1	First publication
0.3	Change R1 & R2 = 1.0 ohm.

**Integrated Device Technology**  
 6024 Silver Creek Valley Road  
 San Jose, CA

Title		9ZXL1950
Size B	Document Number	Rev 0.3
Date:	Friday, March 22, 2019	Sheet 1 of 1