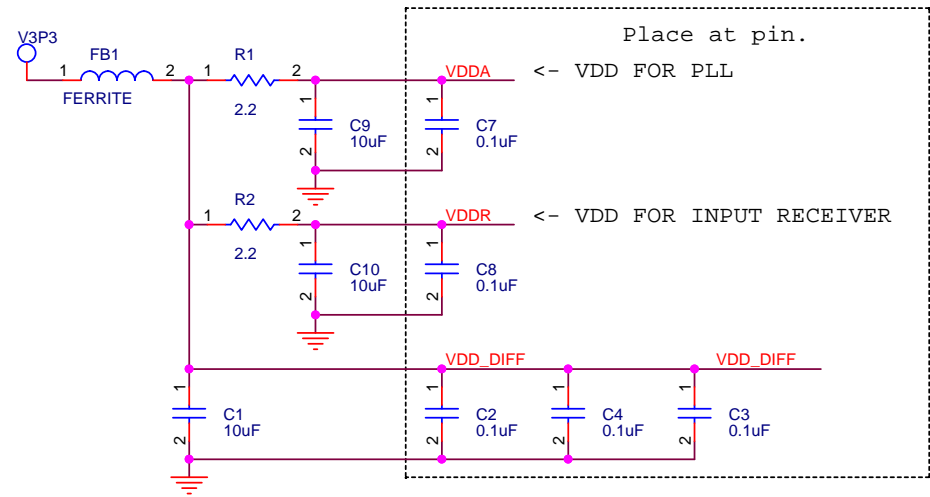
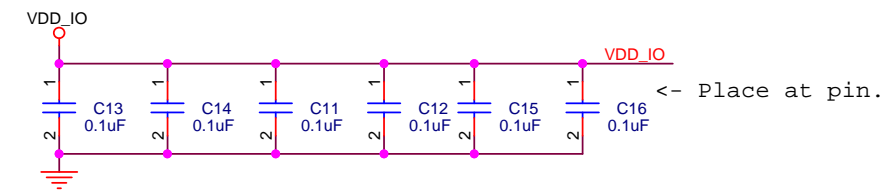


<- Leave Feed Back out floating.

### 85 Ohm Differential

If there are unused outputs leave them floating.  
Provide test points on an unused output for measuring phase noise

VDD\_IO May be 1.05 to 3.3 volts



HiBw BypM LoBW#	MODE
Low	PLL Lo BW
Mid	Bypass
High	PLL Hi BW

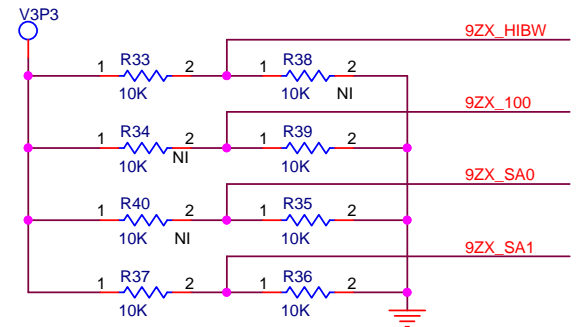
NOTE: PLL is OFF in Bypass Mode

NOTE: FERRITE BEADS =

Manufacture	Part Number	Z@100MHz	PkgSz	DC res	Current (Ma)
muRata	BLM21A601R	600	0805	0.30	600
TDK	MMZ2012S601A	600	0805	0.30	600
STEWART	HZ0805E601R	600	0805	0.30	600
AssocCmpTch	CBG0805-600-50	600	0805	0.30	600

SMB A1	SMB A0	Add
Tri-Level		

0	0	D8
0	M	DA
M	1	DE
M	0	C2
M	M	C4
M	1	C6
1	0	CA
1	M	CC
1	0	CC



CONFIGURATION SHOWN = HIGH\_BANDWIDTH, 133 MHz, SMBus ADDRESS=0xc2

**Integrated Device Technology**  
6024 Silver Creek Valley Road  
San Jose, CA

Title: 9ZXL1550	
Size: B	Document Number
Date: Thursday, August 24, 2017	Rev: 0.2

Rev	Change
0.1	First publication
0.2	Changed 1 uF caps to 10 uF