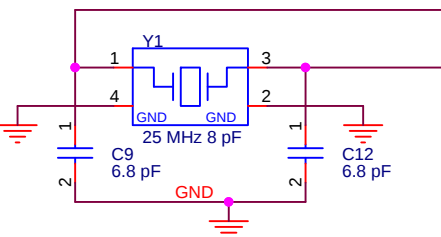
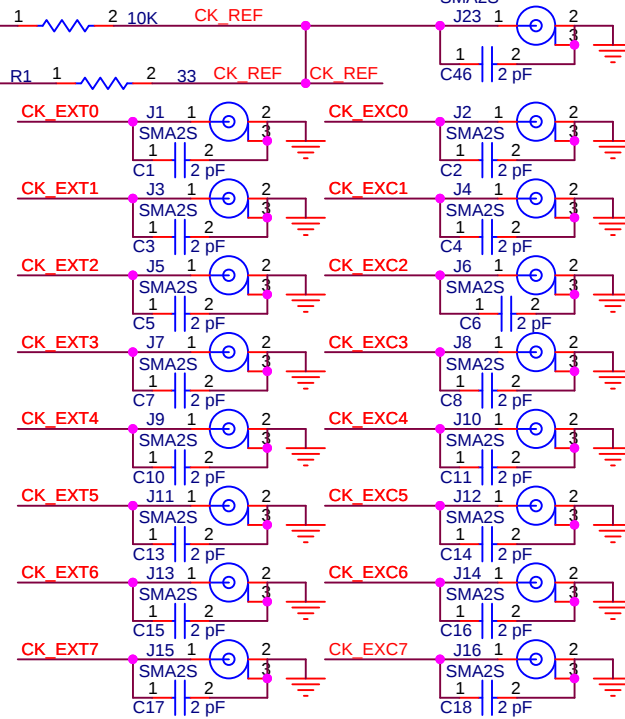
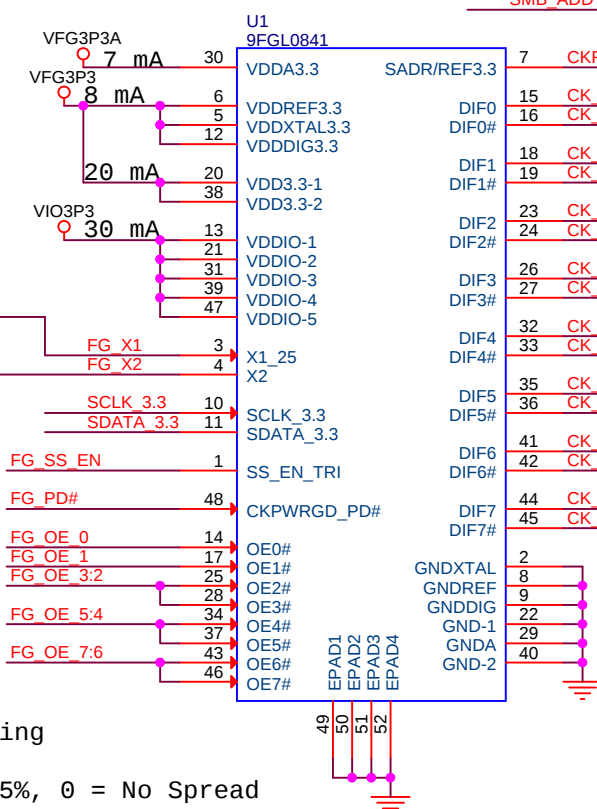


Layout notes

1. Separate Xout and Xin traces by at least 3 x the trace width.
2. Do not share crystal load capacitor ground via with other components.
3. Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
4. Do not share ground vias. One ground pin one ground via.
5. Exposed pad should be grounded but is not required.

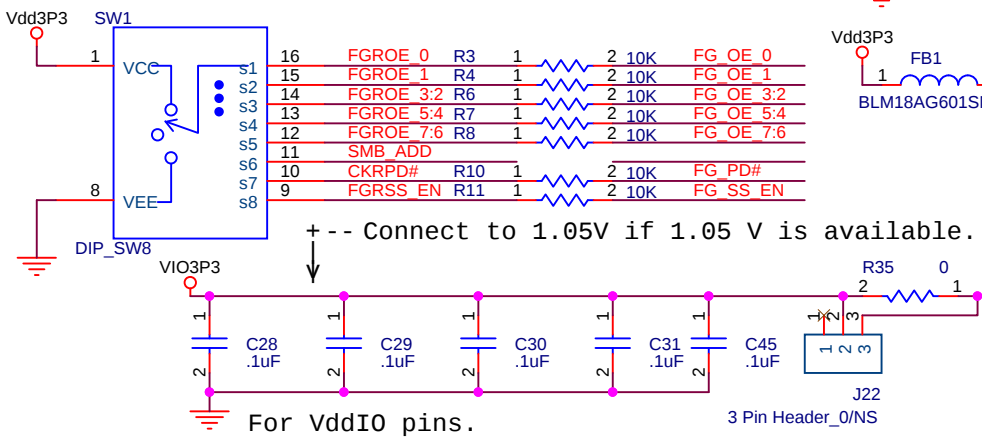


SCLK_3.3
SDATA_3.3

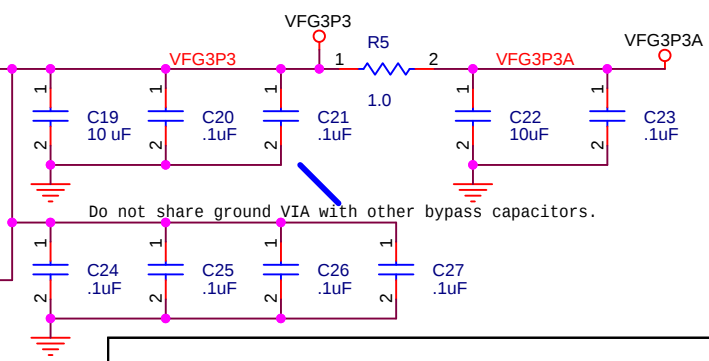


Test load

s5:0 1 = Stop low/low, 0 = Running
s6: 1 = Add 0xD4, 0 = Add 0xD0
s7: 1 = Enable, 0 = Pwr Dwn
s8: 1 = -0.5% Spread, MID = -.25%, 0 = No Spread



For VddIO pins.



Integrated Device Technology		
San Jose, CA		
Size A	Document Number 9FGL0841_EVB	Rev 0.3
Date: Friday, April 06, 2018	Sheet 1	of 2

