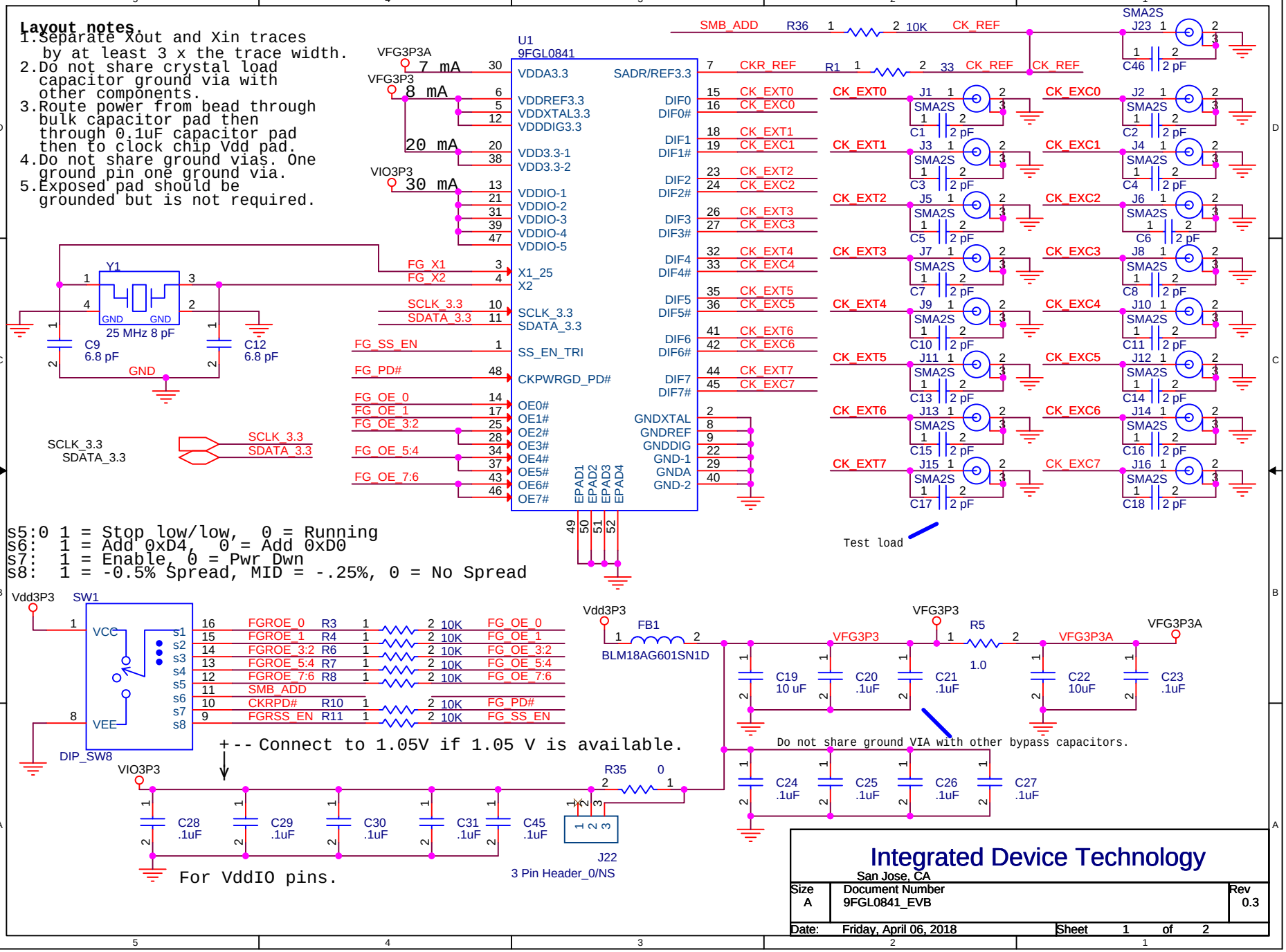
Layout notes.
1. Separate Xout and Xin traces by at least 3 x the trace width.
2. Do not share crystal load capacitor ground via with other components.
3. Route power from bead through bulk capacitor pad then through 0.1uF capacitor pad then to clock chip Vdd pad.
4. Do not share ground vias. One ground pin one ground via.
5. Exposed pad should be grounded but is not required.



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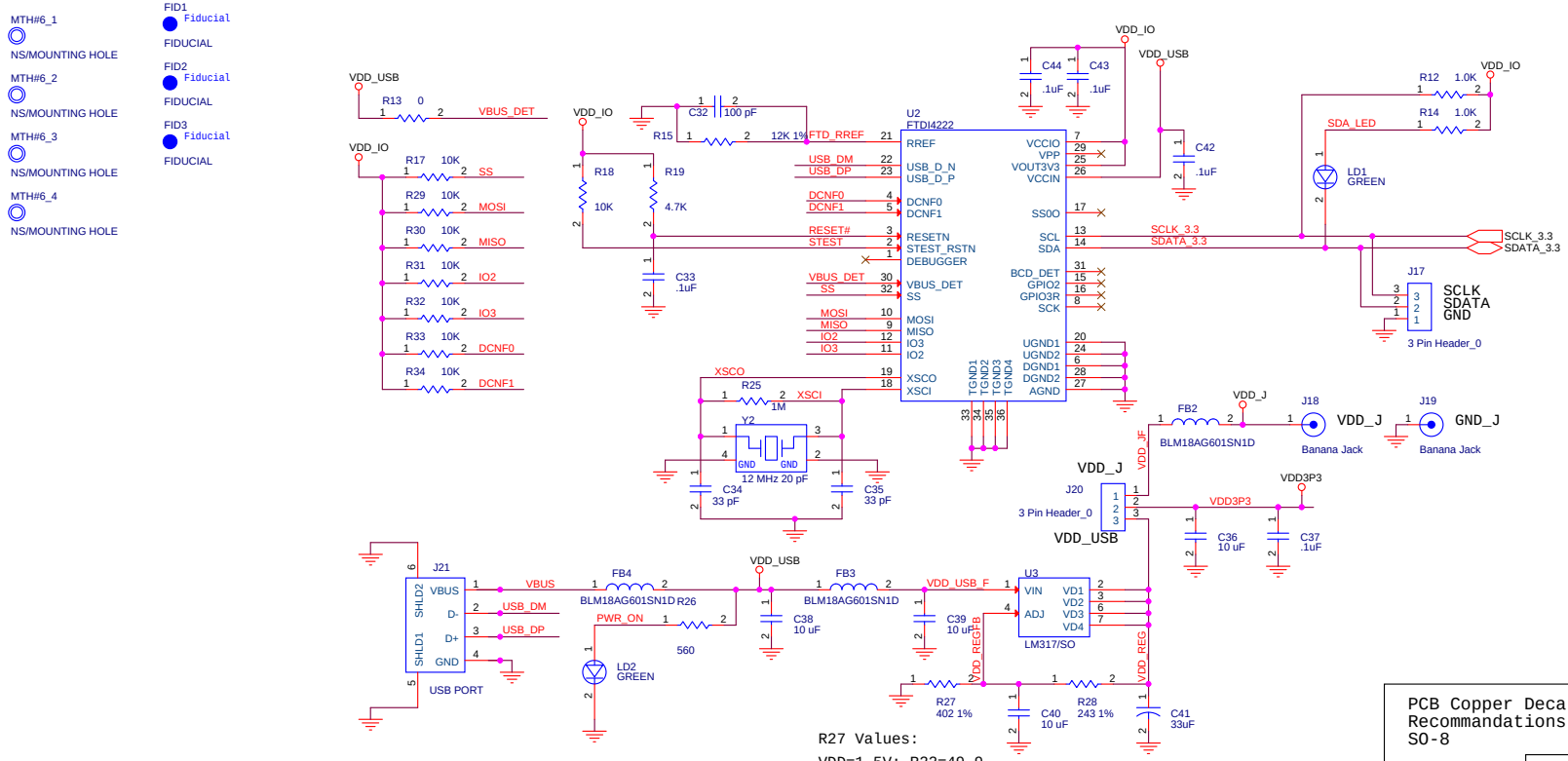
Size	Document Number	Rev
A	9FGL0841_EVB	0.3

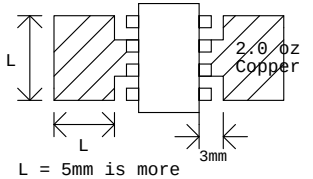
Date: Friday, April 06, 2018 Sheet 1 of 2



R27 Values:

VDD=1.5V: R22=49.9
VDD=1.8V: R22=107
VDD=2.5V: R22=243
VDD=3.3V: R22=402

PCB Copper Decal Recommandations for LM317LD SO-8



L = 5mm is more than enough

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Size	Document Number	Rev
B	USB_SCH	0.1

Date: Friday, April 06, 2018 Sheet 2 of