**Layout notes.**

1. Separate Xout and Xin traces by at least 3 x the trace width.
2. Do not share crystal load capacitor ground via with other components.
3. Route power from bead through bulk capacitor pad then to clock chip Vdd pad.
4. Do not share ground via. One ground pin one ground via.
5. Exposed pad should be grounded but is not required.

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**S4**: 0 = Stop low/low, 0 = Running
**S5**: No connect
**S6**: 1 = Add 0x0D, 0 = Add 0x0D
**S7**: 1 = Enable, 0 = Pwr Dwn
**S8**: 1 = -0.5% Spread, MID = -.25%, 0 = No Spread
R27 Values:

- VDD=1.5V: R22=49Ω
- VDD=1.8V: R22=107Ω
- VDD=2.5V: R22=243Ω
- VDD=3.3V: R22=402Ω

L = 5mm is more than enough.