

Smart Configurator for RX Plug-in in e2 studio 2023-01

Smart Configurator for RX V2.16.0

Release Note

Introduction

Thank you for using the Smart Configurator for RX.

This document describes the restrictions and points for caution. Read this document before using the product.

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1. Introduction

Smart Configurator is a utility for combining software to meet your needs. It supports the following three functions related to the embedding of Renesas drivers in your systems: importing middleware, generating driver code, and setting pins.

Smart Configurator for RX V2.16.0 is equivalent to Smart Configurator for RX plug-in in e² studio 2023-01.

1.1 System requirements

The operating environment is as follows.

1.1.1 Windows PC

- System: x64/x86 based processor
 - Windows® 11
 - Windows® 10 (64-bit version)
 - Windows® 8.1 (64-bit version)
- Memory capacity: We recommend 4 GB or more
- Capacity of hard disk: At least 300 MB of free space.
- Display: Graphics resolution should be at least 1024 x 768, and the mode should display at least 65,536 colors.
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)

1.1.2 Linux PC

Only Smart Configurator for RX plug-in in e² studio 2023-01 is supported on Linux OS.

- System: x64 based processor, 2 GHz or faster (with multicore CPUs)
 - Ubuntu 22.04 LTS Desktop (64-bit version)
 - Ubuntu 20.04 LTS Desktop (64-bit version)
- Memory capacity: We recommend 2 GB or more.
- Capacity of hard disk: At least 2 GB of free space.

1.1.3 Development Environments

- Renesas electronics Compiler for RX [CC-RX] V3.01.00 or later
- GCC for Renesas 4.8.4.201902 or later
- IAR Embedded Workbench 4.12.1 or later

2. Support List

2.1 Support Devices List

Below is a list of devices supported by the Smart Configurator for RX V2.16.0.

Table 2-1 Support Devices

Group (HW Manual number)	PIN	Device name
RX110 Group (R01UH0421EJ0120)	36pin	R5F5110HAXLM, R5F5110JAXLM, R5F51101AXLM, R5F51103AXLM
	40pin	R5F51101AXNF, R5F51103AXNF, R5F5110HAXNF, R5F5110JAXNF
	48pin	R5F51101AXNE, R5F51103AXNE, R5F51104AXNE, R5F51105AXNE, R5F5110JAXNE, R5F51101AXFL, R5F51103AXFL, R5F51104AXFL, R5F51105AXFL, R5F5110JAXFL
	64pin	R5F51101AXLF, R5F51103AXLF, R5F51104AXLF, R5F51105AXLF, R5F5110JAXLF, R5F51101AXFK, R5F51103AXFK, R5F51104AXFK, R5F51105AXFK, R5F5110JAXFK, R5F51101AXFM, R5F51103AXFM, R5F51104AXFM, R5F51105AXFM, R5F5110JAXFM
RX111 Group (R01UH0365EJ0130)	36pin	R5F51111AXLM, R5F51113AXLM, R5F5111JAXLM
	40pin	R5F51111AXNF, R5F51113AXNF, R5F5111JAXNF
	48pin	R5F51111AXFL, R5F51113AXFL, R5F51114AXFL, R5F51115AXFL, R5F51116AXFL, R5F51117AXFL, R5F51118AXFL, R5F5111JAXFL, R5F51111AXNE, R5F51113AXNE, R5F51114AXNE, R5F51115AXNE, R5F51116AXNE, R5F51117AXNE, R5F51118AXNE, R5F5111JAXNE
	64pin	R5F51111AXFM, R5F51113AXFM, R5F51114AXFM, R5F51115AXFM, R5F51116AXFM, R5F51117AXFM, R5F51118AXFM, R5F5111JAXFM, R5F51111AXFK, R5F51113AXFK, R5F51114AXFK, R5F51115AXFK, R5F51116AXFK, R5F51117AXFK, R5F51118AXFK, R5F5111JAXFK, R5F51111AXLF, R5F51113AXLF, R5F51114AXLF, R5F51115AXLF, R5F51116AXLF, R5F51117AXLF, R5F51118AXLF, R5F5111JAXLF
RX113 Group (R01UH0448EJ0110)	64pin	R5F51135AXFM, R5F51136AXFM, R5F51137AXFM, R5F51138AXFM
	100pin	R5F51135AXLJ, R5F51136AXLJ, R5F51137AXLJ, R5F51138AXLJ, R5F51135AXFP, R5F51136AXFP, R5F51137AXFP, R5F51138AXFP
RX130 Group (R01UH0560EJ0200)	48pin	R5F51303AXFL, R5F51305AXFL, R5F51303AXNE, R5F51305AXNE, R5F51306AXNE, R5F51306AXFL, R5F51307AXNE, R5F51307AXFL, R5F51308AXNE, R5F51308AXFL, R5F51306BxFL
	64pin	R5F51303AXFM, R5F51305AXFM, R5F51303AXFK, R5F51305AXFK, R5F51306AXFK, R5F51306AXFM, R5F51307AXFK, R5F51307AXFM, R5F51308AXFK, R5F51308AXFM, R5F51308AXFK, R5F51308AXFM, R5F51306BxFK, R5F51306BxFM
	80pin	R5F51303AXFN, R5F51305AXFN, R5F51306AXFN, R5F51306BxFN
	100pin	R5F51305AXFP, R5F51306AXFP, R5F51307AXFP, R5F51308AXFP, R5F51305BxFP, R5F51306BxFP
RX13T Group (R01UH0822EJ0100)	32pin	R5F513T3AXFJ, R5F513T5AXFJ, R5F513T3AXNH, R5F513T5AXNH
	48pin	R5F513T5AXFL, R5F513T3AXFL, R5F513T5AXNE, R5F513T3AXNE
RX230 Group (R01UH0496EJ0110)	48pin	R5F52305AXNE, R5F52306AXNE, R5F52305AXFL, R5F52306AXFL
	64pin	R5F52305AXND, R5F52306AXND, R5F52305AXFM, R5F52306AXFM, R5F52305AXLF, R5F52306AXLF
	100pin	R5F52305AXLA, R5F52306AXLA, R5F52305AXFP, R5F52306AXFP

Table 2-2 Support Devices

Group (HW Manual number)	PIN	Device name
RX231 Group (R01UH0496EJ0110)	48pin	R5F52315AxNE, R5F52316AxNE, R5F52317AxNE, R5F52318AxNE, R5F52315CxNE, R5F52316CxNE, R5F52317BxNE, R5F52318BxNE, R5F52315AxFL, R5F52316AxFL, R5F52317AxFL, R5F52318AxFL, R5F52315CxFL, R5F52316CxFL, R5F52317BxFL, R5F52318BxFL
	64pin	R5F52315AxND, R5F52316AxND, R5F52317AxND, R5F52318AxND, R5F52315CxND, R5F52316CxND, R5F52317BxND, R5F52318BxND, R5F52315AxFM, R5F52316AxFM, R5F52317AxFM, R5F52318AxFM, R5F52315CxFM, R5F52316CxFM, R5F52317BxFM, R5F52318BxFM, R5F52315CxLF, R5F52316CxLF
	100pin	R5F52315AxLA, R5F52316AxLA, R5F52317AxLA, R5F52318AxLA, R5F52315CxLA, R5F52316CxLA, R5F52317BxLA, R5F52318BxLA, R5F52315AxFP, R5F52316AxFP, R5F52317AxFP, R5F52318AxFP, R5F52315CxFP, R5F52316CxFP, R5F52317BxFP, R5F52318BxFP
RX23E-A Group (R01UH0801EJ0100)	40pin	R5F523E5AxNF, R5F523E6AxNF, R5F523E5SxNF, R5F523E6SxNF
	48pin	R5F523E5AxFL, R5F523E6AxFL, R5F523E5SxFL, R5F523E6SxFL
RX23T Group (R01UH0520EJ0110)	48pin	R5F523T3AxFL, R5F523T5AxFL
	52pin	R5F523T5AxFD, R5F523T3AxFD
	64pin	R5F523T5AxFM, R5F523T3AxFM
RX23W Group (R01UH0823EJ0100)	56pin	R5F523W8BxNG, R5F523W8AxNG, R5F523W7BxNG, R5F523W7AxNG
	83pin	R5F523W8CxLN, R5F523W8DxLN
	85pin	R5F523W7AxBL, R5F523W8AxBL, R5F523W8BxBL, R5F523W7BxBL
RX24T Group (R01UH0576EJ0200)	64pin	R5F524TAAxFM, R5F524T8AxFM, R5F524TAAxFK, R5F524T8AxFK
	80pin	R5F524TAAxFF, R5F524T8AxFF, R5F524TAAxFN, R5F524T8AxFN
	100pin	R5F524TCAxFP, R5F524T8AxFP, R5F524TBAxFP, R5F524TEAxFP, R5F524TAAxFP
RX24U Group (R01UH0658EJ0100)	100pin	R5F524UEAxFP, R5F524UCAxFP, R5F524UBAxFP
	144pin	R5F524UEAxFB, R5F524UBAxFB, R5F524UCAxFB
RX64M Group (R01UH0377EJ0110)	100pin	R5F564MFCxFP, R5F564MFCxLJ, R5F564MFDxFP, R5F564MFDxLJ, R5F564MGCxFP, R5F564MGCxLJ, R5F564MGDxFP, R5F564MGDxLJ, R5F564MJCxFP, R5F564MJCxLJ, R5F564MJDxFP, R5F564MJDxLJ, R5F564MLCxFP, R5F564MLCxLJ, R5F564MLDxFP, R5F564MLDxLJ
	144/145pin	R5F564MFCxFB, R5F564MFCxLK, R5F564MFDxFB, R5F564MFDxLK, R5F564MGCxFB, R5F564MGCxLK, R5F564MGDxFB, R5F564MGDxLK, R5F564MJCxFB, R5F564MJCxLK, R5F564MJDxFB, R5F564MJDxLK, R5F564MLCxFB, R5F564MLCxLK, R5F564MLDxFB, R5F564MLDxLK
	176/177pin	R5F564MFDxFC, R5F564MFDxBG, R5F564MFDxLC, R5F564MFCxFC, R5F564MFCxBG, R5F564MFCxLC, R5F564MGDxFC, R5F564MGDxBG, R5F564MGDxLC, R5F564MGCxFC, R5F564MGCxBG, R5F564MGCxLC, R5F564MJDxFC, R5F564MJDxBG, R5F564MJDxLC, R5F564MJCxFC, R5F564MJCxBG, R5F564MJCxLC, R5F564MLDxFC, R5F564MLDxBG, R5F564MLDxLC, R5F564MLCxFC, R5F564MLCxBG, R5F564MLCxFC

Table 2-3 Support Devices

Group (HW Manual number)	PIN	Device name
RX65N Group (R01UH0590EJ0210)	100pin	R5F565N9AxLJ, R5F565N9BxLJ, R5F565N9ExLJ, R5F565N9FxLJ, R5F565N7AxLJ, R5F565N7BxLJ, R5F565N7ExLJ, R5F565N7FxLJ, R5F565N4AxLJ, R5F565N4BxLJ, R5F565N4ExLJ, R5F565N4FxLJ, R5F565N9AxFP, R5F565N9BxFP, R5F565N9ExFP, R5F565N9FxFP, R5F565N7AxFP, R5F565N7BxFP, R5F565N7ExFP, R5F565N7FxFP, R5F565N4AxFP, R5F565N4BxFP, R5F565N4ExFP, R5F565N4FxFP, R5F565NCHxLJ, R5F565NCDxLJ, R5F565NEHxLJ, R5F565NEDxLJ, R5F565NCHxFP, R5F565NCDxFP, R5F565NEHxFP, R5F565NEDxFP
	144/145 pin	R5F565N9AxFB, R5F565N9BxFB, R5F565N9ExFB, R5F565N9FxFB, R5F565N7AxFB, R5F565N7BxFB, R5F565N7ExFB, R5F565N7FxFB, R5F565N4AxFB, R5F565N4BxFB, R5F565N4ExFB, R5F565N4FxFB, R5F565NCHxFB, R5F565NCDxFB, R5F565NEHxFB, R5F565NEDxFB, R5F565N9AxLK, R5F565N9BxLK, R5F565N9ExLK, R5F565N9FxLK, R5F565N7AxLK, R5F565N7BxLK, R5F565N7ExLK, R5F565N7FxLK, R5F565N4AxLK, R5F565N4BxLK, R5F565N4ExLK, R5F565N4FxLK, R5F565NCHxLK, R5F565NCDxLK, R5F565NEHxLK, R5F565NEDxLK
	176/177 pin	R5F565NCHxBG, R5F565NCDxBG, R5F565NEHxBG, R5F565NEDxBG, R5F565NCHxFC, R5F565NCDxFC, R5F565NEHxFC, R5F565NEDxFC, R5F565NCHxLC, R5F565NCDxLC, R5F565NEHxLC, R5F565NEDxLC
RX651 Group (R01UH0590EJ0210)	64pin	R5F5651CHxFM, R5F56514FxFM, R5F5651EHxFM, R5F5651CDxFM, R5F56514FxBP, R5F56514BxFM, R5F56519FxBP, R5F5651CDxBP, R5F5651EDxBP, R5F5651EDxFM, R5F56517BxBP, R5F5651EHxBP, R5F56519BxBP, R5F56517FxBP, R5F5651CHxBP, R5F56519FxFM, R5F56517BxFM, R5F56514BxBP, R5F56519BxFM, R5F56517FxFM
	100pin	R5F56519AxLJ, R5F56519BxLJ, R5F56519ExLJ, R5F56519FxLJ, R5F56517AxLJ, R5F56517BxLJ, R5F56517ExLJ, R5F56517FxLJ, R5F56514AxLJ, R5F56514BxLJ, R5F56514ExLJ, R5F56514FxLJ, R5F56519AxFP, R5F56519BxFP, R5F56519ExFP, R5F56519FxFP, R5F56517AxFP, R5F56517BxFP, R5F56517ExFP, R5F56517FxFP, R5F56514AxFP, R5F56514BxFP, R5F56514ExFP, R5F56514FxFP
	144/145 pin	R5F56519AxFB, R5F56519BxFB, R5F56519ExFB, R5F56519FxFB, R5F56517AxFB, R5F56517BxFB, R5F56517ExFB, R5F56517FxFB, R5F56514AxFB, R5F56514BxFB, R5F56514ExFB, R5F56514FxFB, R5F5651CDxFB, R5F5651CHxFB, R5F5651EDxFB, R5F5651EHxFB, R5F56519AxLK, R5F56519BxLK, R5F56519ExLK, R5F56519FxLK, R5F56517AxLK, R5F56517BxLK, R5F56517ExLK, R5F56517FxLK, R5F56514AxLK, R5F56514BxLK, R5F56514ExLK, R5F56514FxLK, R5F5651CDxLK, R5F5651CHxLK, R5F5651EDxLK, R5F5651EHxLK
	176/177 pin	R5F5651CDxBG, R5F5651CDxFC, R5F5651CHxBG, R5F5651CHxFC, R5F5651EDxBG, R5F5651EDxFC, R5F5651EHxBG, R5F5651EHxFC, R5F5651CDxLC, R5F5651CHxLC, R5F5651EDxLC, R5F5651EHxLC
RX66N Group (R01UH0825EJ0100)	100pin	R5F566NNDxFP, R5F566NNHxFP, R5F566NDDxFP, R5F566NDHxFP
	144pin	R5F566NNDxFB, R5F566NNHxFB, R5F566NDDxFB, R5F566NDHxFB
	145pin	R5F566NNDxLK, R5F566NNHxLK, R5F566NDDxLK, R5F566NDHxLK
	176pin	R5F566NNDxFC, R5F566NNHxFC, R5F566NDDxFC, R5F566NDHxFC, R5F566NNDxBG, R5F566NNHxBG, R5F566NDDxBG, R5F566NDHxBG
	244pin	R5F566NNDxBD, R5F566NNHxBD, R5F566NDDxBD, R5F566NDHxBD

Table 2-4 Support Devices

Group (HW Manual number)	PIN	Device name
RX66T Group (R01UH0749EJ0120)	48pin	R5F566TABxFL, R5F566TAFxFL, R5F566TEBxFL, R5F566TEFxFL
	64pin	R5F566TAAxFM, R5F566TAExFM, R5F566TEAxFM, R5F566TEExFM
	80pin	R5F566TAAxFF, R5F566TAExFF, R5F566TEAxFF, R5F566TEExFF, R5F566TAAxFN, R5F566TAExFN, R5F566TEAxFN, R5F566TEExFN
	100pin	R5F566TKCxFP, R5F566TAExFP, R5F566TFFxFP, R5F566TFCxFP, R5F566TFExFP, R5F566TFBxFP, R5F566TFAxFP, R5F566TABxFP, R5F566TAFxFP, R5F566TEFxFP, R5F566TKFxFP, R5F566TKGxFP, R5F566TKAxFP, R5F566TKExFP, R5F566TKBxFP, R5F566TEBxFP, R5F566TEExFP, R5F566TEAxFP, R5F566TAAxFP, R5F566TFGxFP
	112pin	R5F566TAAxFH, R5F566TAExFH, R5F566TEExFH, R5F566TEAxFH
	144pin	R5F566TKCxFB, R5F566TFGxFB, R5F566TFCxFB, R5F566TKGxFB
RX71M Group (R01UH0493EJ0110)	100pin	R5F571MLCxFP, R5F571MLDxFP, R5F571MLGxFP, R5F571MLHxFP, R5F571MJCxFP, R5F571MJDxFP, R5F571MJGxFP, R5F571MJHxFP, R5F571MGCxFP, R5F571MGDxFP, R5F571MGGxFP, R5F571MGHxFP, R5F571MFCxFP, R5F571MFDxFP, R5F571MFGxFP, R5F571MFHxFP, R5F571MLCxLJ, R5F571MLDxLJ, R5F571MLGxLJ, R5F571MLHxLJ, R5F571MJCxLJ, R5F571MJDxLJ, R5F571MJGxLJ, R5F571MJHxLJ, R5F571MGCxLJ, R5F571MGDxLJ, R5F571MGGxLJ, R5F571MGHxLJ, R5F571MFCxLJ, R5F571MFDxLJ, R5F571MFGxLJ, R5F571MFHxLJ
	144/145pin	R5F571MLCxLK, R5F571MLDxLK, R5F571MLGxLK, R5F571MLHxLK, R5F571MJCxLK, R5F571MJDxLK, R5F571MJGxLK, R5F571MJHxLK, R5F571MGCxLK, R5F571MGDxLK, R5F571MGGxLK, R5F571MGHxLK, R5F571MFCxLK, R5F571MFDxLK, R5F571MFGxLK, R5F571MFHxLK, R5F571MLCxFB, R5F571MLDxFB, R5F571MLGxFB, R5F571MLHxFB, R5F571MJCxFB, R5F571MJDxFB, R5F571MJGxFB, R5F571MJHxFB, R5F571MGCxFB, R5F571MGDxFB, R5F571MGGxFB, R5F571MGHxFB, R5F571MFCxFB, R5F571MFDxFB, R5F571MFGxFB, R5F571MFHxFB
	176/177pin	R5F571MLCxFC, R5F571MLDxFC, R5F571MLGxFC, R5F571MLHxFC, R5F571MJCxFC, R5F571MJDxFC, R5F571MJGxFC, R5F571MJHxFC, R5F571MGCxFC, R5F571MGDxFC, R5F571MGGxFC, R5F571MGHxFC, R5F571MFCxFC, R5F571MFDxFC, R5F571MFGxFC, R5F571MFHxFC, R5F571MLCxLC, R5F571MLDxLC, R5F571MLGxLC, R5F571MLHxLC, R5F571MJCxLC, R5F571MJDxLC, R5F571MJGxLC, R5F571MJHxLC, R5F571MGCxLC, R5F571MGDxLC, R5F571MGGxLC, R5F571MGHxLC, R5F571MFCxLC, R5F571MFDxLC, R5F571MFGxLC, R5F571MFHxLC, R5F571MLCxBG, R5F571MLDxBG, R5F571MLGxBG, R5F571MLHxBG, R5F571MJCxBG, R5F571MJDxBG, R5F571MJGxBG, R5F571MJHxBG, R5F571MGCxBG, R5F571MGDxBG, R5F571MGGxBG, R5F571MGHxBG, R5F571MFCxBG, R5F571MFDxBG, R5F571MFGxBG, R5F571MFHxBG
RX72M Group (R01UH0804EJ0110)	100pin	R5F572MDDxFP, R5F572MDHxFP, R5F572MNDxFP, R5F572MNHxFP
	144pin	R5F572MDDxFB, R5F572MDHxFB, R5F572MNDxFB, R5F572MNHxFB
	176pin	R5F572MNHxFC, R5F572MDDxBG, R5F572MNDxFC, R5F572MDHxBG, R5F572MDDxFC, R5F572MNHxBG, R5F572MNDxBG, R5F572MDHxFC
	224pin	R5F572MDDxBD, R5F572MDHxBD, R5F572MNHxBD, R5F572MNDxBD

Table 2-5 Support Devices

Group (HW Manual number)	PIN	Device name
RX72N Group (R01UH0824EJ0100)	100pin	R5F572NNDxFP, R5F572NNHxFP, R5F572NDDxFP, R5F572NDHxFP
	144pin	R5F572NNDxFB, R5F572NNHxFB, R5F572NDDxFB, R5F572NDHxFB
	145pin	R5F572NNDxLK, R5F572NNHxLK, R5F572NDDxLK, R5F572NDHxLK
	176pin	R5F572NNDxFC, R5F572NNHxFC, R5F572NDDxFC, R5F572NDHxFC, R5F572NNDxBG, R5F572NNHxBG, R5F572NDDxBG, R5F572NDHxBG
	224pin	R5F572NNDxBD, R5F572NNHxBD, R5F572NDDxBD, R5F572NDHxBD
RX72T Group (R01UH0803EJ0100)	100pin	R5F572TKExFP, R5F572TFFxFP, R5F572TKFxFP, R5F572TFGxFP, R5F572TKCxFP, R5F572TFBxFP, R5F572TFExFP, R5F572TFCxFP, R5F572TFAxFP, R5F572TKAxFP, R5F572TKBxFP, R5F572TKGxFP
	144pin	R5F572TKGxFB, R5F572TKCxFB, R5F572TFGxFB, R5F572TFCxFB
RX671 Group (R01UH0899EJ0100)	48pin	R5F5671EHxNE, R5F5671EDxNE, R5F5671CHxNE, R5F5671CDxNE, R5F56719HxNE, R5F56719DxNE
	64pin	R5F5671EHxFM, R5F5671EDxFM, R5F5671CHxFM, R5F5671CDxFM, R5F56719HxFM, R5F56719DxFM, R5F5671EHxBP, R5F5671EDxBP, R5F5671CHxBP, R5F5671CDxBP, R5F56719HxBP, R5F56719DxBP
	100pin	R5F5671EHxFP, R5F5671EDxFP, R5F5671CHxFP, R5F5671CDxFP, R5F56719HxFP, R5F56719DxFP, R5F5671EHxLJ, R5F5671EDxLJ, R5F5671CHxLJ, R5F5671CDxLJ, R5F56719HxLJ, R5F56719DxLJ
	144pin	R5F5671EHxFB, R5F5671EDxFB, R5F5671CHxFB, R5F5671CDxFB, R5F56719HxFB, R5F56719DxFB
	145pin	R5F5671EHxLE, R5F5671EDxLE, R5F5671CHxLE, R5F5671CDxLE, R5F56719HxLE, R5F56719DxLE, R5F5671EHxLK, R5F5671EDxLK, R5F5671CHxLK, R5F5671CDxLK, R5F56719HxLK, R5F56719DxLK
RX140 Group (R01UH0905EJ0110)	32pin	R5F51403AxFJ, R5F51403AxNH
	48pin	R5F51403AxFL, R5F51403AxNE, R5F51405AxFL, R5F51405AxNE, R5F51405BxFL, R5F51405BxNE, R5F51406AxFL, R5F51406AxNE, R5F51406BxFL, R5F51406BxNE
	64pin	R5F51403AxFK, R5F51403AxFM, R5F51405AxFK, R5F51405AxFM, R5F51405BxFK, R5F51405BxFM, R5F51406AxFK, R5F51406AxFM, R5F51406BxFK, R5F51406BxFM
	80pin	R5F51405AxFN, R5F51405BxFN, R5F51406AxFN, R5F51406BxFN
RX660 Group (R01UH0937EJ0100)	48pin	R5F56609AxFL, R5F56609BxFL, R5F56604AxFL, R5F56604BxFL
	64pin	R5F56609AxFM, R5F56609BxFM, R5F56609CxFM, R5F56609DxFM R5F56604AxFM, R5F56604BxFM, R5F56604CxFM, R5F56604DxFM
	80pin	R5F56609AxFN, R5F56609BxFN, R5F56609CxFN, R5F56609DxFN R5F56604AxFN, R5F56604BxFN, R5F56604CxFN, R5F56604DxFN
	100pin	R5F56609AxFP, R5F56609BxFP, R5F56609CxFP, R5F56609DxFP R5F56609ExFP, R5F56609FxFP, R5F56609GxFP, R5F56609HxFP R5F56604AxFP, R5F56604BxFP, R5F56604CxFP, R5F56604DxFP R5F56604ExFP, R5F56604FxFP, R5F56604GxFP, R5F56604HxFP
	144pin	R5F56609AxFB, R5F56609BxFB, R5F56609CxFB, R5F56609DxFB R5F56609ExFB, R5F56609FxFB, R5F56609GxFB, R5F56609HxFB R5F56604AxFB, R5F56604BxFB, R5F56604CxFB, R5F56604DxFB R5F56604ExFB, R5F56604FxFB, R5F56604GxFB, R5F56604HxFB

2.2 Support Components List

Below is a list of Components supported by the Smart Configurator for RX V2.16.0.

Table 2-6 Support Components (RX100, RX200 family)

✓ : Support, - : Non-support

No	Components	Mode	RX100	RX111	RX113	RX130	RX13T	RX140	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
1	8-Bit Timer	-	-	-	✓	✓	-	✓	✓	✓	✓	✓	✓	
2	CRC Calculator	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
3	D-A Converter	-	-	✓	✓	✓	✓	✓	✓	-	✓	✓	✓	
4	DMA Controller	-	-	-	-	-	-	-	✓	✓	-	✓	-	
5	I2C Slave Mode	I2C mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		SMBus mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
6	I2C Master Mode	I2C mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		SMBus mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
7	LCD Controller	-	-	-	✓	-	-	-	-	-	-	-	-	
8	PWM Mode Timer	PWM mode 1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		PWM mode 2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
9	SCI/SCIF Clock Synchronous Mode	Transmission	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1, 2
		Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1, 2
		Transmission/Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1, 2
10	SCI/SCIF Asynchronous Mode	Transmission	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1
		Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1
		Transmission/Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1
		Multi-processor Transmission	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1
		Multi-processor Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1
		Multi-processor Transmission/Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1
11	SPI Clock Synchronous Mode	Slave transmit/receive	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Slave transmit only	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Master transmit/receive	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Master transmit only	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
12	SPI Operation Mode	Slave transmit/receive	✓	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	
		Slave transmit only	✓	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	
		Master transmit/receive	✓	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	
		Master transmit only	✓	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	
		Multi-master transmit/receive	✓	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	
		Multi-master transmit only	✓	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	
13	Event Link Controller	-	-	✓	✓	✓	-	✓	✓	✓	-	✓	-	
14	Watchdog Timer	-	✓	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	
15	Clock Frequency Accuracy Measurement Circuit	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	

Note 1. Refer to No 2 in Table 6-2

Note 2. Refer to No 3 in Table 6-2

Table 2-7 Support Components (RX100, RX200 family)

✓ : Support, - : Non-support

No	Components	Mode	RX110	RX111	RX113	RX130	RX13T	RX140	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
16	Group Scan Mode S12AD	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
17	Comparator	-	-	-	✓	✓	✓	✓	✓	-	-	✓	-	
18	Compare Match Timer	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
19	Single Scan Mode S12AD	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
20	Smart Card Interface Mode	Transmission	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Transmission/Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
21	Dead-time Compensation Counter	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	-	✓	
22	Data Transfer Controller	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 3
23	Data Operation Circuit	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
24	Normal Mode Timer	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
25	Buses	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
26	Programmable Pulse Generator	-	-	-	-	-	-	-	-	-	-	-	-	
27	Ports	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
28	Port Output Enable	-	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
29	Real Time Clock	Binary	✓	✓	✓	✓	-	✓	✓	-	-	✓	-	
		Calendar	✓	✓	✓	✓	-	✓	✓	-	-	✓	-	
30	Remote Control Signal Receiver	-	-	-	-	✓	-	-	-	-	-	-	-	
31	Low-Power Timer	-	-	-	✓	✓	-	✓	✓	✓	-	✓	-	
32	Phase Counting Mode Timer	16-Bit Phase Counting Mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Cascade Connection 32-Bit Phase Counting Mode	-	-	-	-	✓	-	-	-	✓	-	✓	
33	Interrupt Controller	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
34	General PWM Timer	Saw-wave PWM mode	-	-	-	-	-	-	-	-	✓	-	✓	Note 4
		Saw-wave one-shot pulse mode	-	-	-	-	-	-	-	-	✓	-	✓	Note 4
		Triangle-wave PWM mode 1	-	-	-	-	-	-	-	-	✓	-	✓	Note 4
		Triangle-wave PWM mode 2	-	-	-	-	-	-	-	-	✓	-	✓	Note 4
		Triangle-wave PWM mode 3	-	-	-	-	-	-	-	-	✓	-	✓	Note 4
35	Low Power Consumption	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
36	Complementary PWM Mode Timer	Complementary PWM mode 1	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Complementary PWM mode 2	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Complementary PWM mode 3	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
37	Continuous Scan Mode S12AD	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	

Note 3. Refer to No 6 in Table 6-1

Note 4. Refer to No 1 in Table 6-1

Table 2-8 Support Components (RX100, RX200 family)

✓ : Support, -: Non-support

No	Components	Mode	RX110	RX111	RX113	RX130	RX13T	RX140	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
38	Voltage Detection Circuit	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
39	Delta-Sigma Modulator Interface	Master	-	-	-	-	-	-	-	-	-	-	-	
		Slave	-	-	-	-	-	-	-	-	-	-	-	
40	Single Scan Mode DSAD	-	-	-	-	-	-	✓	-	✓	-	-	-	
41	Continuous Scan Mode DSAD	-	-	-	-	-	-	✓	-	✓	-	-	-	
42	Analog Front End	-	-	-	-	-	-	✓	-	✓	-	-	-	
43	Motor	3-Phase Brushless DC Motor	-	-	-	-	✓	-	-	-	✓	-	✓	
		2-Phase Stepping Motor (Fast Decay)	-	-	-	-	✓	-	-	-	✓	-	✓	
		2-Phase Stepping Motor (Slow Decay)	-	-	-	-	✓	-	-	-	✓	-	✓	

Table 2-9 Support Components (RX600, RX700 family)

✓: Support, -: Non-support

No	Components	Mode	RX64M	RX65N, RX651	RX66N	RX66T	RX660	RX671	RX71M	RX72M	RX72N	RX72T	Remarks
1	8-Bit Timer	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
2	CRC Calculator	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
3	D/A Converter	-	✓	✓	✓	✓	✓	-	✓	✓	✓	✓	
4	DMA Controller	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
5	I2C Slave Mode	I2C mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		SMBus mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
6	I2C Master Mode	I2C mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		SMBus mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
7	LCD Controller	-	-	-	-	-	-	-	-	-	-	-	
8	PWM Mode Timer	PWM mode 1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		PWM mode 2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
9	SCI/SCIF Clock Synchronous Mode	Transmission	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1, 2
		Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1, 2
		Transmission/Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1, 2
10	SCI/SCIF Asynchronous Mode	Transmission	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1
		Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1
		Transmission/Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1
		Multi-processor Transmission	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1
		Multi-processor Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1
		Multi-processor Transmission/Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 1
11	SPI Clock Synchronous Mode	Slave transmit/receive	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Slave transmit only	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Master transmit/receive	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Master transmit only	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
12	SPI Operation Mode	Slave transmit/receive	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Slave transmit only	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Slave receive only	-	-	-	-	✓	✓	-	-	-	-	
		Master transmit/receive	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Master transmit only	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Multi-master transmit/receive	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Multi-master transmit only	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
13	Event Link Controller	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
14	Watchdog Timer	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
15	Clock Frequency Accuracy Measurement Circuit	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	

Note 1. Refer to No 2 in Table 6-2

Note 2. Refer to No 3 in Table 6-2

Table 2-10 Support Components (RX600, RX700 family)

✓ : Support, - : Non-support

No	Components	Mode	RX64M	RX65N, RX651	RX66N	RX66T	RX660	RX671	RX71M	RX72M	RX72N	RX72T	Remarks
16	Group Scan Mode S12AD	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
17	Comparator	-	-	-	-	✓	✓	-	-	✓	-	✓	
18	Compare Match Timer	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
19	Single Scan Mode S12AD	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
20	Smart Card Interface Mode	Transmission	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Transmission/Reception	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
21	Dead-time Compensation Counter	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
22	Data Transfer Controller	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	Note 3
23	Data Operation Circuit	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
24	Normal Mode Timer	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
25	Buses	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
26	Programmable Pulse Generator	-	✓	✓	✓	-	-	✓	✓	-	✓	-	
27	Ports	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
28	Port Output Enable	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
29	Real Time Clock	Binary	✓	✓	✓	-	✓	✓	✓	-	✓	-	
		Calendar	✓	✓	✓	-	✓	✓	✓	-	✓	-	
30	Remote Control Signal Receiver	-	-	-	-	-	✓	✓	-	-	-	-	
31	Low-Power Timer	-	-	-	-	-	-	-	-	-	-	-	
32	Phase Counting Mode Timer	16-Bit Phase Counting Mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Cascade Connection 32-Bit Phase Counting Mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
33	Interrupt Controller	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
34	General PWM Timer	Saw-wave PWM mode	✓	-	✓	✓	-	-	✓	✓	✓	✓	Note 4
		Saw-wave one-shot pulse mode	✓	-	✓	✓	-	-	✓	✓	✓	✓	Note 4
		Triangle-wave PWM mode 1	✓	-	✓	✓	-	-	✓	✓	✓	✓	Note 4
		Triangle-wave PWM mode 2	✓	-	✓	✓	-	-	✓	✓	✓	✓	Note 4
		Triangle-wave PWM mode 3	✓	-	✓	✓	-	-	✓	✓	✓	✓	Note 4
35	Low Power Consumption	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
36	Complementary PWM Mode Timer	Complementary PWM mode 1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Complementary PWM mode 2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
		Complementary PWM mode 3	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
37	Continuous Scan Mode S12AD	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	

Note 3. Refer to No 6 in Table 6-1

Note 4. Refer to No 1 in Table 6-1

Table 2-11 Support Components (RX600, RX700 family)

✓ : Support, -: Non-support

No	Components	Mode	RX64M	RX65N, RX651	RX66N	RX66T	RX660	RX671	RX71M	RX72M	RX72N	RX72T	Remarks
38	Voltage Detection Circuit	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
39	Delta-Sigma Modulator Interface	Master	-	-	-	-	-	-	-	✓	-	-	
		Slave	-	-	-	-	-	-	-	✓	-	-	
40	Single Scan Mode DSAD	-	-	-	-	-	-	-	-	-	-	-	
41	Continuous Scan Mode DSAD	-	-	-	-	-	-	-	-	-	-	-	
42	Analog Front End	-	-	-	-	-	-	-	-	-	-	-	
43	Motor	3-Phase Brushless DC Motor	-	-	-	✓	-	-	-	✓	-	✓	
		2-Phase Stepping Motor (Fast Decay)	-	-	-	✓	-	-	-	✓	-	✓	
		2-Phase Stepping Motor (Slow Decay)	-	-	-	✓	-	-	-	✓	-	✓	

2.3 New support

2.3.1 BSP (Board Support Package) revision update

From Smart Configurator for RX V2.16.0, BSP rev7.21 is supported and will be added as default BSP when creating Smart Configurator project.

2.3.2 RX board feature update

From Smart Configurator for RX V2.16.0, 27 boards' info have been updated.

Table 2-12 List of board feature update

Index	Board name	Remark
1	RSKRX111_V1.02	Version update
2	RSKRX113_V1.02	Version update
3	RSKRX130_V1.02	Version update
4	RSKRX130-512KB_V1.03	Version update
5	RSKRX140_V1.01	Version update
6	RSKRX231_V1.02	Version update
7	RSKRX231B_V1.01	Version update
8	RSKRX23T_V1.02	Version update
9	RSKRX24T_V1.03	Version update
10	RSKRX24U_V1.03	Version update
11	RSK+RX64M_V1.02	Version update
12	RSK+RX65N_V1.02	Version update
13	RSK+RX65N-2MB_V1.05	Version update
14	RSK+RX65N-2MB(TSIP)_V1.02	Version update
15	RSKRX660_V1.01	Version update
16	RSKRX66T_V1.04	Version update
17	RSKRX66T(TSIP)_V1.01	Version update
18	RSK+RX671_V1.02	Version update
19	RSK+RX71M_V1.02	Version update
20	RSKRX72T_V1.02	Version update
21	RSKRX72T(TSIP)_V1.01	Version update
22	RSK+RX72M_V1.02	Version update
23	RSK+RX72M(TSIP)_V1.01	Version update
24	RSK+RX72N_V1.03	Version update
25	RSK+RX72N(TSIP)_V1.01	Version update
26	RSSKRX23W_V1.02	Version update

27	RSSKRX23W(TSIP)_V1.01	Version update
----	-----------------------	----------------

2.3.3 More boards are supported with software component (driver and middleware) recommend feature

From Smart Configurator for RX V2.16.0, the following 10 more boards are supported with software component (driver and middleware) recommended feature. When the user selects those boards, recommended software component can be seen from "Board" page.

- RSKRX111
- RSKRX113
- RSKRX130
- RSKRX130-512KB
- RSKRX23T
- RSKRX24T
- RSKRX24U
- CPUCardRX13T
- CPUCardRX24T
- RX66T CPU Card for CPU Evaluation

2.3.4 New support on the easy configuration of all unused pins in Port Component

From Smart Configurator RX V2.16.0, all unused pins in PORT component can be configured to output 0 / output 1 easily.

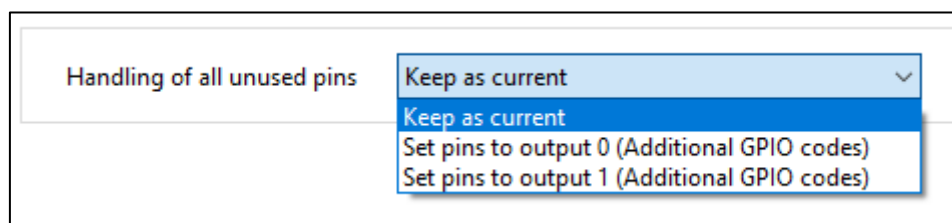


Figure 2-1 Easy configuration on the unused pins in Port Component

To decrease the current drawn, all unused pins are suggested to be configured into "input and add pull-up resistor" or "set to output" as mentioned in the Hardware User Manual. However, the previous version of Smart Configurator does not support the easy configuration for all unused pins in Port component.

With this new feature support, all unused pins can be configured effortlessly in Port component.

2.3.5 New support of Linux OS

From Smart Configurator for RX V2.16.0, Smart Configurator will be supported on Linux OS

Please refer to 1.1.2 Linux PC for the information of supported Linux.

2.3.6 New support of compare match output feature in Phase Counting Mode Timer component

From Smart Configurator for RX V2.16.0, compare match output feature has been supported in "Cascade Connection 32-Bit Phase Counting Mode" of Phase Counting Mode Timer Component.

With this new feature, "Output compare register" will be configured as default setting for TGRALW/TGRBLW register, and signals from MTIOC1A/MTIOC1B pin are able to output at the timing of compare match.

General register setting			
TGRALW	Output compare register	100	count
TGRBLW	Output compare register	100	count

Input/Output setting			
MTIOC1A pin	Output disabled	<input type="checkbox"/>	Use noise filter
MTIOC1B pin	Output disabled	<input type="checkbox"/>	Use noise filter

Figure 2-2 New support of compare match output feature in Phase Counting Mode Timer component

2.3.7 New support for BSP Rev7.21 expansion RAM settings

From Smart Configurator RXV2.16.0, by using the BSP Rev7.21 on e² studio Smart Configurator project, "BSP_CFG_EXPANSION_RAM_ENABLE" macro will be set to 1 for RX devices that support expansion RAM (e.g., RX66N, RX72N, RX72M). At the same time, sections will be added to the linker settings to allow expansion RAM to be used.

Do take note that "BSP_CFG_EXPANSION_RAM_ENABLE" will be set to 0 in CS+ Smart Configurator project due to tool's limitation. Please configure expansion RAM settings manually when enabling this macro in CS+.

2.3.8 Bank mode selection support for IAR project creation with Standalone Smart Configurator

From Smart Configurator for RX V2.16.0, user can configure the bank mode through the wizard page while creating IAR EWRX project with Standalone Smart Configurator, and corresponding Linear/Dual mode device will be automatically configured when loading the IAR project file generated by Smart Configurator into IAR EW for RX.

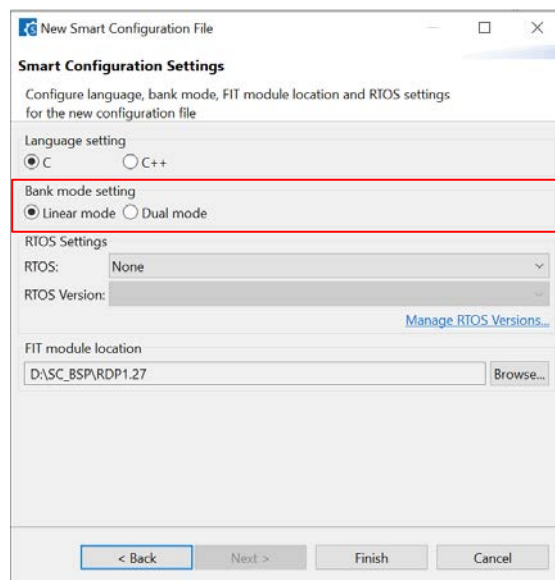


Figure 2-3 Bank mode selection on wizard page of IAR project creation

2.3.9 Language selection (C or C++) support for IAR project creation with Standalone Smart Configurator

From Smart Configurator for RX V2.16.0, user can configure the language setting (C or C++) through wizard page while creating IAR EWRX project with Standalone Smart Configurator, and when C++ language is selected, main.cpp file will also be generated together with the IAR project files.

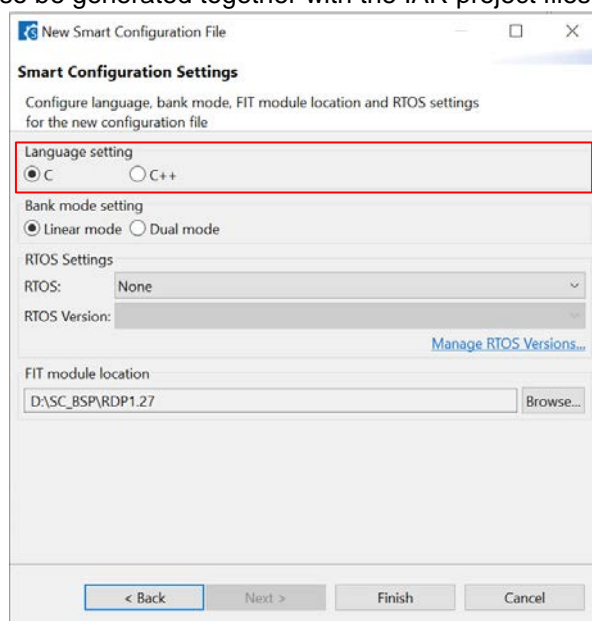


Figure 2-4 Language selection on the wizard page of IAR project creation

2.3.10 User code protection feature for Smart Configurator Code Generation component

For Smart Configurator for RX V2.15.0 or previous version, user code can be protected when user insert the user code into the fixed location defined inside the generated files of Code Generation component.

From Smart Configurator for RX V2.16.0, an enhanced user code protection feature has been implemented which allows user codes to be added to any locations with the specific tags (`/* Start user code */ ... /* End user code */`) as shown in **Figure 2-5**. Inserted user codes will be protected and automatically merged into generated files in the next code generation.

This feature will be available from Smart Configurator for RX Plug-in in e² studio 2023-01.

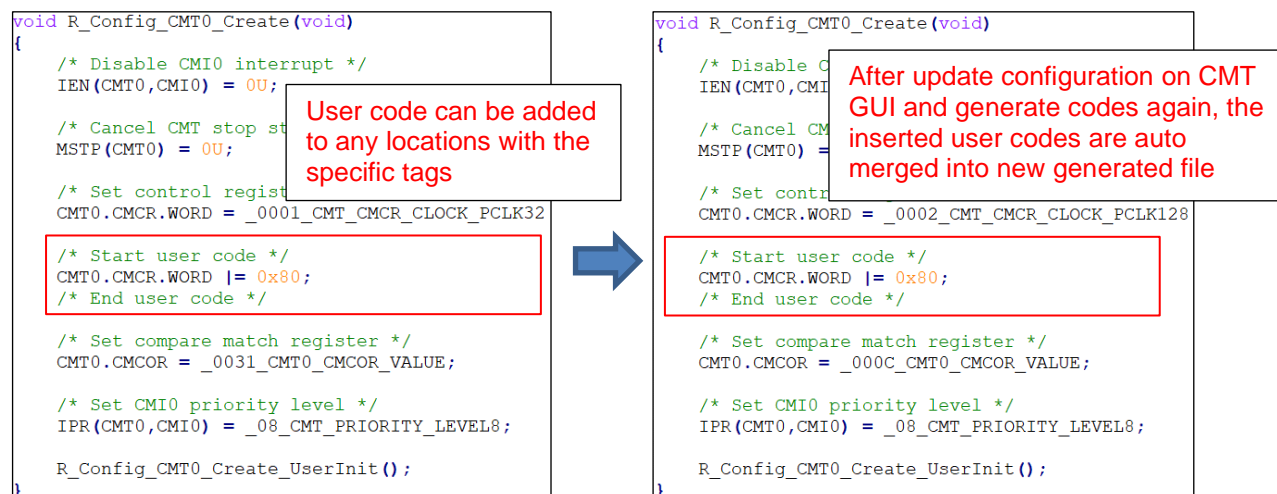


Figure 2-5 User code protection with auto merge

However, if the lines of generated codes before and after the inserted user codes are updated due to the new GUI configuration, merge conflict code will be generated out as shown in **Figure 2-6**.

(By upgrading the version of Smart Configurator, merge conflicts will be generated if the GUI configuration in new environment updated the lines of generated codes before and after the inserted user code.)

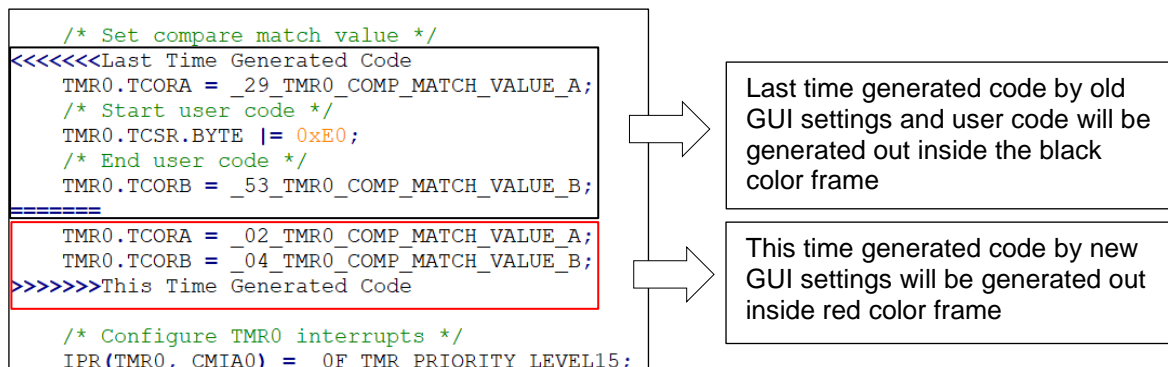


Figure 2-6 User code protection with merge conflict

As shown in **Figure 2-7**, conflict message will be generated out to the Smart Configurator console when the merge conflict occurs.

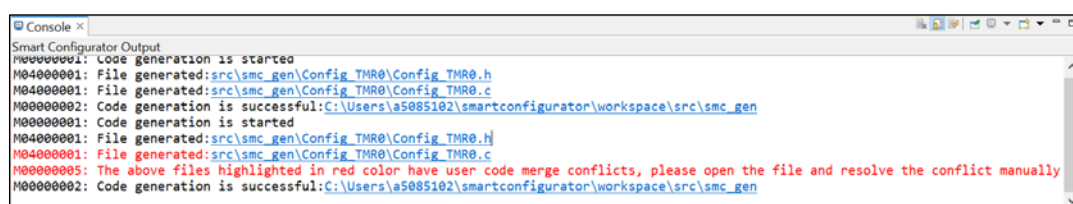


Figure 2-7 The merge conflict message outputted in the Smart Configurator console

To resolve this merge conflict, open the highlighted conflict files and follow the steps below to solve the merge conflicts manually.

- 1) Copy the user code that was generated in **Figure 2-8**.

```

/* Set compare match value */
<<<<<<<Last Time Generated Code
TMR0.TCORB = _29_TMR0_COMP_MATCH_VALUE_A;
/* Start user code */
TMR0.TCSR.BYTE |= 0xE0;
/* End user code */
TMR0.TCORB = _53_TMR0_COMP_MATCH_VALUE_B;
=====
TMR0.TCORB = _02_TMR0_COMP_MATCH_VALUE_A;
TMR0.TCORB = _04_TMR0_COMP_MATCH_VALUE_B;
>>>>>>>This Time Generated Code

/* Configure TMR0 interrupts */
IPR(TMR0, CMIA0) = 0F_TMR_PRIORITY_LEVEL15;
  
```

Figure 2-8 Generated conflict code

- 2) Paste the user code into the new position (inside the code that was generated by new GUI settings) as shown in **Figure 2-9**.

```

/* Set compare match value */
<<<<<<Last Time Generated Code
    TMR0.TCOR_A = _29_TMR0_COMP_MATCH_VALUE_A;
/* Start user code */
    TMR0.TCSR.BYTE |= 0xE0;
/* End user code */
    TMR0.TCOR_B = _53_TMR0_COMP_MATCH_VALUE_B;
=====
    TMR0.TCOR_A = _02_TMR0_COMP_MATCH_VALUE_A;
/* Start user code */
    TMR0.TCSR.BYTE |= 0xE0;
/* End user code */
    TMR0.TCOR_B = _04_TMR0_COMP_MATCH_VALUE_B;
>>>>>>This Time Generated Code

```

Figure 2-9 Generated conflict code

- 3) Remove last time generated code and the conflicts comment (<<<<<<Last Time Generated Code, ===== and >>>>>>This Time Generated Code) as shown in **Figure 2-10**.

```

/* Set compare match value */
TMR0.TCOR_A = _02_TMR0_COMP_MATCH_VALUE_A;
/* Start user code */
TMR0.TCSR.BYTE |= 0xE0;
/* End user code */
TMR0.TCOR_B = _04_TMR0_COMP_MATCH_VALUE_B;

```

Figure 2-10 The codes after resolving the merge conflict

3. Changes

This chapter describes changes to the Smart Configurator for RX V2.16.0.

3.1 Correction of issues/limitations

Table 3-1 List of Correction of issues/limitations (RX100, RX200 Family) ✓ : Applicable, -: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX13T	RX140	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
1	Fixed the input range of deadtime in Motor component	-	-	-	-	✓	-	-	-	✓	-	✓	
2	Fixed the displayed value inside the generated report when using Motor component	-	-	-	-	✓	-	-	-	✓	-	✓	

Table 3-2 List of Correction of issues/limitations (RX600, RX700 Family) ✓ : Applicable, -: Not Applicable

No	Description	RX64M	RX65N, RX651	RX66N	RX66T	RX660	RX671	RX71M	RX72M	RX72N	RX72T	Remarks
1	Fixed the input range of deadtime in Motor component	-	-	-	✓	-	-	-	✓	-	✓	
2	Fixed the displayed value inside the generated report when using Motor component	-	-	-	✓	-	-	-	✓	-	✓	

3.1.1 Fixed the input range of deadtime in Motor component

When configuring the maximum input value for "Timer Operation Period" in Motor component, the input value range for dead time is wrong when "count" is being selected. This issue has been fixed from SC for RX V2.16.0

3.1.2 Fixed the displayed value inside the generated report when using Motor component

When generating report in Motor component, the value inside the generated report will remain as default value and not updating according to the GUI value. This issue has been fixed from SC for RX V2.16.0

3.2 Specification changes

Table 3-3 List of Specification changes (RX100, RX200 family)

○: Applicable, /: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX13T	RX140	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
1	P, P* and PResetPRG sections have been improved to be updated once by code generation in Smart Configurator	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
2	Layout of Smart Configurator Component Preference page has been improved for better user experience	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	

Table 3-4 List of Specification changes (RX600, RX700 family)

○: Applicable, /: Not Applicable

No	Description	RX64M	RX65N, RX651	RX66N	RX66T	RX660	RX671	RX71M	RX72M	RX72N	RX72T	Remarks
1	P, P* and PResetPRG sections have been improved to be updated once by code generation in Smart Configurator	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
2	Layout of Smart Configurator Component Preference page has been improved for better user experience	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	

3.2.1 P, P* and PResetPRG sections have been improved to be updated once by code generation in Smart Configurator

From Smart Configurator for RX V2.16.0, P, P* and PResetPRG sections will only update once by code generation in Smart Configurator.

Previous versions of Smart Configurator will always update the section setting if the code generation is being triggered. Section settings are not able to configure freely as it will be updated every time generating code. With this new feature, users can configure and keep the section setting.

Do take note that if BSP is updated into another newer version and generates code, section setting will be updated.

3.2.2 Layout of Smart Configurator Component Preference page has been improved for better user experience

From Smart Configurator RX V2.16.0, the layout for Smart Configurator Component Preferences page has been improved for better user experience of the "code generation behavior" feature. "Update configuration files" will be selected by default.

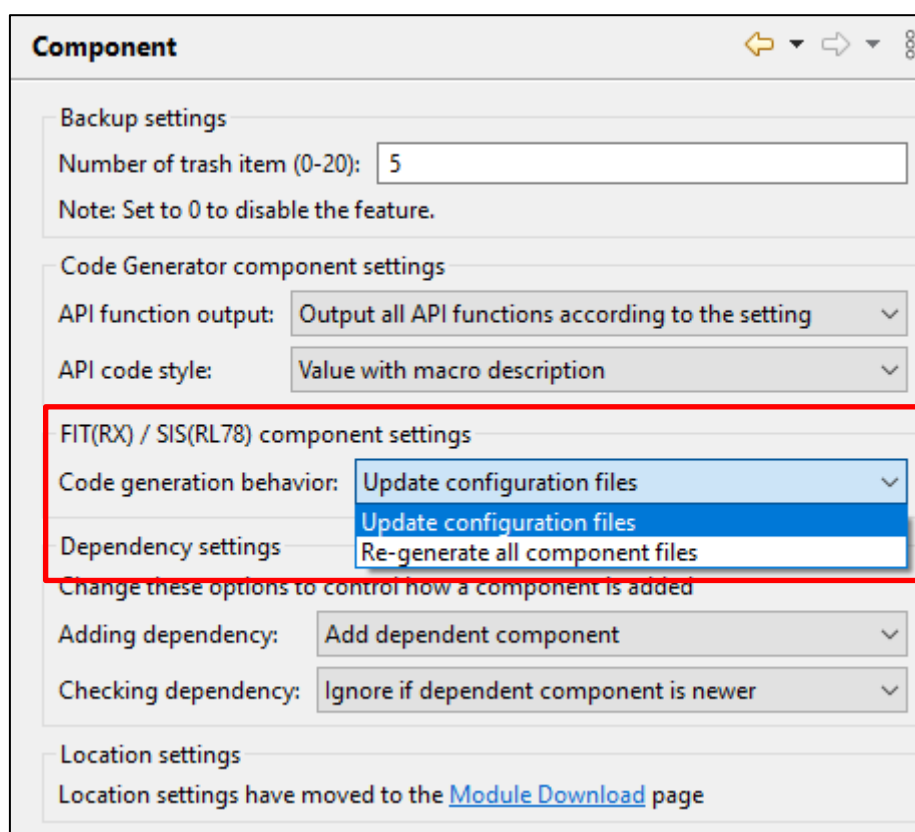


Figure 3-1 New layout for Smart Configurator Component Preference page

If "Update configuration files" is being selected and generate code, Smart Configurator will check whether the files are existing inside the user project. If the file exists, the file will not be overwritten. However, configuration files (e.g., xxx_config.h) will still be refreshed when code is generated.

If "Re-generate all component files" being selected and generate code, Smart Configurator does not check the existence of the file and the file will always be overwritten.

4. List of RENESAS TOOL NEWS AND TECHNICAL UPDATE

Below is a list of notifications delivered by RENESAS TOOL NEWS and TECHNICAL UPDATE.

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Sep. 1, 2017	R20TS0198	1. When using the I2C bus interface in slave mode https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx	RX130, RX64M, RX651, RX65N	V1.3.0
Apr. 1, 2018	R20TS0294	1. When using the bus for peripheral functions https://www.renesas.com/document/tnn/notes-cs-smart-configurator-rx-e-studio-smart-configurator-plug	RX230, RX231	V1.4.0
Oct. 01, 2018	R20TS0351	1. Setting TPU0 channel of PWM Mode Timer https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx-0	RX65N, RX651, RX64M	V1.5.0
Feb.01, 2019	R20TS0401	1. Point for caution when using the GTIOcnm pin (n = 0 to 9, m = A, B) of the general PWM timer (GPTW) as a hardware source https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx-1	RX66T	V2.1.0
Apr.16, 2019	R20TS0425	1. When using the I2C bus interface in master mode https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx-2	RX110, RX111, RX113, RX130, RX230, RX231, RX23T, RX24T, RX24U, RX64M, RX651, RX65N, RX71M	V2.2.0
Jun.01, 2019	R20TS0434	1. When using self-diagnosis function of 12-bit A/D converter in Single Scan Mode 2. When using Serial Peripheral Interface clock synchronous mode in slave transmit 3. When using I2C Bus Interface with Fast-mode Plus enabled https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx-3	RX230, RX231, RX66T, RX72T, RX64M, RX651, RX65N, RX71M	V2.2.0

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Jun.16, 2019	R20TS0436	1. When using general PWM timer https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx-4	RX66T, RX72T	V2.2.0
Aug.01, 2019	R20TS0466	1. When using the NACK reception transfer suspension function on the I ² C bus interface https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx-5	RX110, RX111, RX113, RX130, RX230, RX231, RX23T, RX24T, RX24U, RX64M, RX651, RX65N, RX66T, RX71M, RX72M, RX72T	V2.3.0
Sep.16, 2019	R20TS0477	1. When Using the Automatic Adjustment Function for Time Error Adjustment on the Realtime Clock https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx-6	RX110, RX111, RX113, RX130, RX230, RX231, RX64M, RX651, RX65N	V2.4.0
Dec.16, 2019	R20TS0522	1. When using temperature sensor output or internal reference voltage for comparison function on S12AD components (Single Scan Mode, Group Scan Mode and Continuous Scan Mode) 2. When using calendar mode API to set counter value on RTC component 3. When using window B for comparison function on S12AD Continuous Scan Mode component 4. When using double trigger mode on S12AD Single Scan Mode component https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx-7	RX64M, RX651, RX65N, RX66T, RX71M, RX72M, RX72T	V2.4.0
Feb. 01, 2020	R20TS0546	1. When using the PLL frequency synthesizer of the clock https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx-8	RX64M, RX651, RX65N, RX66T, RX71M, RX72T	V2.5.0

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Mar. 16, 2020	R20TS0555	1. When using the TGIC7 and TGID7 interrupts in Normal Mode Timer or PWM Mode Timer 2. When creating a project with RX24T 64-pin FK packages 3. When using compare level of AN109 in Single Scan Mode S12AD https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx-9	RX24T, RX24U, RX71M	V2.5.0
Apr.03, 2020	TN-RX*-A0222	Errata to RX72N Group User's Manual: Hardware Rev.1.00 https://www.renesas.com/document/tcu/errata-rx72n-group-users-manual-hardware-rev100	RX72N	V2.5.0
May.16, 2020	R20TS0579	1. When using Stop API in Continuous Scan Mode DSAD and Single Scan Mode DSAD components https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx-10	RX23E-A	V2.6.0
Jun.16, 2020	R20TS0591	1. When using Data Transfer Controller (DTC) component and making configuration for its vector base address 2. When using SCI/SCIF Asynchronous Mode component and making configuration for its bit-rate 3. When using AN007 or AN107 as analog input pins in S12AD components https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx-11	RX230, RX231, RX651, RX65N, RX66T, RX72T	V2.6.0
Aug. 21, 2020	TN-RX*-A0234A/E	Errata to the RX113 Group User's Manual: Hardware Rev.1.10 https://www.renesas.com/document/tcu/errata-rx113-group-users-manual-hardware	RX113	V2.8.0
Sep. 01, 2020	R20TS0611	When using PWM Mode component and making configuration with MTU channel 1 and 2 https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plug-smart-configurator-rx-13	RX13T, RX23T, RX24T, RX24U	V2.7.0

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Sep. 24, 2020	TN-RX*-A0235B/E	Notes on the Transmit Data Empty Interrupt When the FIFO is in Use with the Serial Communications Interface (SCI) https://www.renesas.com/document/tcu/notes-transmit-data-empty-interrupt-when-fifo-use-serial-communications-interface-sci	RX651, RX65N, RX66N, RX66T, RX72M, RX72N, RX72T	V2.7.0
Oct. 01, 2020	R20TS0623	1. When using “r_sci_rx” component and making pin configurations for RXD and TXD 2. When using “r_sci_rx” component, duplicate SCI11 channels are displayed in the Components configuration panel https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plugin-smart-configurator-rx-12	RX651, RX65N, RX66N, RX72M, RX72N	V2.7.0
Dec. 01, 2020	R20TS0638	1. Note on setting timer operation period in Motor component. 2. When loading project with port configuration created in V2.5.0 or version before into V2.6.0 version onwards https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plugin-smart-configurator-rx-14	RX13T, RX23T, RX24T, RX24U, RX651, RX65N, RX66T, RX72T, RX72M	V2.8.0
Aug. 29, 2017	TN-RX*-A180A/E	Restriction for the PH7/XCIN Pin https://www.renesas.com/document/tcu/restriction-ph7xcin-pin	RX110, RX111, RX113	V2.9.1
May. 16, 2021	R20TS0696	When using PORT component and configuring PORTC multiplexed pins as input https://www.renesas.com/us/en/document/tnn/notes-e-studio-smart-configurator-plugin-smart-configurator-rx-15	RX130, RX230, RX231	V2.10.0
Aug. 01, 2021	R20TS0735	When using Port Output Enable (POE) component and configuring MTU pins as high impedance https://www.renesas.com/sq/zh/document/tnn/notes-e2-studio-smart-configurator-plugin-smart-configurator-rx	RX23W, RX24T, RX64M, RX651, RX71M, RX72M	V2.11.0

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Nov. 16, 2021	R20TS0770	When using Port component and configuring port pins' driving ability as high drive output https://www.renesas.com/us/en/document/tnn/notes-e-studio-smart-configurator-plugin-smart-configurator-rx-16	RX651, RX65N	V2.12.0
Mar. 01, 2022	R20TS0820	1. When importing existing C++ project and updating BSP component version to 7.00 onwards 2. When build or clean e ² studio Smart Configurator project 3. When using AN107 in S12AD Continuous Scan Mode component https://www.renesas.com/document/tnn/notes-e-studio-smart-configurator-plugin-smart-configurator-rx-17	RX110, RX111, RX113, RX130, RX13T, RX140, RX230, RX231, RX23E-A, RX23T, RX23W, RX24T, RX24U, RX651, RX65N, RX66N, RX66T, RX671, RX72M, RX72N, RX72T, RX64M, RX71M	V2.13.0

5. Points for Limitation

This section describes points for limitation regarding the Smart Configurator for RX V2.16.0. Regarding to FIT component driver limitation, please refer to its document generated out after code generation.

5.1 List of Limitation

Table 5-1 List of limitations (RX100, RX200 Family)

✓ : Applicable, -: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX13T	RX140	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
1	Note on general I/O port direction issue on MCU package view when using Port Component	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
2	Note on the resource tree in the FIT component GUI configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
3	Note on address pin when using external bus	-	-	-	-	-	-	✓	-	-	✓	-	
4	Note on "Out of range for memory type" build error when using Data Transfer Controller component on EWRX IAR tool chain	-	-	-	-	-	-	-	-	-	-	-	
5	Note on Overlaps build error when using Data Transfer Controller component on EWRX IAR tool chain	✓	✓	✓	-	✓	✓	✓	✓	-	✓	✓	
6	Note on generated code when using Port component	-	-	-	-	-	✓	-	-	-	-	-	

Table 5-2 List of Limitation (RX600, RX700 family)

✓ : Applicable, -: Not Applicable

No	Description	RX64M	RX65N, RX651	RX66N	RX66T	RX660	RX671	RX71M	RX72M	RX72N	RX72T	Remarks
1	Note on the general I/O port direction issue on MCU package view when using Port Component	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
2	Note on the resource tree in the FIT component GUI configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
3	Note on address pin when using external bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
4	Note on "Out of range for memory type" build error when using Data Transfer Controller component on EWRX IAR tool chain	-	-	✓	-	-	-	-	✓	✓	-	
5	Note on Overlaps build error when using Data Transfer Controller component on EWRX IAR tool chain	✓	✓	-	✓	-	✓	✓	-	-	✓	
6	Note on generated code when using Port component	-	-	-	-	✓	-	-	-	-	-	

5.2 Details of Limitation

5.2.1 Note on the general I/O port direction issue on MCU package view when using Port Component

When adding two configurations for Port component and set different direction for the same port pin in these two configurations, e.g. set P14 as output in 1st configuration while P14 as input in the 2nd configuration, after that remove the 2nd configuration, but now the P14 direction is marked as 'I' on the MCU package view for 1st configuration.

5.2.2 Note on the resource tree in the FIT component GUI configuration

When configuring the FIT component, the resource tree is still visible even there is no pins under it, for such case it will be hidden from next release.

Property	Value
# RX FIFO threshold for channel 9	8
# RX FIFO threshold for channel 10	8
# RX FIFO threshold for channel 11	8
# Received data match function for chann	Not
# Received data match function for chann	Not
# Received data match function for chann	Not
# Received data match function for chann	Not
# Received data match function for chann	Not
# Received data match function for chann	Not
# Received data match function for chann	Not
# Received data match function for chann	Not
# Received data match function for chann	Not
# Received data match function for chann	Not
# Received data match function for chann	Not
# Received data match function for chann	Not
# Received data match function for chann	Not
# Received data match function for chann	Not
Resources	
SCI	

Figure 5-1 Resource tree without any pin in FIT component GUI

5.2.3 Note on address bus when using external bus

When using Address/Data multiplexed bus in external bus, disable all unnecessary address output pin settings.

Address output pin setting

☐ A7-A0, BC0#, DQM2, DQM3

☐ A8 ☐ A9 ☐ A10 ☐ A11

☐ A12 ☐ A13 ☐ A14 ☐ A15

☐ A16 ☐ A17 ☐ A18 ☐ A19

☐ A20 ☐ A21 ☐ A22 ☒ A23

Settings for External Address Buses A0 to A7 :
Set PA0 to PA7.

Settings for External Address Buses A16 to A23 :
(Option 1) Set PC0 to PC7.
(Option 2) Set PC0, PC1, P71, P72, P74, and PC5 to PC7.
(Option 3) Set P90 to P97.

Figure 5-2 “Address output pin setting” value should be disabled

5.2.4 Note on “Out of range for memory type” build error when using Data Transfer Controller component on EWRX IAR tool chain

When using Data Transfer Controller component in Smart Configurator project that is using EWRX IAR tool chain, the following “Out of range for memory type” build error might occur.

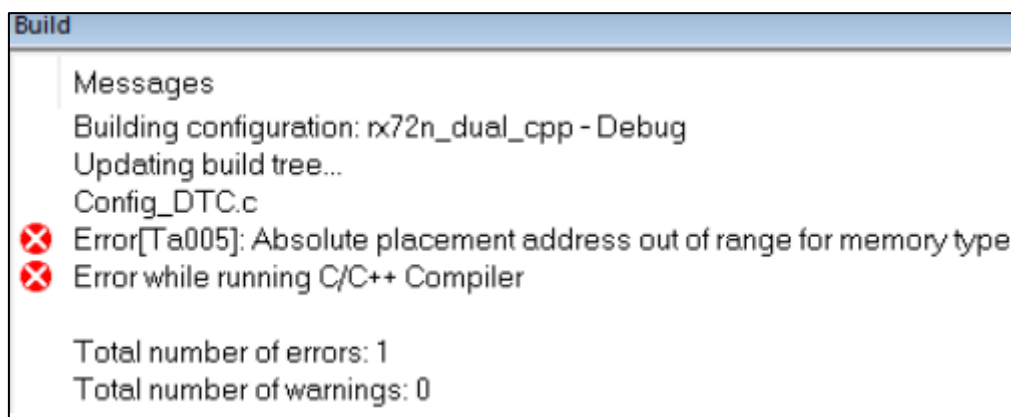


Figure 5-1 Build error when using Data Transfer Controller component

To resolve this build error, modify the variable type of `dtc_vector26` in “Config_DTC.c” as below.

- Variable type of “`dtc_vector26`” in “Config_DTC.c” before modifying

```

/*****
Global variables and functions
*****/
#pragma location = 0x0087FC68UL
__no_init volatile uint32_t dtc_vector26;
__no_init volatile st_dtc_data_t dtc_transferdata_vector26;
/* Start user code for global. Do not edit comment generated here */
/* End user code. Do not edit comment generated here */

```

- Manually update the variable type of "dtc_vector26" as below

```

/*****
Global variables and functions
*****/
#pragma location = 0x0087FC68UL
__no_init __data32 volatile uint32_t dtc_vector26;
__no_init volatile st_dtc_data_t dtc_transferdata_vector26;
/* Start user code for global. Do not edit comment generated here */
/* End user code. Do not edit comment generated here */

```

5.2.5 Note on Overlaps build error when using Data Transfer Controller component on EWRX IAR tool chain

When using Data Transfer Controller component in Smart Configurator project that is using EWRX IAR tool chain, the following Overlaps build error might occur.

```

✖ Error[Lp023]: absolute placement (in [0x3c6c-0x3fff]) overlaps with absolute section:
[0x3c6c-0x3c6f].data24.abs.noinit (Config_DTC.o #9) [dtc_vector27]

✖ Error[Lp011]: section placement failed
unable to complete "place at" directives with a total estimated minimum size of 0x1000 bytes in <[0x3c6c-0x3fff]> (total space 0x394).
✖ Error[Lp015]: section placement failure: overcommitted content in [0x3c6c-0x3fff]
✖ Error while running Linker

Total number of errors: 3
Total number of warnings: 0

Build failed.

```

Figure 5-2 Build error when using Data Transfer Controller component

To solve the build error, please reconfigure the value of DTC vector base address in Smart Configurator GUI into the value that is out of the range value mentioned inside the build error message and smaller than the default value of DTC vector base address in 1-Kbyte units.

- The following is an example on how to reconfigure the value of DTC vector base address of Data Transfer Controller component in RX671 device

- 1) Add Data Transfer Controller in Smart Configurator and generate code with default settings.
- 2) Import the project to IAR Workbench and build.
- 3) The following error is generated out when build the project in IAR Workbench.

```

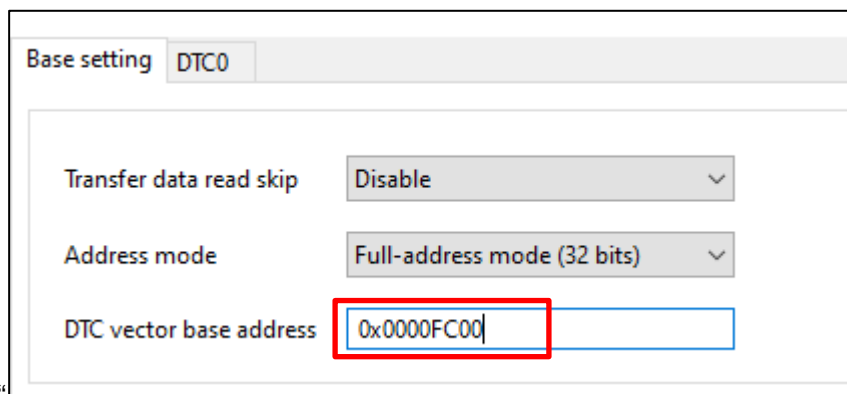
✖ Error[Lp023]: absolute placement (in [0x1'fc68-0x1'ffff]) overlaps with absolute section:
[0x1'fc68-0x1'fc6b].data24.abs.noinit (Config_DTC.o #9) [dtc_vector26]

✖ Error[Lp011]: section placement failed
unable to complete "place at" directives with a total estimated minimum size of 0x1000 bytes in <[0x1'fc68-0x1'ffff]> (total space 0x398).
✖ Error[Lp015]: section placement failure: overcommitted content in [0x1'fc68-0x1'ffff]
✖ Error while running Linker

```

- 4) From the error message, the invalid range [0x1'fc68-0x1'ffff] will be shown at the console. Moreover, the valid input value of DTC vector base address must also be smaller than the default value.

- 5) Configure the value of DTC vector base address into "0x0000FC00"



Base setting DTC0

Transfer data read skip Disable

Address mode Full-address mode (32 bits)

DTC vector base address 0x0000FC00

- 6) Generate code and rebuild the project in IAR Workbench.
- 7) Build error has been resolved.

```
Messages
r_bsp_cpu.c
r_bsp_interrupts.c
r_bsp_mcu_startup.c
r_cg_hardware_setup.c
r_bsp_software_interrupt.c
r_rx_intrinsic_functions.c
r_smc_cgc.c
r_smc_cgc_user.c
r_smc_interrupt.c
resetprg.c
vecttbl.c
Linking

Total number of errors: 0
Total number of warnings: 0
```

5.2.6 Note on generated code when using Port component

When using PORT component in the following device and pin packages, the default value of the PDR register that mentioned in the table below are not generated as expected. This issue will be fixed from the next release.

Table 5-3 List of the generated PDR default value in PORT component

Device	Pin package	Port number	Current PDR default value	Expected PDR default value
RX140	80 pin	PORTJ	0x3E or _3E_PORTJ_DEFAULT	0x3D or _3D_PORTJ_DEFAULT
	48 pin	PORTE	0xF0 or _F0_PORTE_DEFAULT	0xE1 or _E1_PORTE_DEFAULT
	32 pin	PORTE	0xF0 or _F0_PORTE_DEFAULT	0xE1 or _E1_PORTE_DEFAULT
RX660	80 pin	PORT3	0x04 or _04_PORT3_DEFAULT	0x08 or _08_PORT3_DEFAULT
		PORT5	0xC0 or _C0_PORT5_DEFAULT	0xCF or _CF_PORT5_DEFAULT

As a temporary workaround, please follow the below steps to resolve this issue

Here using PORTJ in RX140_80 pin device as example.

- After making PORTJ GUI setting and generate codes, please open the “R_Config_Port.c” file and find the PORTJ PDR initialization line of code in “R_Config_Port_Create(void)” API.

```
void R_Config_PORT_Create(void)
{
    /* Set PORTJ registers */
    PORTJ.PCR.BYTE = _00_Pm1_PULLUP_OFF | _00_Pm6_PULLUP_OFF |
    _00_Pm7_PULLUP_OFF;
    PORTJ.PMR.BYTE = _00_Pm1_PIN_GPIO | _00_Pm6_PIN_GPIO | _00_Pm7_PIN_GPIO;
    PORTJ.PDR.BYTE = _00_Pm1_MODE_INPUT | _00_Pm6_MODE_INPUT |
    _00_Pm7_MODE_INPUT | _3E_PDRJ_DEFAULT;

    R_Config_PORT_Create_UserInit();
}
```

- Copy the above line of code and paste into the “R_Config_PORT_Create_UserInit(void)” API inside the “R_Config_PORT_user.c” file.

```
void R_Config_PORT_Create_UserInit(void)
{
    /* Start user code for user init. Do not edit comment generated here */
    PORTJ.PDR.BYTE = _00_Pm1_MODE_INPUT | _00_Pm6_MODE_INPUT |
    _00_Pm7_MODE_INPUT | 3E_PDRJ_DEFAULT;
    /* End user code. Do not edit comment generated here */
}
```


- Replace the wrong default value for PORTJ PDR register with the expected value “_3D_PDRJ_DEFAULT” described in above Table 5-3 and save.

```
void R_Config_PORT_Create_UserInit(void)
{
    /* Start user code for user init. Do not edit comment generated here */
    PORTJ.PDR.BYTE = _00_Pm1_MODE_INPUT | _00_Pm6_MODE_INPUT |
    _00_Pm7_MODE_INPUT | _3D_PDRJ_DEFAULT;
    /* End user code. Do not edit comment generated here */
}
```

6. Points for Caution

This section describes points for caution regarding the Smart Configurator for RX V2.16.0. Regarding to FIT component driver caution, please refer to its document generated out after code generation.

6.1 List of Caution

Table 6-1 List of Caution (RX100, RX200 Family)

✓ : Applicable, -: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX13T	RX140	RX230, RX231	RX23E-A	RX23T	RX23W	RX24T, RX24U	Remarks
1	Note on configuring GPT interrupt	-	-	-	-	-	-	-	-	-	-	✓	
2	Note on using only reception in SCI Clock Synchronous Mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
3	Notes on using high transfer speed in SCIF Synchronous Mode	-	-	-	-	-	-	-	-	-	-	-	
4	Note on device change functionality	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
5	Note on using Smart Configurator for GCC project in e ² studio 7.4.0	✓	✓	✓	✓	✓	-	✓	✓	✓	-	✓	
6	Note on using Data Transfer Controller	-	-	-	-	✓	✓	-	✓	-	-	-	
7	Note on Ports setting when using S12AD components	✓	-	✓	✓	-	✓	-	-	-	✓	-	
8	Note on section build warning when using FIT components	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
9	Note on C++ project support in CS+	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
10	Note on Installation directory	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
11	Note on the build error of RTOS C++ project	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
12	Note on the output of high impedance issue for TXDn pin	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
13	Note on the include path update issue when renaming the component's configuration name	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
14	Note on the "Show view" dialog in Standalone Smart Configurator	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
15	Note on accessing "Release Notes" and "Tool News" URL from the help menu	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
16	Note on the IPCF file naming change for IAR project	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
17	Note on using user code protection feature	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	

Table 6-2 List of Caution (RX600, RX700 Family)

✓: Applicable, -: Not Applicable

No	Description	RX64M	RX65N, RX651	RX66N	RX66T	RX660	RX671	RX71M	RX72M	RX72N	RX72T	Remarks
1	Note on configuring GPT interrupt	✓	-	✓	✓	-	-	✓	✓	✓	✓	
2	Note on using only reception in SCI Clock Synchronous Mode	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
3	Notes on using high transfer speed in SCIF Synchronous Mode	✓	-	-	-	-	-	✓	-	-	-	
4	Note on device change functionality	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
5	Note on using Smart Configurator for GCC project in e ² studio 7.4.0	✓	✓	✓	✓	-	-	✓	-	✓	✓	
6	Note on using Data Transfer Controller	-	✓	✓	-	✓	✓	-	✓	✓	-	
7	Note on Ports setting when using S12AD components	✓	✓	✓	-	-	✓	✓	✓	✓	-	
8	Note on section build warning when using FIT components	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
9	Note on C++ project support in CS+	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
10	Note on Installation directory	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
11	Note on the build error of existing RTOS C++ project	✓	✓	✓	✓	-	✓	✓	✓	✓	✓	
12	Note on the output of high impedance issue for TXDn pin	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
13	Note on the include path update issue when renaming the component's configuration name	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
14	Note on the "Show view" dialog in Standalone Smart Configurator	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
15	Note on accessing "Release Notes" and "Tool News" URL from the help menu	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
16	Note on the IPCF file naming change for IAR project	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
17	Note on using user code protection feature	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	

6.2 Details of Caution

6.2.1 Note on configuring GPT interrupts

The GPT interrupts are not specified as the Software Configurable Interrupt in the initial state even after the GPT interrupts are configured by GPT component. To specify GPT interrupts as Software Configurable Interrupt source, release unused Software Configurable interrupt source on the Interrupt sheet and allocate GPT interrupts instead.

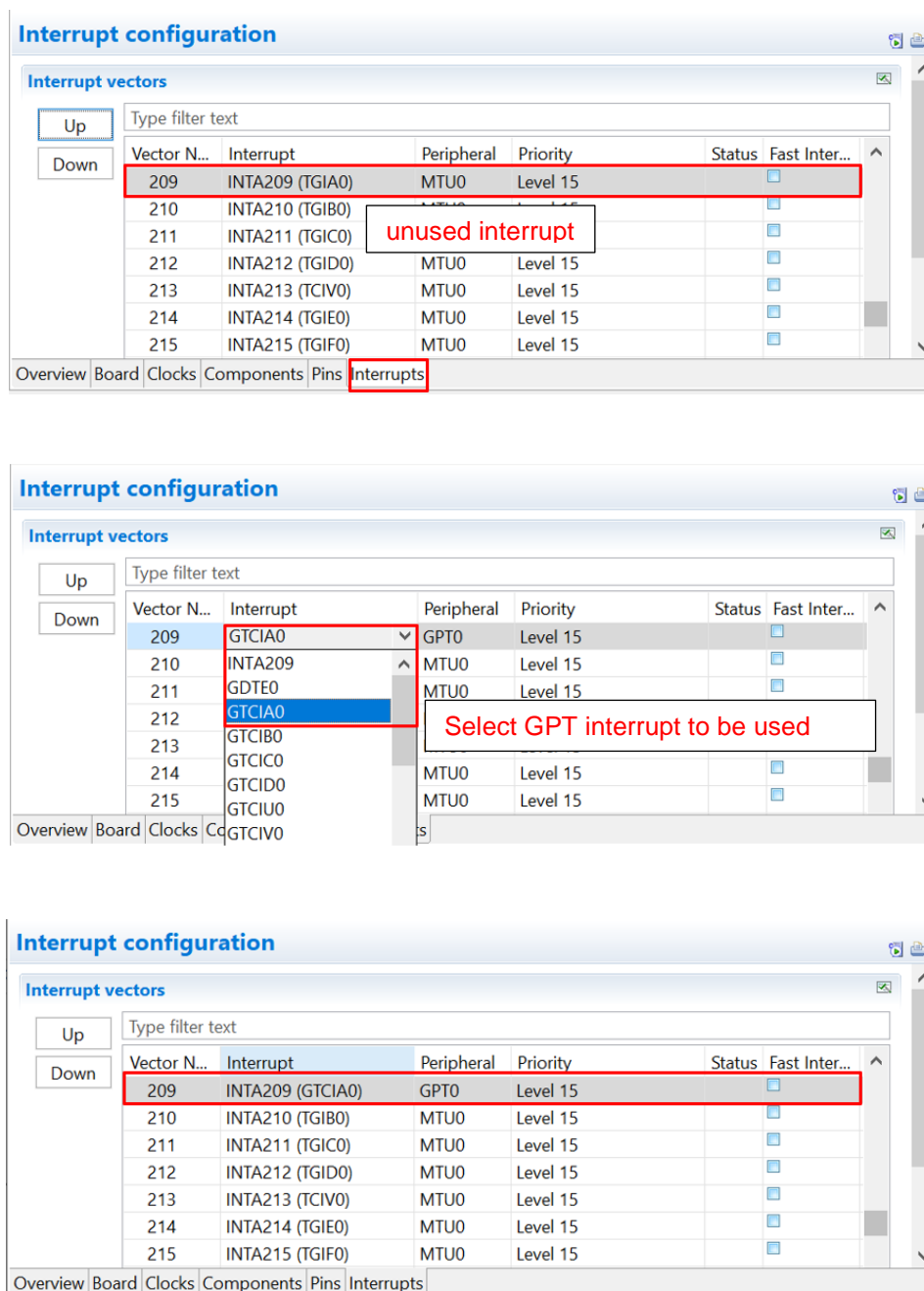


Figure 6-1 GPT interrupt vector number assignment

6.2.2 Note on using only reception in SCI Clock Synchronous Mode

In SCI Clock Synchronous Mode using internal clock, if only reception is enabled in high communication speed, extra clocks are generated even though reception has been completed.

This is due to the delay in disabling RE to stop the clock after the desired number of data is received.

To prevent this issue, select Transmission/Reception work mode when using Smart Configurator. Use "R_<Configuration Name>_Serial_Send_Receive" function instead of "R_<Configuration Name>_Serial_Receive". The same number of data for tx_num and rx_num should be specified.

Disable TXDn pin in Smart Configurator Pins page and send dummy data if transmission is not required.

There will be warnings when TXDn pin is disabled. These warnings can be ignored as TXDn pin is not intended to be used originally.

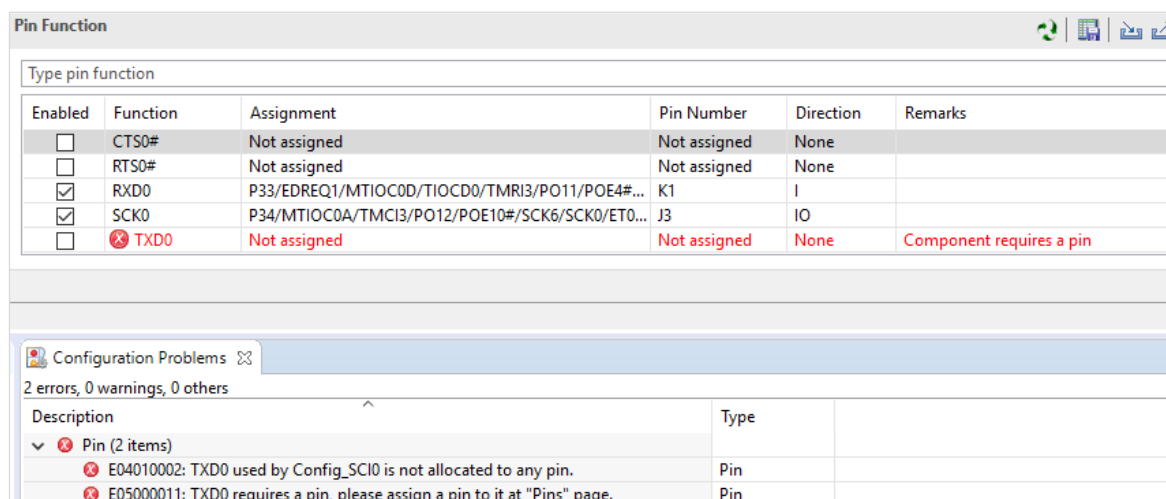


Figure 6-1-2 Ignore warnings when TXDn pin is disabled (Example with TXD0)

6.2.3 Note on using high transfer speed in SCIF Synchronous Mode

If the number of reception data specified for the API (R_<Configuration Name>_Serial_Receive or R_<Configuration Name>_Serial_Send_Receive) and reception FIFO threshold specified on GUI do not satisfy the formula below:

$$(\text{Reception Data Size}) = n * (\text{Reception FIFO threshold}) \quad (n=1,2,3,\dots)$$

extra clock generation may occur after the desired number of data is received in high communication speed when using internal clock.

To prevent this issue, specify the reception data size and reception FIFO threshold that satisfy the formula.

6.2.4 Note on device change functionality

Save project settings before performing change device operation. After change device, perform these operations:

1. Visual check on Components window and Configuration Problems window. Resolve errors and conflicts if there is any.
2. Check each component and convert settings.
3. Re-generate codes.

6.2.5 Note on using Smart Configurator for GCC project in e2 studio 7.4.0

When using default options to create new "GCC for Renesas RX Executable Project" with Smart Configurator in e2 studio 7.4.0, build error occurs.

```
C:\example\src\smc_gen\r_bsp\mcu/all/r_bsp_common.h:55:24:
fatal error: stdbool.h: No such file or directory
```

As workaround, use e2 studio 7.5.0 to create new "GCC for Renesas RX Executable Project" with Smart Configurator.

6.2.6 Note on using Data Transfer Controller

Smart Configurator does not support sequence transfer, write-back skip, write-skip disable and displacement addition features.

6.2.7 Note on Ports setting when using S12AD components

Some pins cannot be configured as output pins when S12AD components (Single Scan Mode, Continuous Scan Mode and Group Scan Mode) are used. For more information, refer to User's Manual: Hardware of the affected groups, "12-Bit A/D Converter" chapter, "Pin Setting When Using the 12-bit A/D Converter" usage note. From SC for RX 2.4.0, this note has been highlighted on the top GUI of S12AD components.

Device groups	Port pins
RX110, RX113	P40 to P44, P46
RX113	P40 to P44, P46 P90 to P92
RX130, RX140, RX23W	P40 to P47
RX64M, RX651, RX65N, RX66N, RX71M, RX72M, RX72N	P00 to P02, P03, P05, P07 P40 to P47 P90 to P93 PD0 to PD7 PE0 to PE7
RX671	P00 to P02, P03, P05, P07 P40 to P47 P90 PD0 to PD7 PE0, PE1

6.2.8 Note on section build warning when using FIT components

When using FIT components (e.g. r_ether_rx) with section settings, these section settings will be added automatically into IDE C/C++ builder setting, but these section settings will not automatically removed from the C/C++ builder setting when these FIT components are deleted from SC, thus there are build warnings for not finding section declaration when execute build operation after these FIT components are removed, please ignore these build warnings.

6.2.9 Note on C++ project support in CS+

When using Smart Configurator for C++ project application in CS+, please be noted to manually prepare the following content in the main.cpp generated out by these IDEs to make it work properly with Smart Configurator source codes.

- CS+: please manually add the following highlighted one line of code into main.cpp

```
#ifdef __cplusplus
// #include <ios> // Remove the comment when you use ios
// _SINT ios_base::Init::init_cnt; // Remove the comment when you use ios
#endif

void main(void);
#ifdef __cplusplus
extern "C" {
#include "r_smc_entry.h"
void abort(void);
}
#endif

void main(void)
{
}

#ifdef __cplusplus
void abort(void)
{
}
#endif
```

6.2.10 Note on Installation directory

When installing Smart Configurator, you may get an error message "The specified path is too long" if the installation file path is longer than the maximum length permitted by Windows. The suggested way is to re-install the CS+ into its default path (C:\Program Files (x86)\Renesas Electronics\) or a folder whose paths' length is less than 65 characters, then install Smart Configurator again.

6.2.11 Note on the build error of existing RTOS C++ project

When building existing RTOS C++ CCRX project (FreeRTOS & Azure RTOS) in e² studio, there will be a build error saying "E0562310: Undefined external symbol "_abort" referenced in "error"" in the output console, these existing projects were created by Smart Configurator for RX V2.12.0 and before version while BSP version was updated to V7.00. To resolve this build error, please add the "abort" function manually into main program file.

e.g. Add the "abort" function for FreeRTOS C++ CCRX project

```
#include "FreeRTOS.h"
#include "task.h"

void main_task(void *pvParameters)
{
    /* Create all other application tasks here */

    while(1);

    vTaskDelete(NULL);
}

void abort (void)
{
}
```

6.2.12 Note on the output of high impedance issue for TXDn pin

When using the serial components, the SCR.TE bit is set to 1 after changing the pin function to TXDn which will cause the output of TXDn pin becomes high impedance. To fix this issue, SCI/SCIF Asynchronous Mode component has followed the UM suggestion (set the TE bit to 1 before changing the pin function to "TXDn". Change the pin function to "general-purpose I/O port, output" before setting the TE bit to 0) and updated the generated codes from Smart Configurator for RX V2.14.0. For the other serial components as below, the generated codes are not updated to follow the UM suggestion because the high impedance time is quite short, there is no impact to these modes' communications.

- SCI/SCIF Clock Synchronous Mode
- Smart Card Interface Mode
- SPI Clock Synchronous Mode (SCI channels)

6.2.13 Note on the include path update issue when renaming the component's configuration name

When renaming the added component's configuration in e² studio Smart Configurator project that has self-defined include path setting for any folder or file, include path setting for that folder or file will keep the old name setting after code generation. This will cause build error when compiling the newly generated codes so please manually update the include path.

The folder or file which has self-defined include path setting can be recognized by checking the overlay icon (📁) on that folder or file. Below is an example on how to handle the include path update after renaming Compare Match Timer component configuration.

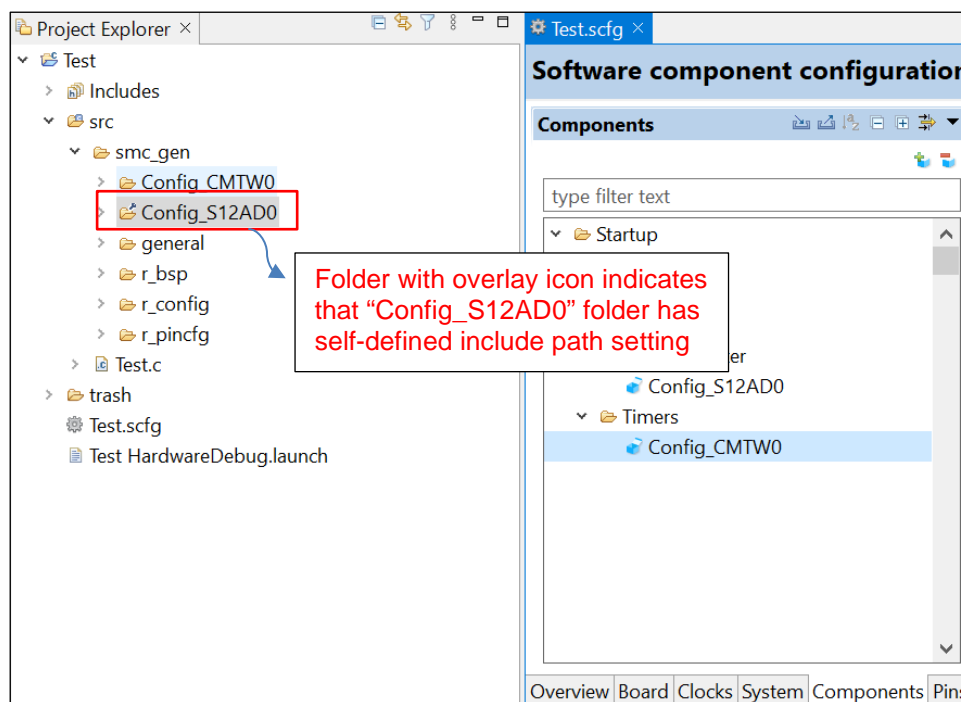


Figure 6-3 Compare Match Timer component configuration before renaming

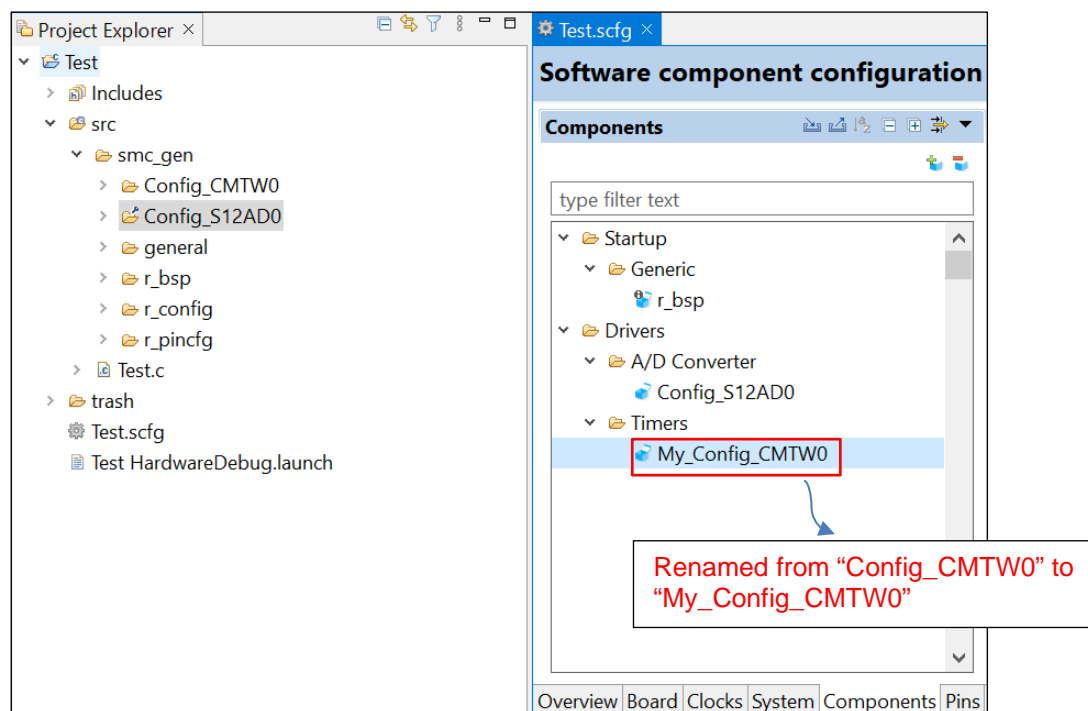


Figure 6-4 The Compare Match Timer component configuration after renaming

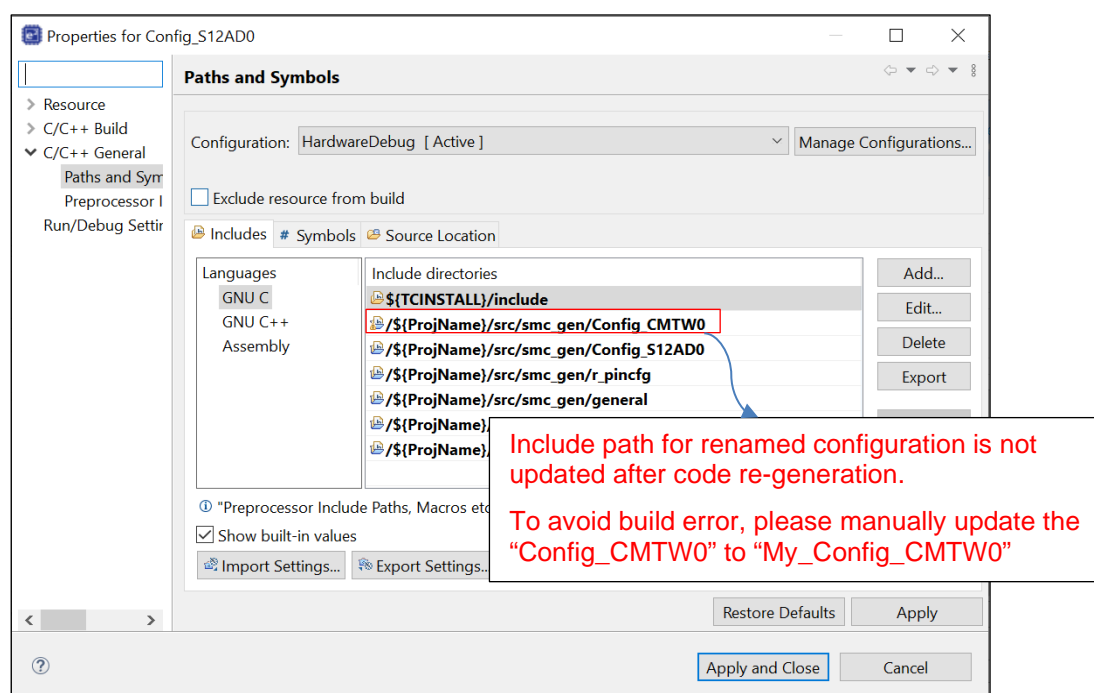


Figure 6-5 Include path setting for the "Config_S12AD0" configuration

6.2.14 Note on the “Show view” dialog in Standalone Smart Configurator

When configuring the "Show View" dialog in Standalone Smart Configurator, although the following items will be shown inside the menu, but do not configure or use it. This issue will be fixed from the next release.

- Bookmarks
- Markers
- Navigator (Deprecated)
- Problems
- Progress
- Tasks
- Welcome
- Cheat Sheets

6.2.15 Note on accessing “Release Notes” and “Tool News” URL from the help menu

For Smart Configurator for RX V2.15.0 or before version, “Release Notes” and “Tools News” in the help menu cannot access the correct URL. This issue has been fixed from this version.

Please access the URL below directly for Smart Configurator for RX V2.15.0 or before version.

Release Notes: <https://www.renesas.com/rx-smart-configurator-release-note>

Tool News: <https://www.renesas.com/rx-smart-configurator-tn-notes>

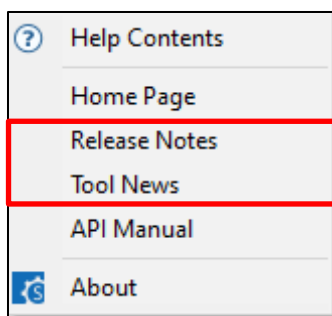


Figure 6-2 "Release Notes" and "Tool News" in help menu

6.2.16 Note on the IPCF file naming change for IAR project

From Smart Configurator for RX V2.15.0 onwards, IPCF file name has been updated from “projectname.ipcf” to “buildinfo.ipcf”, thus for existing IAR project which is using “projectname.ipcf”, please register the new IPCF file “buildinfo.ipcf” file into IAR EWRX workbench via the “Add project connection” menu to restore the connection between Smart Configurator and IAR EWRX workbench, otherwise there is no update for the generated files in the IAR EWRX workbench when changing GUI setting in Smart Configurator and then generating codes.

6.2.17 Note on using user code protection feature

From Smart Configurator for RX V2.16.0 onwards, user code protection feature will be supported for all Code Generation components. Please use the following specific tags to add user code when using the user code protection feature. If the specific tags do not match exactly, inserted user code will not be protected after the code generation.

```
/* Start user code */
```

User code can be added between the specific tags

```
/* End user code */
```

The user code protection feature will only be supported on the files that are generated by the Code Generation component. Hence, the user code protection feature is not available for non-Code Generation components.

Revision History

Rev.	Section	Description
1.00	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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