RL78/G16 Simulator V1.00.00

Release Note

Thank you for using the RL78/G16 simulator.

This document describes restrictions on and points for caution regarding the simulator.

Read this document before using the product.

Contents

Chapter 1. Target Devices and Supported Simulation Functions

The RL78/G16 simulator supports the following target devices.

Device group	Device name
RL78/G16	10 pins R5F1211A, R5F1211C 16 pins R5F1214A, R5F1214C 20 pins R5F1216A, R5F1216C 24 pins R5F1217A, R5F1217C 32 pins R5F121BA, R5F121BC

As well as CPU instructions, the RL78/G16 simulator is capable of simulating the following items in the target devices.

- Peripheral modules such as timers, the serial array unit, and the serial interface
- Virtual target board (simulation via the [I/O panel] window)
- MCU pin signal waveforms (simulation via the [Timing chart] window)

Note that the RL78/G16 simulator does not support simulation of current drawn by this MCU.

Chapter 2. Points for Caution

This section lists points for caution on using the RL78/G16 simulator. These points for caution are in the following two categories.

• Differences in behavior between the target devices and the simulator due to simulator specifications

• Usage of simulation functions (operations in and configuration of the GUI windows)

CS+ for CC supports the [Virtual Board] panel which is described in those points for caution.

2.1 Differences in behavior between the target devices and the simulator

2.1.1 Peripheral functions not supported by the simulator

The simulator is not capable of simulating the following peripheral functions of the target devices.

- Selectable power-on-reset circuit
- Flash self-programming
- Capacitive touch sensing unit (CTSUb)
- CSI slave communication mode of the serial array unit

2.1.2 Peripheral I/O redirection registers 0 to 6 (PIOR0 to PIOR6)

The peripheral I/O redirection registers 0 to 6 (PIOR0 to PIOR6) can be manipulated by a program or debugger operations to re-assign specific multiplexed pin functions to alternative port pins in the same way as on the actual device.

Note, however, that the assignment of serial interface functions to port pins must not be changed since doing so will disable normal connections through the [Serial] window or the serial communication component of the [Virtual Board] panel.

After re-assigning a given pin function by using PIOR0 to PIOR6, be sure to select the name of the port pin you are currently using in the [Select Pin] dialog box of the simulator GUI or “Connected To” of the component in the [Virtual Board] panel. Note that when a multiplexed function is assigned to a port pin by using PIOR0 to PIOR6, the name of the multiplexed pin function is not displayed as the pin name by the simulator.

2.1.3 Special function registers (SFRs) for controlling port functions

The following SFRs which control port functions are not simulated.

Although read/write access for each register can proceed normally, the operation does not change even though the value is changed.

- Touch pin function select registers 0 and 1 (TSSEL0 and TSSEL1)
- TSCAP pin setting register (VTSEL)

2.1.4 Oscillation stabilization time for the clock generator

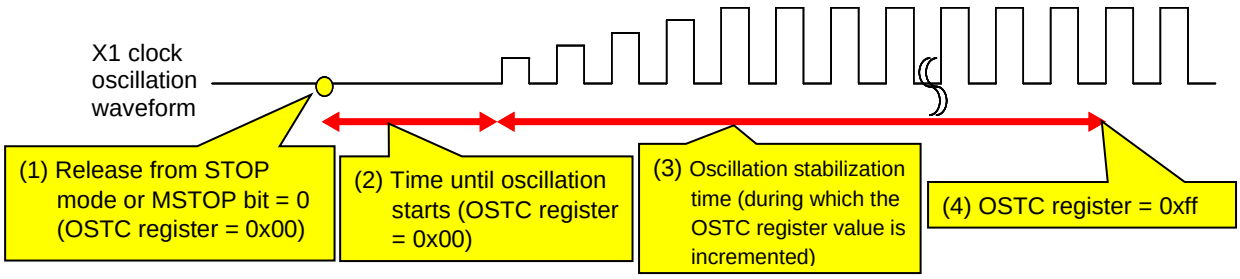
Since the simulator does not simulate the clock oscillator oscillation stabilization time, stabilization always takes no time. When the oscillation is started, the OSTC register is set to one of the following values (i.e. not incremented).

OSTS Setting	OSTC Value
0x0 : $(2^8+16)/fx$	0x80
0x1 : $(2^9+16)/fx$	0xc0
0x2 : $(2^{10}+16)/fx$	0xe0
0x3 : $(2^{11}+16)/fx$	0xf0
0x4 : $(2^{13}+16)/fx$	0xf8
0x5 : $(2^{15}+16)/fx$	0xfc
0x6 : $(2^{17}+16)/fx$	0xfe
0x7 : $(2^{18}+16)/fx$	0xff

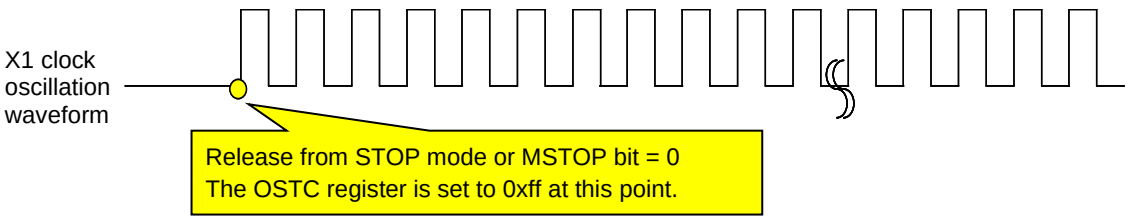
The following figure illustrates this operation.

In the target device, oscillation by the X1 clock starts after operation has passed through states (1) to (4). In the simulator, states (1) through (4) are skipped and oscillation instantly starts.

[Target device (an example of when OSTS is set to 0x07)]



[Simulator (an example of when OSTS is set to 0x07)]



Therefore, pay attention to the code that waits for oscillation stabilization.

There is no problem if a program is created under the condition that execution proceeds after the oscillation stabilization wait period when the OSTC register value becomes the maximum value, or when the OSTC register value exceeds the specified value, but if a program is created under the condition that execution proceeds after the oscillation stabilization wait period when the OSTC register value becomes a value other than the maximum value, execution will enter an endless loop.

The following shows examples of code that causes and does not cause problems.

The examples are when the OSTS is set to 0x07.

Correct code example (1)

```
while(OSTC != 0xff)
{
NOP();/* wait */
}
```

Correct code example (2)

```
while(OSTC <= 0xf0)
{
NOP();/* wait */
}
```

Example of code that may cause problems

```
while(OSTC != 0xf0)
{
NOP();/* wait */
}
```

2.1.5 SFRs (CMC, HIOTRM, and CSC) in the clock generator

The following SFRs which belong to the clock generator are not simulated. Although read/write access for each register can proceed normally, the operation does not change even if the value is changed.

- Bits 0, 1, and 2 (AMPH, AMPHS0, and AMPHS1) of the clock operating mode control register (CMC)
- High-speed on-chip oscillator trimming register (HIOTRM)

The operation in initialization of the EXCLKS, OSCSELS, XTSEL, AMPHS1, and AMPHS0 bits of the clock operation mode control register (CMC) and the XTSTOP bit of the clock operation status control register (CSC) differs between the target device and the simulator.

[Target device]

EXCLKS, OSCSELS, XTSEL, AMPHS1, AMPHS0, and XTSTOP bits are only initialized by an internal reset by data retention power supply voltage and retain their values following resetting by other reset sources.

[Simulator]

The bits are initialized by the following reset sources.

- External reset input via the RESET pin
- Internal reset due to detection of a program malfunction by the watchdog timer

2.1.6 Operating clock of the timer array unit

Do not specify an operating clock that runs at or below 233 Hz. If the operating clock for the timer array unit runs at or below 233 Hz, then the timer array unit will not work properly (it will behave as if operating with a clock that is faster than the one selected).

2.1.7 Noise filter of the timer array unit

Although the target device's timer array unit has a function to turn the noise filters on and off in order to reduce noise from the timer input pins, the simulator does not simulate this function since there is no noise in the simulator's signals. That is, whether filtering is on or off makes no difference to the behavior.

2.1.8 SFRs (RTCC0, RTCC1, and SUBCUD) of real-time clock 2 (RTC2)

The clock error correction register (SUBCUD) is not simulated. Although read/write access for the register can proceed normally, the operation does not change even if the value is changed.

The operation of real-time clock control register 0 (RTCC0), real-time clock control register 1 (RTCC1), and the clock error correction register (SUBCUD) of real-time clock 2 (RTC2) differs between the target device and the simulator.

[Target device]

RTCC0 and RTCC1 are cleared to 00H and SUBCUD is set to 0020H in response to an internal reset generated by the data retention power supply voltage of the internal reset circuit.

[Simulator]

RTCC0 and RTCC1 are cleared to 00H and SUBCUD is set to 0020H in response to resetting by the following reset sources.

- External reset input via the RESET pin
- Internal reset due to detection of a program malfunction by the watchdog timer

2.1.9 Clock output/buzzer output controller

When f_{MAIN} is selected as an output clock, the [Timing chart] window does not show the clock waveform of the PCLBUZ0 signal.

When $f_{MAIN}/2$ or a slower signal is selected as an output clock, the [Timing chart] window shows the clock waveform.

2.1.10 Interval interrupts generated by the watchdog timer

The timing of the generation of interval interrupts by the watchdog timer differs between the target device and the simulator.

[Target device]

When 75% + 3/(4xf_{IL}) of overflow time is reached

[Simulator]

When 75% of overflow time is reached

2.1.11 A/D converter

When no voltage is being applied to VDD, the default reference voltage of the A/D converter is 5.0 V.

To change the reference voltage, input the desired voltage values for VDD via the [Signal Data Editor] window.

The temperature sensor output voltage is always 1.05 V. Note that the simulator does not support the TSCAP voltage of the CTSU and the voltage is always 0 V.

2.1.12 Digital filters in the comparators (CMP)

The simulator does not simulate the digital filters in the comparators (CMP).

2.1.13 Response time of the comparators

Since the simulator does not simulate the response time of the comparators, the response time is always 0 second. This does not change even if the speed of the comparators is changed in the comparator output control register (COMPOCR).

2.1.14 Clock used in the serial array unit

Do not specify a clock that is 233 Hz or lower in the following cases. If the following clock of the serial array unit is 233 Hz or lower, then the serial array unit will not operate correctly (it will behave as if operating via a clock that is faster than the one selected).

- Operating clock (f_{MCK}) is 233 Hz or lower.
- Transfer clock setting by dividing the operation clock (f_{MCK} ÷ (SDRmn[15:9] + 1)) is 233 Hz or lower.

2.1.15 Noise filter of the serial array unit

Although the target device's serial array unit has a function to turn the noise filter on and off in order to reduce noise on the input pin, the simulator does not simulate this function since there is no noise in the simulator's signals. That is, whether filtering is on or off makes no difference to the behavior.

2.1.16 SDRmn registers of the serial array unit

The values read from the seven higher-order bits of the serial data registers (SDRmn) during serial operation differ between the target device and the simulator.

[Target device]

0 is read.

[Simulator]

The value read is that at the time serial operation starts.

2.1.17 SSm registers of the serial array unit

During serial communications, when the operation start trigger of channel n (SSmn) in the serial channel start register m (SSm) is set to 1, operation of the simulator differs from that of the actual target device in the way stated below.

[Target device]

The target device stops communications and enters the suspended state.

[Simulator]

The simulator does not stop communications. Accordingly, the TSFmn and BFFmn bits in the serial status register mn (SSRmn) are not cleared to 0.

2.1.18 IICA serial interface

IICA supports pin waveform generation and the communications through the [Serial] window. The following functions are not supported.

- Digital filter
- Arbitration
- Detection of transmission errors
- Communication reservation

2.1.19 SFR (IICCTL01) for the IICA serial interface

The following SFR which controls the IICA serial interface is not simulated.

Although read/write access for the register can proceed normally, the operation does not change even if the value is changed.

- Bit 2 (DFC0) [Note] and bit 3 (SMC0) of the IICA control register 01 (IICCTL01)

Note: In the simulator, the DFC0 bit can be set to 1 only when the SMC0 bit is 1.

2.1.20 Reset

Among the sources for generating reset signals, the following types of internal reset do not occur in the simulator.

- Internal reset by comparison of supply voltage and detection voltage of selectable power-on-reset (SPOR) circuit
- Internal reset by execution of illegal instruction
- Internal reset by data retention power supply voltage
- Internal reset by illegal-memory access
- Internal reset by the RAM parity error

In addition, the behavior differs as follows if a reset signal is input from the RESET pin.

[Target device]

The MCU is reset when the RESET pin goes low. Release from the reset state proceeds when the RESET pin goes high.

[Simulator]

The MCU is not reset when the RESET pin goes low. The simulator is reset momentarily and then released when the RESET pin goes high.

2.1.21 Reset control flag register (RESF)

The simulator only supports the WDTRF bit of the reset control flag register (RESF).

The simulator is not capable of simulating the operations of the other bits (TRAP, RPERF, IAWRF, and SPORF). Only the default values of these bits are indicated.

The reset control flag register (RESF) of the target device is cleared by an external reset input via the RESET pin, a reset by the data retention lower limit voltage, or reading the RESF register by using an 8-bit

memory manipulation instruction. However, on the simulator, the RESF is only cleared by an external reset input via the RESET pin.

2.1.22 SFR (PORSR) for the reset function

The simulator does not simulate the internal reset status register by data retention power supply voltage (PORSR). Although read/write access for the register can proceed normally, the operation does not change even if the value is changed.

2.1.23 Safety functions

The simulator does not support the following safety functions.

- Flash memory CRC operation function (general-purpose CRC)
- RAM parity error detection
- RAM guard function
- SFR guard function
- Invalid memory access detection

2.1.24 Executing illegal instructions

If an illegal instruction (instruction code: 0xFF) is executed, the target device will be reset, but the simulator will go into an endless loop (the illegal instruction will be executed repeatedly).

2.2 Usage of simulation functions

2.2.1 Simulation speed

The simulation speed of RL78/G16 simulator depends on the number of operating peripheral functions.

If many peripheral functions are operating, the simulation speed becomes from several to ten times slower than the actual device. Note

With the use of only a few, or even no peripheral functions, the simulation speed may become faster than the actual device.

Note: The measurement environment for simulation speed is as follows.

CPU: 3.20 GHz (Quad-Core); memory: 8 Gbytes; OS: Windows10 64-bit edition

2.2.2 Pin waveforms in the [Timing chart] window

The maximum length of a pin waveform is 4096 signal-level changing points. After reaching this maximum length, the data will be overwritten from the oldest value. If this length is not sufficient, use the following methods.

- Reduce the number of registered pins
- Stop the user program at the place where you want to confirm the waveform by using a breakpoint

2.2.3 Controlling windows

The following keyboard operations are not available in the simulator windows ([Signal Data Editor], [I/O panel], and [Serial]).

- Navigation via tab or arrow keys (←, ↑, →, ↓)
- Deletion via the Del or Backspace keys
- Cut & paste and other operations via the Ctrl + C, V, X, A, or Z keys.

Perform the above operations as follows.

- Navigation: Navigate by using the mouse.
- Deletion: Right-click and perform the action from the context menu.
- Cut & paste, etc.: Right-click and perform the action from the context menu.

2.2.4 Closing the [Simulator GUI] window

The [Simulator GUI] window can only be closed by disconnecting from the debugging tool, or by closing CS+ in proper manner. The [X] button cannot be used.

Additionally, although it appears that the [X] button can be pressed if Aero is enabled in Windows, pressing this button will not close the [Simulator GUI] window.

2.2.5 Disconnecting the debug tool

CS+ may be closed if the debugging tool is disconnected while any of the following dialog boxes is open from the [Simulator GUI] window. Be sure that the following dialog boxes have been closed before disconnecting the simulator.

- Save As
- Open
- New
- Color
- Font
- Customize
- Loop
- Select Pin
- Search Data
- Format (UART)
- Format (CSI)
- Format (IIC)
- Message (e.g. Error)
- Parts Button Properties
- Analog Button Properties
- Parts Key Properties
- Parts Level Gauge Properties
- Parts Led Properties
- Parts Segment LED Properties
- Parts Matrix Led Properties
- Parts Buzzer Properties
- Pull up / Pull down
- Entry Bitmap
- Object Properties

2.2.6 [Serial] window

When using the [Serial] window as the data receiver for the simplified I^2C of the serial array unit or IICA, only ACK can be generated after receiving the data. NACK cannot be generated.

Revision History

Rev.	Date	Description	
		Page	Summary
Rev.1.00	Jun.01.23	-	First Edition

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