

This document describes the following items. Refer to the user's manual for cautions on using an in-circuit emulator.

- Restrictions not applicable to the target device but applicable to an in-circuit emulator
- Restrictions applicable to both the target device and an in-circuit emulator but the correction is planned only for the in-circuit emulator

Also refer to the following documents for the restrictions in the target device.

- User's manual of target device
- Restrictions notification document for target device

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Chapter 1. Product Version

The product versions of Renesas Electronics in-circuit emulators IECUBE are indicated by a control code. The control code is the second digit from the left in the 10-digit serial number. On the back of IECUBE are labeled in Figure 1. The red frame control code in Figure 1. If the product has been upgraded, the control code can be checked by 'IECUBE Self Check Tool'. Please start 'IECUBE Self Check Tool' and press START button, and then IECUBE information is displayed (Figure 2).

To start 'IECUBE Self Check Tool' check following place.

[Start]→[programs]→[Renesas Electronics CubeSuite+]→[Emulator Utilities]→[78K0R]→[IECUBE Self Check Tool]

Figure 1. Checking Control Code (Label on QB-78K0RFX3)

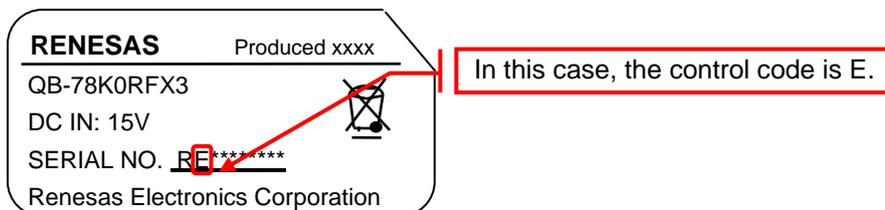
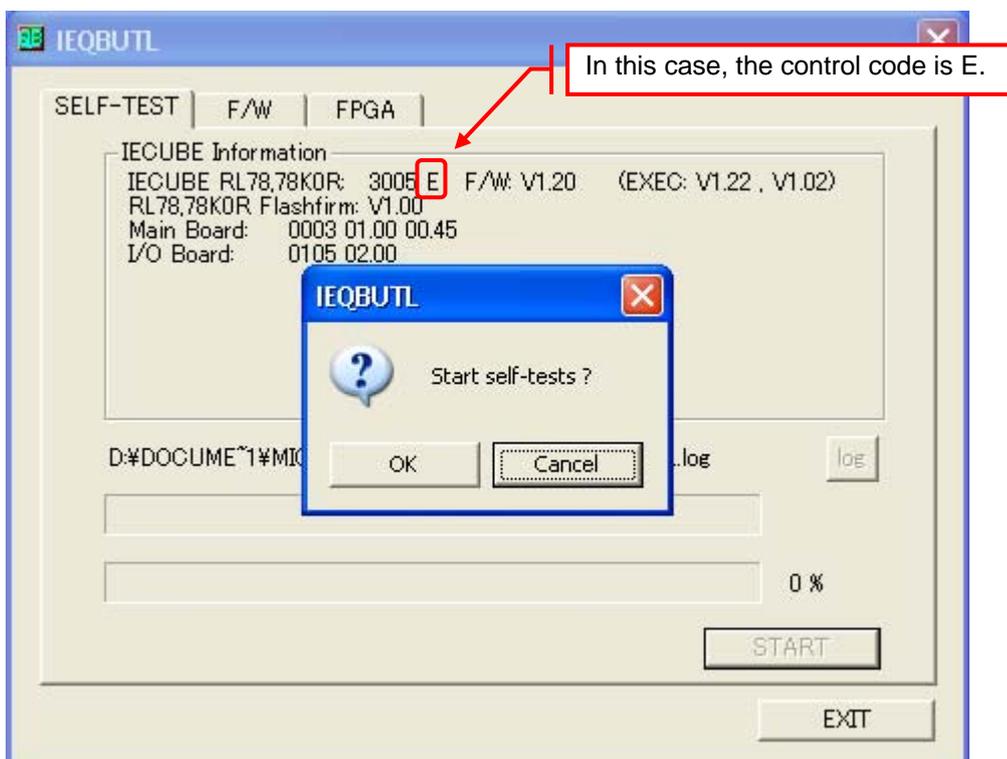


Figure 2. Checking Control Code for 'IECUBE Self Check Tool'



Chapter 2. Support Devices

Control Code	Supported Devices
A,B,C,D	uPD78F1804, uPD78F1805, uPD78F1806, uPD78F1807, uPD78F1808, uPD78F1809, uPD78F1810, uPD78F1811, uPD78F1812, uPD78F1813, uPD78F1814, uPD78F1815, uPD78F1816, uPD78F1817, uPD78F1818, uPD78F1819, uPD78F1820, uPD78F1821, uPD78F1822, uPD78F1823, uPD78F1824, uPD78F1825, uPD78F1826, uPD78F1827, uPD78F1828, uPD78F1829, uPD78F1830, uPD78F1831, uPD78F1832, uPD78F1833, uPD78F1834, uPD78F1835, uPD78F1836, uPD78F1837, uPD78F1838, uPD78F1839, uPD78F1840, uPD78F1841, uPD78F1842, uPD78F1843, uPD78F1844, uPD78F1845, uPD78F8064, uPD78F8065, uPD78F8066, uPD78F8067, uPD78F8068,uPD78F8069
E	uPD78F1804A, uPD78F1805A, uPD78F1806A, uPD78F1807A, uPD78F1808A, uPD78F1809A, uPD78F1810A, uPD78F1811A, uPD78F1812A, uPD78F1813A, uPD78F1814A, uPD78F1815A, uPD78F1816A, uPD78F1817A, uPD78F1818A, uPD78F1819A, uPD78F1820A, uPD78F1821A, uPD78F1822A, uPD78F1823A, uPD78F1824A, uPD78F1825A, uPD78F1826A, uPD78F1827A, uPD78F1828A, uPD78F1829A, uPD78F1830A, uPD78F1831A, uPD78F1832A, uPD78F1833A, uPD78F1834A, uPD78F1835A, uPD78F1836A, uPD78F1837A, uPD78F1838A, uPD78F1839A, uPD78F1840A, uPD78F1841A, uPD78F1842A, uPD78F1843A, uPD78F1844A, uPD78F1845A uPD78F8064, uPD78F8065, uPD78F8066, uPD78F8067, uPD78F8068,uPD78F8069

Chapter 3. Changed Specifications

3.1 List of changed specifications

No.	Restrictions	Control Code				
		A	B	C	D	E
1	On emulating the PLL clock	×	×	×	×	○

×: Change not implemented, ○: Change implemented

3.2 Details of changed specifications

No.1 On emulating the PLL clock
【contents】 QB-78K0RFX3 supported 7.3728MHz as the input frequency to PLL.
 Target devices: uPD78F8064,uPD78F8065,uPD78F8066
 uPD78F8067,uPD78F8068,uPD78F8069

Chapter 4. Restrictions

4.1 List of restrictions

No.	Restrictions	Control Code				
		A	B	C	D	E
1	Self-programming	×	×	○	○	○
2	Data flash	×	○	○	○	○
3	The limitation concerning the A/D conversion	×	×	○	○	○
4	The limitation concerning the dead lock condition of CPU	×	○	○	○	○
5	EEPROM emulation	×	×	○	○	○
6	Restriction on trace data when an interrupt occurs	×	×	×	○	○
7	On emulating the Simplified IIC function	×	×	×	×	○

–: Not relevant, ×: Applicable, ○: Corrected

4.2 Details of Restriction

No. 1 Self-programming

[Description] Self-programming is not supported.

[Work-around] There is no workaround.

[Correction] This issue has been corrected in control code C and later.

No. 2 Data flash.

[Description] Data flash is not supported.

[Work-around] There is no workaround.

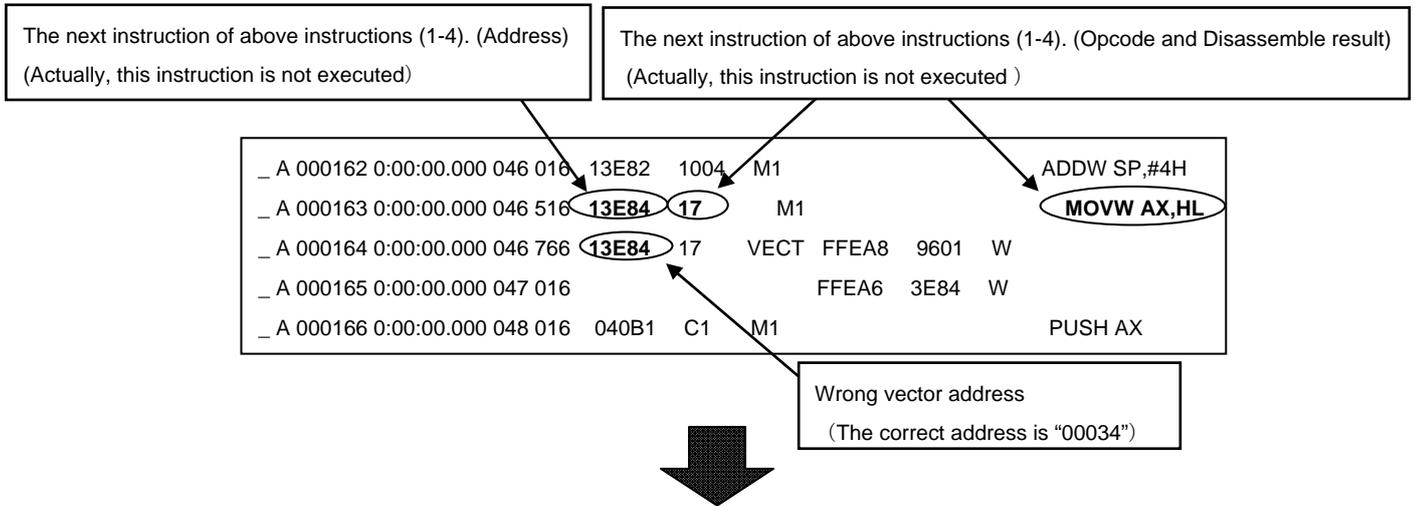
[Correction] This issue has been corrected in control code B and later.

- No. 3 The limitation concerning the A/D conversion
- [Description]** The following limitation exists about the A/D conversion.
- a. When a conversion time is short at SCAN mode, the switching noise which happens by analog selector isn't convergent. So A/D converted result comes bad.
 - b. When there is outside resistance by parasitic capacitance typ220pF of an analog selector on the O board, ANI corrupted by CR circuit. So A/D converted result comes bad.
- [Work-around]** There is no workaround.
- [Correction]** This issue has been corrected in control code C and later.
-
- No. 4 The limitation concerning the dead lock condition of CPU
- [Description]** When it meets the following requirement, CPU dead locks.
- a. The stability waiting which is at the time of FSEL change, when a counter (It's counted in 1MHz.) was the specific count, it's cleared in a BASECK. But BASECK can't take the specific counter value in case of less than 1 MHz. So it hangs up.
 - b. When STOP instruction executes right after clearing PLLON(from PLLON=1 and PLLSEL=1), it hangs up.
- [Work-around]** There is no workaround.
- [Correction]** This issue has been corrected in control code B and later.
-
- No. 5 EEPROM emulation
- [Description]** About error emulation setting for flash(code flash), 'EEPROM_Write Error(Verify)' and 'FlashBlockIVerify Error(Verify)' generate error not only at itself but also at the other one.
- [Work-around]** When you use error emulation with 'EEPROM_Write Error(Verify)' and 'FlashBlockIVerify Error(Verify)', please run twice for each function with individual error setting
- [Correction]** This issue has been corrected in control code C and later.

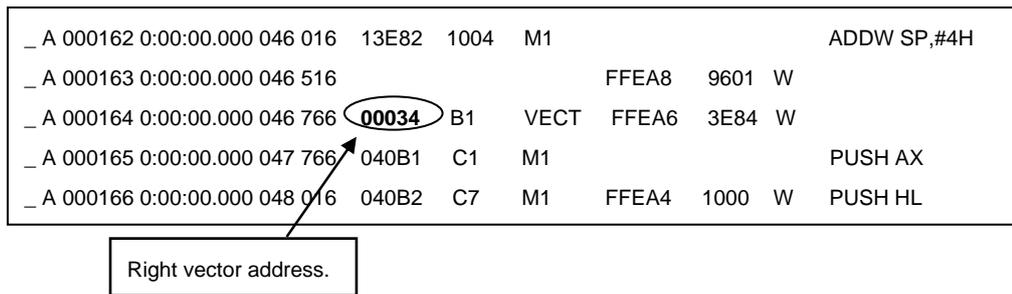
No. 6	Restriction on trace data when an interrupt occurs
[Description]	<p>If interrupt request occurs by the specific condition, a trace result may not be correct.</p> <p>Detailed condition and phenomenon are explained in the following. This is a restriction only about trace function. The instruction is executed correctly.</p> <ul style="list-style-type: none">• Condition <p>When branching to interrupt vector just after executing one of following instructions, a trace result may not be correct.</p> <ol style="list-style-type: none">1. MOVW SP, #word2. MOVW SP, AX3. ADDW SP, #byte4. SUBW SP, #byte <p>The above instructions are relevant by the following case.</p> <ul style="list-style-type: none">- In case of fetching ROM, 1, 2, 3 and 4 of the above instructions are relevant- In case of fetching RAM, 3 and 4 of the above instructions are relevant <ul style="list-style-type: none">• Phenomenon <p>When branching to interrupt vector just after executing the above instructions (1-4), the next instruction of above instructions (1-4) is not executed, thus it is not displayed on trace window. But the following contents are displayed on trace window actually.</p> <ul style="list-style-type: none">- The next instruction of above instructions (1-4)- The wrong vector address
[Work-around]	There is no workaround.
[Correction]	This issue has been corrected in control code D and later.

An example of trace data before and after the correction of this restriction is shown below.

[Before correction]



[After correction]



- No. 7 On emulating the simplified IIC function
- [Description]** When emulating the simplified IIC function, the QB-78K0RFX3, which is used as the master of signal transmission, cannot acknowledge the ACK signal from the slave device.
- [Work-around]** There is no workaround.
- [Correction]** This issue has been corrected in control code E and later.

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Renesas Electronics America Inc.
2880 Scott Boulevard, Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavi'd or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141