CubeSuite+ Simulator for V850ES/Jx2 V3.00.03

Release Note

R20UT2508EJ0100
Rev.1.00
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Contents

Chapter 1. Target Devices

Below is a list of devices supported by the V850ES/Jx2 simulator.

Nickname	Device name
V850ES/JG2	μPD70F3715, μPD70F3716, μPD70F3717, μPD70F3718, μPD70F3719
V850ES/JJ2	μPD70F3720, μPD70F3721, μPD70F3722, μPD70F3723, μPD70F3724
V850ES/JG3	μPD70F3739, μPD70F3740, μPD70F3741, μPD70F3742
V850ES/JJ3	μPD70F3743, μPD70F3745, μPD70F3744, μPD70F3746
V850ES/JC3-L	μPD70F3797, μPD70F3798, μPD70F3799, μPD70F3800, μPD70F3801, μPD70F3802, μPD70F3803, μPD70F3804
V850ES/JE3-L	μPD70F3805, μPD70F3806, μPD70F3807, μPD70F3808
V850ES/JF3-L	μPD70F3735, μPD70F3736
V850ES/JG3-L	μPD70F3737, μPD70F3738, μPD70F3792, μPD70F3793, μPD70F3794, μPD70F3795, μPD70F3796
V850ES/JC3-H	μPD70F3809, μPD70F3810, μPD70F3811, μPD70F3812, μPD70F3813, μPD70F3814, μPD70F3815, μPD70F3816, μPD70F3817, μPD70F3818, μPD70F3819
V850ES/JE3-H	μPD70F3820, μPD70F3821, μPD70F3822, μPD70F3823, μPD70F3824, μPD70F3825
V850ES/JG3-H	μPD70F3760, μPD70F3761, μPD70F3762, μPD70F3770
V850ES/JH3-H	μPD70F3765, μPD70F3766, μPD70F3767, μPD70F3771
V850ES/JG3-U	μPD70F3763, μPD70F3764
V850ES/JH3-U	μPD70F3768, μPD70F3769

Chapter 2. User's Manuals

Please read the following user's manuals together with this document.

Manual Name	Document Number
CubeSuite+ V2.00.00 V850 Debug	R20UT2446EJ0100
CubeSuite+ V2.00.00 Message	R20UT2448EJ0100

Chapter 3. Key Word for Uninstallation

To uninstall this product, use the integrated uninstaller (uninstalls CubeSuite+).

Chapter 4. Changes

This chapter describes changes from V3.00.02 to V3.00.03.

4.1 Specifications changed

4.1.1 Simulation on CubeSuite+ V2.00.00

Support simulation on CubeSuite+ V2.00.00. There is no functional change.

Chapter 5. Cautions

This section describes cautions for using the V850ES/Jx2 simulator. The following two types of caution are described:

•Differences between target devices and simulator : Differences from behavior of target devices due to simulator specifications

•Notes for using simulator GUI : Notes for using the simulator GUI window

5.1 Differences between target devices and simulator

5.1.1 Unsupported peripheral functions

The simulator does not support the following peripheral functions of the target device (the following functions cannot be debugged on the simulator).

* Flash self programming function
* CRC function
* Clock monitor
* Regulator
* USB function controller
* USB host controller
* CAN controller
* IIC

5.1.2 Reset

If a reset is generated by the low voltage detector circuit, the simulator will display "STANDBY" in the status bar. (The status is actually reset, not standby.)

And the behavior differs as follows if a reset is generated by the RESET pin.

[Target device]

Goes into reset status when the RESET pin goes to low level. Reset status is released when it goes to high level.

[Simulator]

Does not go into reset status when the RESET pin goes to low level. When it goes to high level, the simulator momentarily goes into reset status, and then the reset status is released immediately.

5.1.3 Oscillation stabilization time and lock-up time of clock generator

The simulator does not simulate the oscillation stabilization time of the clock generator. For this reason, no matter what value the oscillation stabilization time selection register (OSTS) is set to, the simulator's oscillation stabilization time is always 0 seconds. Therefore, the value of CCLS register is always "00H".
The simulator also does not simulate the PLL's lock-up time. No matter what value the PLL lock-up time specification register (PLLS) is set to, the lock-up time is always 0 seconds. Additionally, bit 0 (the LOCK bit) of the lock register (LOCKR) is cleared at the same time as the above lock-up.

5.1.4 Internal feedback resister of main clock and sub clock

The simulator does not simulate the internal feedback resister of the main clock or sub clock. For this reason, the main clock and sub clock will always oscillate, regardless of the settings of the MFRC and FRC bits on the processor clock control register (PCC).

5.1.5 Port function

If both of the conditions below are met, then the simulator will ignore writes to the port registers (e.g. P0 and PDL). Don’t perform writes under the conditions below.
[Conditions for ignoring writes to port registers]

* The corresponding bit of the port mode control register (e.g. PMC0 or PMCDL) is set to 1 (port's dual function is enabled)
* The corresponding bit of the port mode register (e.g. PM0 or PMDL) is clear to 0 (set to output mode)

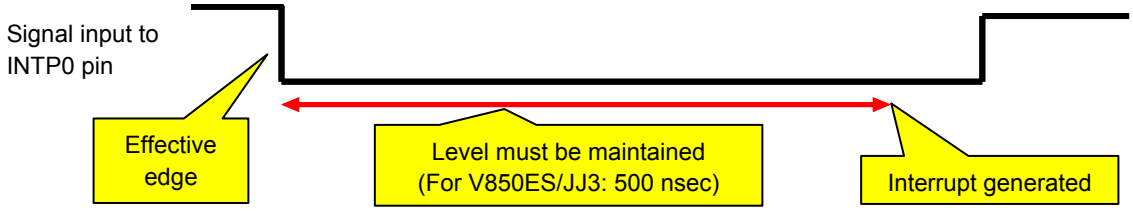
5.1.6 Noise reduction circuit for external-interrupt pin

The simulator does not simulate the noise reduction circuit. For example, if you input the active level to an external-interrupt pin with a noise reduction circuit, the interrupt will be received even if the active-level amplitude is too low.

The example below considers the case when there is input to the INTP0 pin.

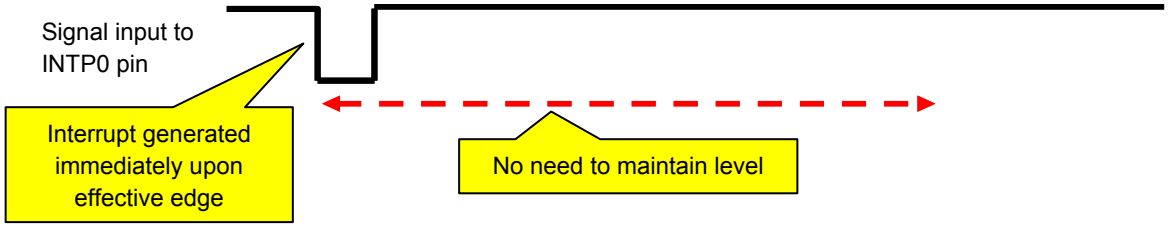
There is a noise reduction circuit on the INTP0 pin of the target device. For this reason, in order to generate an interrupt, it is necessary to input an effective edge to the target device, and subsequently maintain the signal level. (See the user's manual of the target device for the length of time it must be maintained.)

Target device behavior (falling effective edge)



In the case of the simulator, however, this noise reduction circuit is not simulated. For this reason, an interrupt will be generated any time a valid edge is generated. (No need to maintain signal level).

Simulator behavior (falling effective edge)



5.1.7 External bus interface functions

Some of the external bus interface functions can be simulated, and some cannot.

[Functions that can be simulated]

* ROM and RAM connection
* Access to connected ROM/RAM

[Functions that cannot be simulated]

* External bus-related SFR simulation (External bus access is possible even without configuring SFR.)
* Check signal input to external bus pins in the Timing Chart window
  (It will appear as high impedance.)
* Input to WAIT or HLDRQ pin (It will be ignored.)
* Access Speed (always 0 clock)

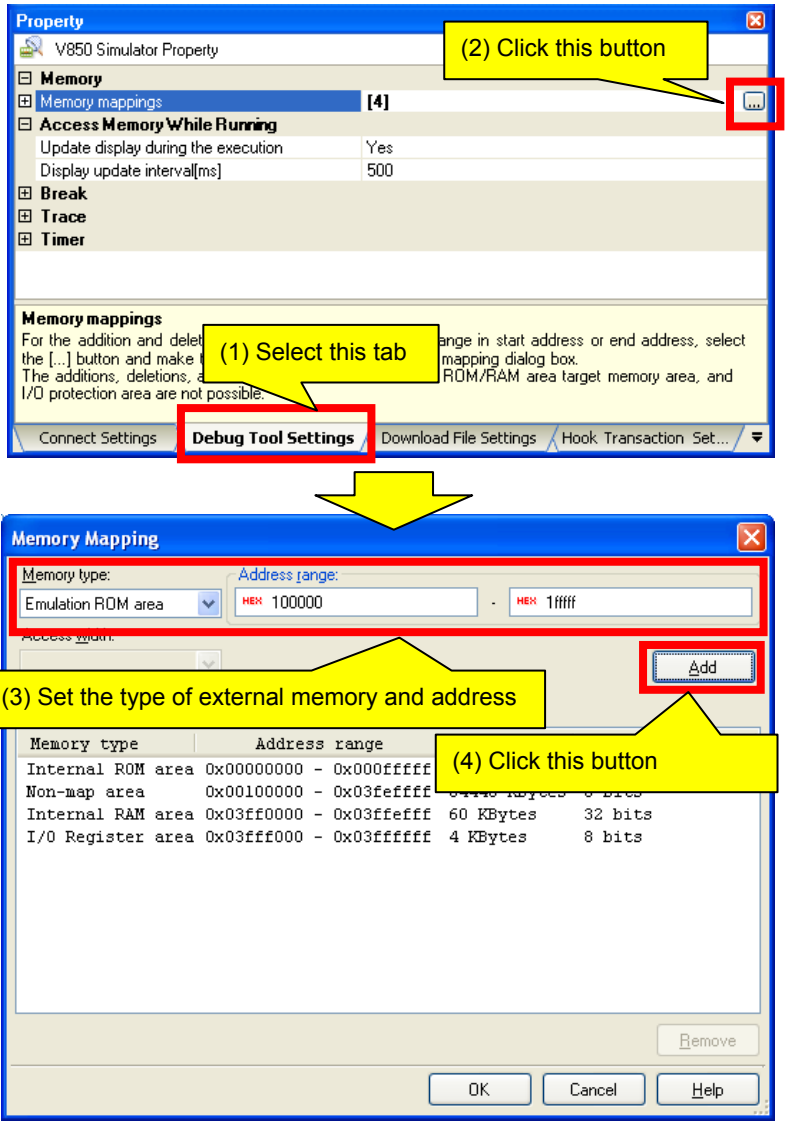
When connecting ROM or RAM to the external bus, perform configuration in the Property panel, from the Debugging Tool Setting tab.

Connect by entering:

* Type of memory to connect to (emulation ROM area or emulation RAM area)
* Memory address to connect to

This setting enables both:

* Writing to external bus
* Reading from external bus



5.1.8 DMA controller

The transfer speeds of the target device and simulator differ as follows when simulating the DMA controller.

[Target device]

* The time required for a DMA transfer is: DMA response time + memory access time of transfer source + 1 clock cycle + memory access time of transfer destination.
* If there is a contention of DMA transfer timing between CPU bus access and DMA bus access by another channel, then the bus access with the lower priority waits until the bus access with the higher priority completes.

[Simulator]

* It takes zero clock cycles to complete one DMA transfer.
* If there is a contention of DMA transfer timing between CPU bus access and DMA bus access by another channel, then the bus accesses are performed simultaneously.

5.1.9 Noise filter on asynchronous serial interface

Although the target device's asynchronous serial interfaces (UARTA/UARTC) have a noise filter to reduce noise on the input pin, the simulator does not simulate this. Since there is no noise in the simulator's signal, it would be meaningless to simulate this function.

5.1.10 Baud rate of asynchronous serial interface

If the baud rate of the asynchronous serial interface (UARTA/UARTC) is set to 233 bps or lower, operation will be abnormal (it will operate at a higher baud rate than the one set). Don’t specify a baud rate that is 233 bps or lower.

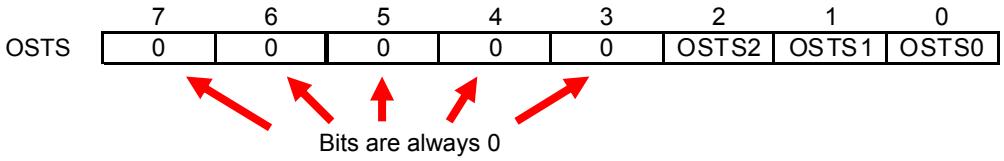
5.1.11 Baud rate clock input of asynchronous serial interface

Although the target device's asynchronous serial interfaces (UARTA/UARTC) have ASCKA0 and ASCKC0 pins as baud rate clock input pins, the simulator does not simulate this. Inputs of baud rate clocks to these pins are ignored.

5.1.12 Constant 0/1 bits of I/O registers

The I/O register has bits that are always 0 or 1.

For example, bits 3 to 7 are always 0 for the oscillation stabilization time selection register (OSTS).



Although the values of these bits cannot be changed from the target device, the can be changed from the simulator. Note that changing these values has no effect on behavior.

5.1.13 Stabilization time of A/D converter

The simulator does not simulate the stabilization time of the A/D converter. This causes the following differences in behavior.

[Time from start to end of A/D conversion on target device]

* Normal conversion mode: stabilization time + conversion time + wait time
* High-speed conversion mode: stabilization time + conversion time
* Continuous conversion mode: stabilization time + conversion time (first conversion), conversion time (second and subsequent conversions)

[Time from start to end of A/D conversion on simulator]

* Normal conversion mode: conversion time + wait time
* High-speed conversion mode: conversion time
* Continuous conversion mode: conversion time

5.1.14 Default voltage of AV_{REF0} pin and AV_{REF1} pin

Default voltage of AV_{REF0} pin is 3.3V. And default voltage of AV_{REF1} pin is 3.6V.

Note : The meaning of "Default voltage " is the voltage when the pin have no connection.

5.1.15 Capture trigger of 16-bit timer/event counter Q (TMQ)

The simulator does not support the CAN controller. For this reason, you should not select the CAN0's TSOUT signal as the TIAB02 pin's capture trigger input signal, as the capture trigger of the 16-bit timer/event counter AB (TAB) (do not set the ISEL0 bit of selector operation control register 0 (SELCNT0) to 1). If this setting is made, the capture trigger will not be activated.

5.1.16 Noise filter of 16-bit timer/event counter

Although the target device's 16-bit timer/event counters AA (TAA) and T (TMT) have noise filters to reduce noise on the input pin, the simulator does not simulate this. Since there is no noise in the simulator's signal, it would be meaningless to simulate this function.

5.1.17 1-Hz pin output of real-time counter

If the waveform of the RTC1HZ pin is checked in the timing chart window using 1 Hz pin output of the real-time counter, the output waveform has a frequency of 32.768 Hz.

In this case, determine that 1 Hz output is being performed without problems.

5.1.18 RTC back up mode

RTC back up mode simulation is supported, but simulation when turning off the power supply (VDD or EVDD) is not supported. When you want to simulate RTC back up mode, please set condition for RTC back up mode by only software.

5.1.19 Reset during RTC back up mode

Reset operations during RTC back up mode are following.

*The case pushing CPU Reset button : RTC is stopped, RTC registers are initialized.

*The case setting RESET signal level low : RTC continues to count.

5.1.20 Interrupt response time

The interrupt response times of the target device and simulator differ.

[Target device]

It takes at least 4 clock cycles after an interrupt is generated until execution branches to the handler address.

[Simulator]

Execution branches to the handler address immediately upon the interrupt.

5.1.21 Low-voltage detector

The simulator does not simulate the internal RAM data status register (RAMS). Although the initial value will be the same as the target device (0x01), the behavior differs on the following three points.

* Writing is possible without a specific sequence.
* The RAMF bit will not be set to 1 if a voltage below the RAM hold voltage is detected.
* Setting the EVARAMIN bit of peripheral emulation register 1 (PEMU1) to 1 will not cause the RAMF bit to be set to 1.

5.2 Cautions for using simulator GUI

5.2.1 Cautions for controlling each windows

The following keyboard operations are not available in the simulator windows (signal-data editor window, I/O panel window, and serial window).

* Navigation via tab or arrow keys (←, ↑, →, ↓)
* Deletion via the Del or Backspace keys
* Copy & paste and other operations via the Ctrl + C, V, X, A, or Z keys.

Perform the above operations as follows.

* Navigation: Navigate using the mouse.
* Deletion: Right click and perform the action via the context menu.
* Copy & paste, etc.: Right click and perform the action via the context menu.

5.2.2 Cautions for closing simulator GUI window

The simulator GUI window can only be closed by disconnecting from the debugging tool, or by closing CubeSuite+ proper. (The [X] button cannot be clicked.)
Additionally, although it appears that the [X] button can be pressed if Aero is enabled in Windows Vista, pressing this button will not close the GUI window.

5.2.3 Cautions for showing help for the simulator GUI window

Pressing the F1 key in the simulator GUI window will not display the help if none of the internal windows are visible (e.g. the I/O panel window).
To display the help for the simulator GUI window, from the GUI window's menu, select [Help] > [Main Window].

5.2.4 Cautions for disconnecting the debug tool

CubeSuite+ may exit if the debugging tool is disconnected while any of the following dialog boxes is open from the simulator GUI window. Make sure that the following dialog boxes are closed before disconnecting the debugging tool.

- •Save As
- •Open
- •New
- •Color
- •Font
- •Customize
- •Loop
- •Select Pin
- •Search Data
- •Format (UART)
- •Format (CSI)
- •Message (e.g. Error)
- •Parts Button Properties
- •Analog Button Properties
- •Parts Key Properties
- •Parts Level Gauge Properties
- •Parts Led Properties
- •Parts Segment LED Properties
- •Parts Matrix Led Properties
- •Parts Buzzer Properties
- •Pull up / Pull down
- •Entry Bitmap
- •Object Properties

5.2.5 Cautions for setting the Host Machine's language and region

If a Japanese OS is installed on your Host Machine, then if the language or region is set to other than Japanese/Japan, the menus and dialog-box names of the simulator GUI window will be shown in English. Similarly, if a non-Japanese OS is installed on your Host Machine, then if the language or region is set to Japanese/Japan, the menus and dialog-box names of the simulator GUI window will be shown in Japanese.

Chapter 6. Restrictions

This section describes the restrictions for the Simulator for V850ES/Jx2.

6.1 Restrictions for the Simulator for V850ES/Jx2

6.1.1 List of restrictions for the Simulator for V850ES/Jx2

No.	Target Devices	Restrictions
1	V850ES/JC3-L, V850ES/JE3-L, V850ES/JC3-H, V850ES/JE3-H	Restriction on accessing PMDL, PDL registers

6.1.2 Restriction Details for the Simulator for V850ES/Jx2

No. 1 Restriction on accessing PMDL, PDL registers

[Devices] V850ES/JC3-L, V850ES/JE3-L, V850ES/JC3-H, V850ES/JE3-H

[Description] It is impossible to access PMDL and PDL registers by 16-bit access instructions.

[Workaround] Please use 8-bit access instructions or 1-bit access instructions for accessing PMDLL and PDLL registers.

[Fix] In planning

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141