Code Generator for RL78

Introduction
Thank you for using the Code Generator for RL78. This document describes the restrictions and points for caution. Read this document before using the product. You can also check the latest release notes on the RENESAS website.

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1. Introduction

The Code Generator for RL78 is a software tool to generate control programs (device driver programs) for peripheral modules (timers, UART, A/D, etc.). It generates device driver codes using user settings through GUI. Initialize code and API (Application Programming Interface) functions are provided. The following products are provided as code generator for RL78.

- Code Generator Plug-in for RL78 (IDE CS+ for CC, CS+ for CA,CX, e² studio)
- AP4 for RL78
- Applilet3 for RL78

1.1 Product version

- CS+ Code Generator for RL78 (CS+ for CC) 2.19.00
- CS+ Code Generator for RL78 (CS+ for CA,CX) 2.19.00
- e² studio V7.8.0 Code Generator Plug-in 2.15.1
- e² studio 2020-04 (64-bit) Code Generator Plug-in 2.16.100
- AP4 for RL78 1.18.00 (3.08.04.01)

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- Applilet3 for RL78 1.18.00 (1.10.05.01)

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1.2 Operating environments

1.2.1 PC
- IBM PC/AT compatible (Windows® 10, Windows® 8.1)
- Processor: At least 1 GHz (the product supports hyper-threading and multi-core CPUs)
- Memory capacity: 2 GB or more is recommended. At least 1 GB (or 2 GB for 64-bit versions of Windows®) is required.
- Hard disk capacity: At least 200 MB available
- Display resolution: 1024x768 or higher; at least 65536 colors
- Required elements of the software environment other than the Windows OS: .NET Framework 4.5 plus a language pack

1.2.2 Development tools

1.2.2.1 CS+
- Integrated development environment CS+ from Renesas, V8.03.00 or later
- Renesas electronics Compiler for RL78 [CC-RL] V1.08 or later
- Renesas electronics Compiler for 78K0R [CA78K0R] V1.30 or later

1.2.2.2 e² studio, AP4 for RL78 and Applilet3 for RL78
- Integrated development environment e² studio (64-bit) from Renesas, 2020-04 or later
- Integrated development environment e² studio (32-bit) from Renesas, V7.8.0 or later
- Renesas electronics Compiler for RL78 [CC-RL] V1.08 or later
- Renesas GCC for RL78 V4.9 or later
- IAR Embedded Workbench for Renesas RL78 V2.21 or later
## 2. Supported devices

The devices supported by the Code Generator for RL78 are listed below.

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Table 2-5. Supported devices

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3. Changes

Describes the changes in this release of the Code Generator for RL78.

3.1 List of Changes

Table 3-1. List of Points for Change 1/2

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Table 3-2. List of Points for Change 2/2

<table>
<thead>
<tr>
<th>No</th>
<th>Description</th>
<th>Group</th>
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<tr>
<td></td>
<td></td>
<td>RL78/F12</td>
</tr>
<tr>
<td>1</td>
<td>Supports e² studio 64-bit version</td>
<td>○</td>
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</table>

3.2 Details of Changes

3.2.1 Supports e² studio 64-bit version

The Code Generator can be used in e² studio 2020-04 (64-bit).
4. History of Corrections Announced in Renesas Tool News

This section is a summary of corrections announced in Renesas Tool News.

<table>
<thead>
<tr>
<th>Issue Date</th>
<th>Document No.</th>
<th>Description</th>
<th>Device Concerned</th>
<th>Fixed version</th>
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<tbody>
<tr>
<td>May 21, 2012</td>
<td>120521/tn2</td>
<td>With generating codes for the R5F1007x and R5F1017x MCUs, RL78/G13 group</td>
<td>RL78/G13</td>
<td>CS+ V1.00.06</td>
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<tr>
<td>Aug. 01, 2012</td>
<td>120801/tn3</td>
<td>Problems arising in Applilet3 for RL78/G13 and Applilet3 for RL78/G14</td>
<td>RL78/G13, RL78/G14</td>
<td>CS+ V1.00.06</td>
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<tr>
<td>Sep. 01, 2012</td>
<td>120901/tn1</td>
<td>With using the code generator for the RL78/G12 group</td>
<td>RL78/G12</td>
<td>CS+ V1.00.06</td>
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<tr>
<td>Feb. 01, 2013</td>
<td>130201/tn1</td>
<td>With using the code generator for the RL78/G14 group of MCUs</td>
<td>RL78/G14</td>
<td>CS+ V2.00.00</td>
</tr>
<tr>
<td>Jul. 01, 2013</td>
<td>130701/tn1</td>
<td>When edited source codes disappear</td>
<td>RL78/F12, RL78/F13, RL78/F14, RL78/F15, RL78/G10, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/G1C, RL78/G1D, RL78/G1E, RL78/G1F, RL78/G1G, RL78/G1H, RL78/I1A, RL78/I1D, RL78/I1E, RL78/L12, RL78/L13, RL78/L1C</td>
<td>CS+ V2.11.00</td>
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<tr>
<td></td>
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<td>When the port cannot be set properly</td>
<td>RL78/G1A</td>
<td>CS+ V2.00.01</td>
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<tr>
<td>Aug. 01, 2013</td>
<td>130801/tn1</td>
<td>With using the code generator for the RL78/G12 group of MCUs</td>
<td>RL78/G12</td>
<td>CS+ V2.00.01</td>
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<tr>
<td>Oct. 16, 2013</td>
<td>131016/tn1</td>
<td>2. When a RL78/G13 product in a 100-pin package is selected</td>
<td>RL78/G13</td>
<td>CS+ V2.03.00</td>
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<td>3. With the key input interrupt setting</td>
<td>RL78/L12</td>
<td>CS+ V2.03.00</td>
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<td>4. With A/D converter operation setting</td>
<td>RL78/G1A</td>
<td>CS+ V2.03.00</td>
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<tr>
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<td></td>
<td>5. When the timer KB20 is in use</td>
<td>RL78/L13</td>
<td>CS+ V2.03.00</td>
</tr>
<tr>
<td>Issue Date</td>
<td>Document No.</td>
<td>Description</td>
<td>Device Concerned</td>
<td>Fixed version</td>
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<tr>
<td>Apr. 16, 2014</td>
<td>140416/tn5</td>
<td>With selecting the 20-pin, 30-pin, or 32-pin package for the RL78/F13 or RL78/F14 group</td>
<td>RL78/F13, RL78/F14</td>
<td>CS+ V2.04.00</td>
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<td>With using the remote control carrier wave mask signal in the RL78/L12 or RL78/L13 group</td>
<td>RL78/L12, RL78/L13</td>
<td>CS+ V2.04.00</td>
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<td>With processing to reflect the pin configurator when the A/D converter is set in the RL78/G12 group</td>
<td>RL78/G12</td>
<td>CS+ V2.04.00</td>
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<tr>
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<td>With the case when ports that are not available in the MCU are displayed in the RL78/G14 group</td>
<td>RL78/G14</td>
<td>CS+ V2.04.00</td>
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<tr>
<td>Jul. 01, 2014</td>
<td>140701/tn1</td>
<td>With setting port 2</td>
<td>RL78/L13</td>
<td>CS+ V2.07.00</td>
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<tr>
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<td>With setting an interval timer</td>
<td>RL78/G10, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/G1C, RL78/L12, RL78/L13, RL78/L1C, RL78/I1A</td>
<td>CS+ V2.07.00</td>
</tr>
<tr>
<td>Aug. 16, 2014</td>
<td>140816/tn1</td>
<td>With setting of P20 and P21 of port2</td>
<td>RL78/L1C</td>
<td>CS+ V2.05.00</td>
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<td>With setting of port1</td>
<td>RL78/G14</td>
<td>CS+ V2.05.00</td>
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<tr>
<td>Nov. 1, 2014</td>
<td>141101/tn2</td>
<td>1. Point for Caution on Settings for CPU Stack Pointer Monitoring</td>
<td>RL78/F13</td>
<td>CS+ V2.07.00</td>
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<td>2. Point for Caution on Writing to the Serial Flag Clear Trigger Register (SIR) When Using 3-wire Serial (CSI) Transfer</td>
<td>RL78/F14</td>
<td>CS+ V2.07.00</td>
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<td>1. Code Generated for Comparator Settings</td>
<td>RL78/I1A</td>
<td>CS+ V2.07.00</td>
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<tr>
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<td>2. DTC Settings</td>
<td>RL78/F13, RL78/F14</td>
<td>CS+ V2.07.00</td>
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<td>3. Setting the Voltage Detection Circuit to &quot;Interrupt Mode&quot;</td>
<td>RL78/L12, RL78/I1A, RL78/G1A, RL78/F13, RL78/F14</td>
<td>CS+ V2.07.00</td>
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<td>Dec. 16, 2014</td>
<td>141216/tn3</td>
<td>4. Saving Projects with Settings for the A/D Convertor</td>
<td>RL78/L1C</td>
<td>CS+ V2.07.00</td>
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<td>5. Reflection of Pin Configurations in Generated Code</td>
<td>RL78/G12, RL78/G13, RL78/G14</td>
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<td>Description</td>
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<tr>
<td>Jul. 16, 2015</td>
<td>150716/tn2</td>
<td>1. Clock Generation Circuit (PLL Circuit Operation)</td>
<td>RL78/F13, RL78/F14, RL78/G1C, RL78/L1C</td>
<td>CS+ V2.11.00</td>
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<td>AP4 V1.10.00</td>
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<td>2. Setting P40 of Port 4</td>
<td>RL78/F12, RL78/F13, RL78/F14, RL78/G10, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/G1C, RL78/G1E, RL78/G1F, RL78/G1G, RL78/I1A, RL78/I1D, RL78/L1C, RL78/L12, RL78/L13</td>
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<td>3. Code Generated for UART0 and UARTF</td>
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<td>Nov. 16, 2015</td>
<td>151116/tn2</td>
<td>1. Indication of Channels of Serial Interface IICA</td>
<td>RL78/G14</td>
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<td>2. Procedure for Setting the PLL Clock</td>
<td>RL78/F13, RL78/F14, RL78/F15</td>
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<tr>
<td>Jan. 16, 2016</td>
<td>160116/tn5</td>
<td>Transfer of data with a length of 10 or more bits through an element of a</td>
<td>RL78/F12, RL78/F13, RL78/F14, RL78/F15, RL78/D1A</td>
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<td>through an element configured as a UART</td>
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<tr>
<td>Feb. 16, 2016</td>
<td>160216/tn5</td>
<td>1. Using the error interrupt of serial array unit 4 as UART4 or DALI4</td>
<td>RL78/I1A</td>
<td>CS+ V2.11.00</td>
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<td>2. Using serial array unit 4 as DALI4</td>
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<tr>
<td>Mar. 16, 2016</td>
<td>160316/tn1</td>
<td>Pin settings for the IICA serial interface when setting the PIOR to change</td>
<td>RL78/G12</td>
<td>CS+ V2.11.00</td>
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<tr>
<td></td>
<td></td>
<td>the assignment of pin functions</td>
<td></td>
<td>Applilet3 V1.10.00</td>
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<tr>
<td>Issue Date</td>
<td>Document No.</td>
<td>Description</td>
<td>Device Concerned</td>
<td>Fixed version</td>
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<tr>
<td>Jun. 16, 2016</td>
<td>R20TS003 8EJ0100</td>
<td>Scan Mode of A/D Converter</td>
<td>RL78/F12, RL78/F13, RL78/F14, RL78/F15, RL78/G1A</td>
<td>CS+ V2.12.00, Applilet3 V1.11.00</td>
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<tr>
<td>Aug. 01, 2016</td>
<td>R20TS004 5EJ0100</td>
<td>Peripheral I/O redirection register 0 (PIOR0)</td>
<td>RL78/G1F</td>
<td>CS+ V2.12.00, AP4 V1.11.00</td>
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<tr>
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<td>2. Port Settings Related to Reset Processing</td>
<td>RL78/F12 (20pin product)</td>
<td>CS+ V2.14.00, Applilet3 V1.13.00</td>
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<tr>
<td>Dec. 16, 2017</td>
<td>R20TS024 4EJ0100</td>
<td>When Continuous Transfer Mode is Selected in the CSI Configuration</td>
<td>RL78/D1A, RL78/F12, RL78/F13, RL78/F14, RL78/F15, RL78/L12</td>
<td>CS+ V2.16.00</td>
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<td>Mar. 16, 2018</td>
<td>R20TS029 0EJ0100</td>
<td>When Opening a Project for RL78/G11 Created by a Previous Version of Code Generator</td>
<td>RL78/G11 (20-pin R5F1056A)</td>
<td>CS+ V2.16.00, AP4 V1.15.00, Applilet3 V1.15.00</td>
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<tr>
<td>May. 16, 2018</td>
<td>R20TS031 3EJ0100</td>
<td>Writing to Port-Related Registers for Unused Pins</td>
<td>RL78/I1D</td>
<td>CS+ V2.16.00, AP4 V1.15.00</td>
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<tr>
<td>Nov. 16, 2018</td>
<td>R20TS037 0EJ0100</td>
<td>When setting the Serial UART4</td>
<td>RL78/I1A</td>
<td>CS+ V2.17.00, Applilet3 V1.16.00</td>
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<tr>
<td>Jun. 1, 2019</td>
<td>R20TS043 2EJ0100</td>
<td>1. PLL clock setting of clock generator</td>
<td>RL78/F13, RL78/F14, RL78/F15</td>
<td>CS+ V2.18.00, Applilet3 V1.17.00</td>
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<td>2. RTC operation clock setting of clock generator</td>
<td>RL78/F13, RL78/F14, RL78/F15</td>
<td>CS+ V2.18.00, Applilet3 V1.17.00</td>
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<td>RL78/D1A</td>
<td>CS+ V2.19.00, Applilet3 V1.18.00</td>
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<tr>
<td>Issue Date</td>
<td>Document No.</td>
<td>Description</td>
<td>Device Concerned</td>
<td>Fixed version</td>
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<tr>
<td>2019/08/01</td>
<td>R20TS045 9JJ0100</td>
<td>1. When using IICA0 or IICA1 as a Single Master System</td>
<td>RL78/G10, RL78/G11, RL78/G12, RL78/G13, RL78/G14, RL78/F12, RL78/F13, RL78/F14, RL78/F15</td>
<td>CS+ V2.19.00 AP4 V1.18.00 Applilet3 V1.18.00</td>
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<tr>
<td>2019/08/01</td>
<td>R20TS045 9JJ0100</td>
<td>2. When using the R_ADC_Set_ADChannel() function in the A/D converter</td>
<td>RL78/D1A, RL78/G1A, RL78/G1F, RL78/I1D</td>
<td>Not supported</td>
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<tr>
<td>2019/09/16</td>
<td>R20TS047 2JJ0100</td>
<td>1. When using the data flash library</td>
<td>RL78/D1A, RL78/G11, RL78/G12, RL78/G13, RL78/G14, RL78/F12, RL78/F13, RL78/F14, RL78/F15</td>
<td>CS+ V2.19.00 AP4 V1.18.00 Applilet3 V1.18.00</td>
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</tbody>
</table>
5. Restrictions

This section describes the restriction regarding the Code Generator for RL78.

5.1 List of Restrictions

Table 5-1. List of Points of Restriction 1/2

<table>
<thead>
<tr>
<th>No</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>RL78D1A</td>
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<tr>
<td>1</td>
<td>Timer array unit input clock sauce</td>
<td>/</td>
</tr>
<tr>
<td>2</td>
<td>24-pin device TAU0 channel 1 setting restriction</td>
<td>/</td>
</tr>
<tr>
<td>3</td>
<td>Real-time clock API function</td>
<td>/</td>
</tr>
<tr>
<td>4</td>
<td>Unit for 'Gain setting' of ( \Delta \Sigma ) A/D CONVERTER</td>
<td>/</td>
</tr>
<tr>
<td>5</td>
<td>Restrictions on CSI continuous transfer mode</td>
<td>/</td>
</tr>
<tr>
<td>6</td>
<td>Incorrect clock mode selection (SELPLL) of R_CGC_Set_ClockMode() function</td>
<td>/</td>
</tr>
<tr>
<td>7</td>
<td>Incorrect function description in data lash library</td>
<td>/</td>
</tr>
<tr>
<td>8</td>
<td>Operation clock when fSUB and fIL are selected in TAU input pulse interval measurement</td>
<td>/</td>
</tr>
<tr>
<td>9</td>
<td>64-bit environment restrictions</td>
<td>/</td>
</tr>
</tbody>
</table>

○: Applicable, /: Not applicable
Table 5-2. List of Points of Restriction 2/2

<table>
<thead>
<tr>
<th>No</th>
<th>Description</th>
<th>Group</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Timer array unit input clock sauce</td>
<td>○ ○ ○ / / / / / / / / / / / / / / / /</td>
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<td>2</td>
<td>24-pin device TAU0 channel 1 setting restriction</td>
<td>/ / / / / / / / / / / / / / / / / /</td>
</tr>
<tr>
<td>3</td>
<td>Real-time clock API function</td>
<td>/ / / / / / / / / / ○ / / / / / /</td>
</tr>
<tr>
<td>4</td>
<td>Unit for &quot;Gain setting&quot; of ΔΣ A/D CONVERTER</td>
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<tr>
<td>5</td>
<td>Restrictions on CSI continuous transfer mode</td>
<td>/ / / / / ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○ ○</td>
</tr>
<tr>
<td>6</td>
<td>Incorrect clock mode selection (SELPLL) of R_CGC_Set_ClockMode() function</td>
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</tr>
<tr>
<td>7</td>
<td>Incorrect function description in data lash library</td>
<td>○ ○ ○ ○ / / / / / / ○ / / / / / /</td>
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<tr>
<td>8</td>
<td>Operation clock when fSUB and fIL are selected in TAU input pulse interval measurement</td>
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</tr>
<tr>
<td>9</td>
<td>64-bit environment restrictions</td>
<td>/ / / / / / / / / / / / / / / / / /</td>
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</table>
5.2 Details for Restriction

5.2.1 Timer array unit input clock sauce
When the clock sauce of a timer input is set as a RTC1HZ output by setup of a timer array unit, a setup about the output of the RTC1HZ terminal of a real-time clock becomes invalid. The code which outputs RTC1HZ then is not generated.

[Workaround] When you set to a RTC1HZ signal by setup of a timer array unit, please choose a setup which uses a real-time clock and add the code which outputs RTC1HZ.

5.2.2 24-pin device TAU0 channel 1 setting restriction
In the 24-pin device, interval timer is only selectable for the TAU0 channel 1 setting.

[Workaround] There is no workaround.
In the 32-pin device, other timer functions besides "Interval timer" are selectable for the TAU0 channel 1 setting. Refer to the setting to make a correction.

5.2.3 Real-time clock API function
An unnecessary wait time code is output in the R_RTC_Set_AlarmOn().

```c
/* Change the waiting time according to the system */
for (w_count = 0U; w_count < RTC_WAITTIME_2FRTC; w_count++)
{
    NOP();
}
```

[Workaround] There is no workaround.
I Delete the wait time code in the R_RTC_Set_AlarmOn () function after generating the code.

5.2.4 Unit for 'Gain setting' of ΔΣ A/D CONVERTER
The unit of Multiplexer 0/1/2/3(Internal)/3(external) are 'db' but it should be 'Gain'.

[Workaround] Please interpret ‘db’ as ‘Gain’ when use GSET01 and/or GSET02.
5.2.5 Restrictions on CSI continuous transfer mode

When CSI is used in continuous transfer mode, 2 bytes are received even if 1 is specified in the function argument.

[Workaround] Change the code in the red frame below. If code generation is executed again after changing the code, the code will be overwritten and deleted, so be caution.

[R_CSIn_Receive() function] case with CSI00

Before:
```c
MD_STATUS R_CS100_Receive(uint8_t * const rx_buf, uint8_t rx_num) {
    MD_STATUS status = MD_OK;
    if (rx_num < 1U) {
        status = MD_ARGERROR;
    } else {
        SNR00 |= _0001_SAU_BUFFER_EMPTY;
        g_cs100_rx_length = rx_num;  /* receive data length */
        g_cs100_rx_count = 0U;      /* receive data count */
        g_p_cs100_rx_address = rx_buf;  /* receive buffer pointer */
        S1000 = OxFFU;    /* start receive by dummy write */
    }
    return (status);
}
```

After:
```c
MD_STATUS R_CS100_Receive(uint8_t * const rx_buf, uint8_t rx_num) {
    MD_STATUS status = MD_OK;
    if (rx_num < 1U) {
        status = MD_ARGERROR;
    } else {
        if (1U == rx_num) {
            SNR00 &= ~_0001_SAU_BUFFER_EMPTY;
        } else {
            SNR00 |= _0001_SAU_BUFFER_EMPTY;
        }
        g_cs100_rx_length = rx_num;  /* receive data length */
        g_cs100_rx_count = 0U;      /* receive data count */
        g_p_cs100_rx_address = rx_buf;  /* receive buffer pointer */
        S1000 = OxFFU;    /* start receive by dummy write */
    }
    return (status);
}
```
[R_CSIn_Send_Receive() function] case with CSI00

Before:

```c
MD_STATUS R_CS100_Send_Receive(uint8_t *const tx_buf, uint16_t tx_num, uint8_t *const rx_buf)
{
    MD_STATUS status = MD_OK;
    if (tx_num < U)
    {
        status = MD_ARGERROR;
    }
    else
    {
        g_csi00_send_length = tx_num;    /* send data length */
        g_csi00_tx_count = tx_num;       /* send data count */
        sp_csi00_tx_address = tx_buf;   /* send buffer pointer */
        sp_csi00_rx_address = rx_buf;   /* receive buffer pointer */

        if (0 == sp_csi00_tx_address)
        {
            if (0 == g_csi00_send_length)
            {
                R_CSIn_Send_Receive: /* 0001 SAU BUFFER EMPTY; */
            }
            else
            {
                R_CSIn_Send_Receive: /* 0001 SAU BUFFER EMPTY; */
            }
        }
        S16O0 = 0x00;  /* started by writing data to SDR[7:0] */
        S16O0 = 0x00;
        g_csi00_tx_count--;  /* enable INTCSI00 interrupt */
        return (status);
    }
}
```

After:

```c
MD_STATUS R_CS100_Send_Receive(uint8_t *const tx_buf, uint16_t tx_num, uint8_t *const rx_buf)
{
    MD_STATUS status = MD_OK;
    if (tx_num < U)
    {
        status = MD_ARGERROR;
    }
    else
    {
        g_csi00_send_length = tx_num;    /* send data length */
        g_csi00_tx_count = tx_num;       /* send data count */
        sp_csi00_tx_address = tx_buf;   /* send buffer pointer */
        sp_csi00_rx_address = rx_buf;   /* receive buffer pointer */

        if (0 == sp_csi00_tx_address)
        {
            if (0 == g_csi00_send_length)
            {
                R_CSIn_Send_Receive: /* 0001 SAU BUFFER EMPTY; */
            }
            else
            {
                R_CSIn_Send_Receive: /* 0001 SAU BUFFER EMPTY; */
            }
        }
        S16O0 = 0x00;  /* started by writing data to SDR[7:0] */
        S16O0 = 0x00;
        g_csi00_tx_count--;  /* enable INTCSI00 interrupt */
        return (status);
    }
}
```
5.2.6 Incorrect clock mode selection (SELPLL) of R_CGC_Set_ClockMode() function

There is an erroneous in the judgment on writing to the SELPLL bit used when switching between the main system clock (fMAIN) and PLL clock (fPLL).

```c
MD_STATUS R_CGC_Set_ClockMode(clock_mode_t mode)
{
  (Omitted)
  if (mode != old_mode)
  {
    switch (mode)
    {
      case MCLK:
        (Omitted)
      if (_00_CGC_CLK_MODE_MAIN != (PLLST & _00_CGC_CLK_MODE_MAIN))
      {
        SELPLL = 0U; /* clock through mode [MAIN] */
      }
    }
  }

[Workaround] Change the code in the red frame to "& _08_CGC_CLK_MODE_PLL".
If code generation is executed again after changing the code, the code will be overwritten and deleted, so be caution.
```

5.2.7 Incorrect function description in data lash library

There is an erroneous in the description of the R_FDL_BlankCheck() function and the R_FDL_Iverify() function. The description in Code Generator RL78 API Reference (P740-741) is the correct explanation. Please refer to it.

[Workaround] The code is not affected.

5.2.8 Operation clock when fSUB and fIL are selected in TAU input pulse interval measurement

When input pulse interval measurement is specified with TAU and fSUB and fIL are selected, the division ratio is fixed to fclk/2^6. Due to the fixed operation clock, the intended detection accuracy may not be achieved in the safety function frequency detection.

[Workaround] After code generation, change the operating clock (fMCK) of the timer mode register from CK00 to CK01. If code generation is executed again after changing the code, the code will be overwritten and deleted, so be caution.
### 5.2.9 64-bit environment restrictions

After loading project (e² studio project or AP3 project) which is saved on 32-bit environment in 64-bit environment, TAU0 channel1 input selection (refer to the red box in the figure below) can’t be kept.

[Table]

<table>
<thead>
<tr>
<th></th>
<th>TAU0</th>
<th>TAU1</th>
<th>TAU2</th>
</tr>
</thead>
<tbody>
<tr>
<td>General setting</td>
<td>Channel 0</td>
<td>Channel 1</td>
<td>Channel 2</td>
</tr>
<tr>
<td>Functions</td>
<td>Unused</td>
<td>Input pulse interval measurement</td>
<td>Unused</td>
</tr>
</tbody>
</table>

[Workaround] Custom should confirm this GUI setting after loading project in such a case.
6. **Cautions**

This section describes points for caution regarding the Code Generator for RL78.

### 6.1 List for Cautions

Table 6-1. List of Points for Caution 1/2

<table>
<thead>
<tr>
<th>No</th>
<th>Description</th>
<th>Group</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>RL78/G1A</td>
</tr>
<tr>
<td>1</td>
<td>Online Help (Applilet3, AP4)</td>
<td>○</td>
</tr>
<tr>
<td>2</td>
<td>Coding rule of MISRA-C.</td>
<td>○</td>
</tr>
<tr>
<td>3</td>
<td>High-speed on-chip oscillator frequency select register</td>
<td>○</td>
</tr>
<tr>
<td>4</td>
<td>Internal low-speed or internal high-speed oscillator trimming</td>
<td>○</td>
</tr>
<tr>
<td>5</td>
<td>Serial array unit</td>
<td>/</td>
</tr>
<tr>
<td>6</td>
<td>Flash memory CRC operation function (high-speed CRC)</td>
<td>○</td>
</tr>
<tr>
<td>7</td>
<td>Port mode select register (PMS)</td>
<td>○</td>
</tr>
<tr>
<td>8</td>
<td>LIN-bus function of UART</td>
<td>○</td>
</tr>
<tr>
<td>9</td>
<td>Extension code, wakeup function and multimaster of serial interface IICA or IIC0</td>
<td>○</td>
</tr>
<tr>
<td>10</td>
<td>CAN controllers</td>
<td>/</td>
</tr>
<tr>
<td>11</td>
<td>Safety Functions</td>
<td>○</td>
</tr>
<tr>
<td>12</td>
<td>USB</td>
<td>/</td>
</tr>
<tr>
<td>13</td>
<td>RI78V4 project</td>
<td>/</td>
</tr>
<tr>
<td>14</td>
<td>DTC function (CS+ for CA,CX)</td>
<td>○</td>
</tr>
<tr>
<td>15</td>
<td>High Speed DTC chain transfer</td>
<td>/</td>
</tr>
<tr>
<td>16</td>
<td>Fast Mode Plus setting in IICA slave</td>
<td>○</td>
</tr>
<tr>
<td>17</td>
<td>high-speed on-chip oscillator (CS+ for CA,CX)</td>
<td>/</td>
</tr>
<tr>
<td>18</td>
<td>Pin Configurator (CS+ for CA,CX)</td>
<td>/</td>
</tr>
<tr>
<td>19</td>
<td>Version notation of RL78/G13A generation file.</td>
<td>/</td>
</tr>
</tbody>
</table>

Notes: 1. These version numbers are stated in the file headers of the source code which is generated by the code generator.
### Table 6-2. List of Points for Caution 1/2

<table>
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<tr>
<th>No</th>
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<th>RL78/F1-13</th>
<th>RL78/F1-14</th>
<th>RL78/F1-15</th>
<th>RL78/F1-1E</th>
<th>RL78/I1-1A</th>
<th>RL78/I1-1B</th>
<th>RL78/I1-1C</th>
<th>RL78/I1-1D</th>
<th>RL78/I1-1E</th>
<th>RL78/I1-1F</th>
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<th>RL78/L1-1A</th>
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<th>RL78/L1-1C</th>
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</tr>
</tbody>
</table>
6.2 Details for Cautions

6.2.1 Online Help (Applilet3, AP4)
Applilet3 and AP4 do not support online help.

6.2.2 Coding rule of MISRA-C
Compliance with the MISRA-C (Guidelines for the Use of the C Language in Vehicle Based Software) coding convention is not supported for source code output by the code generator.

6.2.3 High-speed on-chip oscillator frequency select register
Code generator is not equivalent to a setup of high-speed on-chip oscillator frequency select register.

6.2.4 Internal low-speed or internal high-speed oscillator trimming
Code generator is not equivalent to a setup of internal low-speed or internal high-speed oscillator trimming register.

6.2.5 Serial array unit
Code generator is not equivalent to a setup of single-wire UART mode and DMX512 communication.

6.2.6 Flash memory CRC operation function (high-speed CRC)
Code generator does not correspond to a flash memory CRC operation function (high-speed CRC). Please refer to application note r01an0736.
https://www.renesas.com/search/keyword-search.html#genre=document&q=r01an0736

6.2.7 Port mode select register (PMS)
Code generator does not correspond to a port mode select register (PMS).

6.2.8 LIN-bus function of UART
The code generator is not supporting the LIN-bus functions of serial interface UART0, UART2, UART3, UART6 or UARTF.

6.2.9 Extension code, multimaster, wakeup function of serial interface IICA or IIC0
The code generator is not supporting the extension code, multimaster, wakeup function of serial interface IIC.

6.2.10 CAN controllers
The code generator is not supporting the CAN Controllers.

6.2.11 Safety Functions
The code generator is not supporting the USB host, USB function.
### 6.2.12 USB

The code generator is not supporting the USB host, USB function.

### 6.2.13 RI78V4 project

The Code generator can't be used in a project of RI78V4. But code generator is shown to a project of RI78V4. Even if a code is generated, RI78V4 will be an unsupported purpose build error.

### 6.2.14 DTC function (CS+ for CA,CX)

When DTC is used, the following warning message is displayed and an object file is not generated.

CC78K0R warning W0837: Output assembler source file, not object file.

**[Workaround]**

Set up the following individual option of building.

---

#### Build Settings

<table>
<thead>
<tr>
<th>Build Settings</th>
<th>Individual Compile Options</th>
<th>File Information</th>
</tr>
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</tr>
<tr>
<td><strong>File type</strong></td>
<td><strong>C source</strong></td>
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**Build Options**

- **Property:** Code Generator
- **Build:** Code Generator Preview

**Property**

- **Property:** Code Generator
- **Build:** Code Generator Preview

**Build Settings**

<table>
<thead>
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<tr>
<td><strong>Property</strong></td>
<td><strong>Code Generator</strong></td>
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**Build Settings**

- **Property:** Code Generator
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**Build Options**

- **Property:** Code Generator
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**Build Options**

- **Property:** Code Generator
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<tbody>
<tr>
<td><strong>Build Settings</strong></td>
<td><strong>Individual Compile Options</strong></td>
</tr>
<tr>
<td><strong>Property</strong></td>
<td><strong>Code Generator</strong></td>
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</tbody>
</table>
6.2.15 High Speed DTC chain transfer

Although there are chain transfer setting items of High Speed DTC, code corresponding to chain transfer is not supported.

<table>
<thead>
<tr>
<th>Normal Speed</th>
<th>High Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>DTC setting</td>
<td>DTCH0</td>
</tr>
</tbody>
</table>

High Speed Activation Source:
- Control detail (DTCH0)
- Chain transfer

[Workaround] It cannot be used for chain transfer.

6.2.16 Fast Mode Plus setting in IICA slave

If the Fast Mode Plus is set when using the IICA slave, IICA Low level range setting register (IICWLn, n= channel number), and IICA High level range setting register (IICWHLn) are not set correctly.

[Workaround] There is no workaround.

After doing code generator, please rewrite the numerical value of the register setting of IICWLn, IICWHLn in the R_IICAn_Create function. I depend on a system for the numerical value. Please change device UM to reference.

6.2.17 High-speed on-chip oscillator (CS+ for CA,CX)

When a high-speed on-chip oscillator clock is set up by CubeSuite+ RL78, 78K0R, and 78K0 code generator V2.01.00 or earlier, If it is read by CubeSuite+V2.03.00, a clock frequency setup of a high-speed on-chip oscillator may not be right.

[Workaround] Re-set up the frequency right in that case.

6.2.18 Pin Configurator (CS+ for CA,CX)

There is a pin which is not reflected even if it performs reflection to pin configurator from code generator. Even if it sets up using a code generator PIOR function, it is not reflected to pin configurator.

[Workaround] Edit terminal information with pin configurator.


The device name output in the version of the file generated by RL78/G13A is output as “RL78/G13” instead of “RL78/G13A”.

```
#!/usr/bin/env python
#
# File Name : r_main.c
# Version : CodeGenerator for RL78/G13 V2.05.04.02 [20 Nov 2018]
# Device(s) : RSF440PL
# Tool-Chain : GCC
# Description : This file implements main function.
# Creation Date: 2018/11/27
```
## Revision History

<table>
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<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Description</th>
<th>Summary</th>
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<tr>
<td>1.00</td>
<td>Oct 8, 2019</td>
<td>-</td>
<td>First edition issued</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>31</td>
<td>Update “6. Cautions” for Jan 20, 2020 release</td>
<td>-</td>
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<tr>
<td>1.02</td>
<td>Apr 20,2020</td>
<td>3</td>
<td>Updated “1.1 Product version” for Apr.20. 2020 release</td>
<td>-</td>
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<tr>
<td></td>
<td></td>
<td>4</td>
<td>Added e² studio 64-bit environment to &quot;1.2.2 Development Tools&quot;</td>
<td>-</td>
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<tr>
<td></td>
<td></td>
<td>10</td>
<td>Updated “3. Changes” for Apr.20. 2020 release</td>
<td>-</td>
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<td></td>
<td></td>
<td>16</td>
<td>Updated “5. Restrictions” for Apr.20. 2020 release</td>
<td>-</td>
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</tbody>
</table>
General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between \( V_{IL} \) (Max.) and \( V_{IH} \) (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between \( V_{IL} \) (Max.) and \( V_{IH} \) (Min.).

7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
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