ClockMatrix Firmware Version 5.4.1

Contents

1. Overview

This document describes changes in the functionality and register map between firmware version 5.4.1 and version 5.3.5.

Table 1. Related Documents

Document Title	Document Description
Device Datasheet	Contains a functional overview of a specific device and hardware design related details including pinouts, AC and DC specifications, and applications information related to power filtering and terminations.
8A3xxx Family Programming Guide v5.3 dated April 13, 2022	Contain detailed register descriptions and address maps for all members of the family of devices. All devices use some subset of this register map.
8A3xxx Family Programming Guide v5.4 dated May 1, 2024	

2. Firmware Version Number

The firmware version can be read from the GENERAL_STATUS registers as shown in the following table.

Register Module Base Address: C014h			Firmware Version v5.3.5	Firmware Version v5.4.1
Offset Address (Hex)	Individual Register Name	Register Description	Default Value	Default Value
010h	GENERAL_STATUS.MAJ_REL	Major release number	0Bh	0Bh
011h	GENERAL_STATUS.MIN_REL	Minor release number	03h	04h
012h	GENERAL_STATUS.HOTFIX_REL	Hotfix release number	05h	01h

3. Firmware Version 5.4.1 Functions Added Since Version 5.3.5

Issue Number	Description of Function
BRMBXR-3592	Added a soft control and status register (SCSR) for the received time of day (TOD) value via PWM. The new register is in module SCSR_PWM_RX_INFO.
BRMBXR-3594	Added counters in the SCSRs for PWM parity errors for each PWM decoder. The new registers are in module SCSR_PWM_RX_INFO.
BRMBXR-3597	Added TOD automatic update for PWM transmission.
BRMBXR-3621 BRMBXR-3622 BRMBXR-3641	Added support to use PWM to transmit and receive clocks that are asynchronous with the PWM carrier.

4. Improvements in Version 5.4.1 Added Since Version 5.3.5

Issue Number: BRMBXR-3555	
Firmware	**Functional Difference**
v5.3.5	When a DISQUAL_TIMER bit field is set to 1.25ms the reference monitor may generate false alarms.
v5.4.1	The issue is corrected and the reference monitors operate as intended.

Issue Number: BRMBXR-3598	
Firmware	**Functional Difference**
v5.3.5	For coarse phase measurement mode, the output of the TDC is filtered to improve measurement accuracy. The filtering is done by both the decimator filter and the loop filter. The device automatically detects steps in the filtered measured phase and opens the decimator bandwidth to respond more quickly.
v5.4.1	For coarse phase measurement mode, the output of the TDC is filtered to improve measurement accuracy. The filtering is done by the decimator filter only. The device automatically detects steps in the filtered measured phase and opens the decimator bandwidth to respond more quickly.

Issue Number: BRMBXR-3599	
Firmware	**Functional Difference**
v5.3.5	For coarse phase measurement mode, the phase measurement values are provided to the user in both the DPLLx_FILTER_STATUS field and the DPLLx_PHASE_STATUS field.
v5.4.1	For coarse phase measurement mode, the phase measurement values are provided to the user in the DPLLx_PHASE_STATUS field only. In this mode, the DPLLx_FILTER_STATUS field remains available to the user according to its description in the programming guide.

Issue Number: BRMBXR-3611	
Firmware	**Functional Difference**
v5.3.5	After a configuration is loaded, the PWM encoder must be disabled and then re-enabled for correct operation.
v5.4.1	PWM features operate as intended.

ClockMatrix Firmware Version 5.4.1 Release Notes

Issue Number: BRMBXR-3636

Firmware	Functional Difference
v5.3.5	The DPLL phase pull-in procedure does not pull-in the phase offset when DPLL_PHASE_PULL_IN_OFFSET is 1 ns and the DPLL_PHASE_PULL_IN_SLOPE_LIMIT is 1 ppb.
v5.4.1	The DPLL phase pull-in procedure does pull-in the phase offset when DPLL_PHASE_PULL_IN_OFFSET is 1 ns and the DPLL_PHASE_PULL_IN_SLOPE_LIMIT is 1 ppb.

Issue Number: BRMBXR-3639

Firmware	Functional Difference
v5.3.5	The DPLL_PHASE_PULL_IN function uses the configured DPLL_PHASE_PULL_IN_ OFFSET, and DPLL_PHASE_PULL_IN_SLOPE_LIMIT to estimate the time duration required for a frequency offset to achieve the desired phase pull-in.
v5.4.1	The accuracy of the estimated time duration is improved so that the residual phase error after a pull-in completes is reduced.

Issue Number: BRMBXR-3644

Firmware	Functional Difference
v5.3.5	When tod_frame_access_en = 1, if TOD frames are not discarded by the user, then over the course of many hours, TOD frames can accumulate in the receive FIFO.
v5.4.1	When tod_frame_access_en = 1, TOD frames cannot accumulate in the receive FIFO.

Issue Number: BRMBXR-3650

Firmware	Functional Difference
v5.3.5	When a ClockMatrix device is configured with a satellite channel it implements an auto-alignment algorithm that uses the output time-to-digital converters (TDC) to align the satellite channel output clock with the source channel output clock. The auto-alignment algorithm applies temporary frequency offsets to the satellite channel output clock to accomplish phase adjustments.
v5.4.1	The minimum duration of the temporary frequency offsets is increased from 50ms to 100ms so that the magnitude of temporary frequency offsets for small phase adjustments is reduced.

Issue Number: BRMBXR-3679

Firmware	Functional Difference
v5.3.5	When a DPLL is configured to follow the feedback clock of another DPLL, if the index of the master channel is higher than the index of the follower (e.g., DPLL0 follows DPLL1) then the follower can remain in the Freerun state for up to 10 seconds (approximately) before it begins locking to the master.
v5.4.1	A DPLL can be configured to follow the feedback clock of any other DPLL, and it will lock as expected.

Issue Number: BRMBXR-3689	
Firmware	**Functional Difference**
v5.3.5	The following applies when the DPLL_COMBO_SW_VALUE_CNFG field is set to a non-zero value. If the total FFO sent to an FOD is zero or near zero, then phase transients of up to 50 ns (approximately) can occur randomly on the FOD output clock. The total FFO means the total from all sources, including DPLL_COMBO_SW_VALUE_CNFG, the DPLL filter associated with the FOD and any source over the Combo Bus.
v5.4.1	The DPLL_COMBO_SW_VALUE_CNFG field operates as expected.

Issue Number: BRMBXR-3696	
Firmware	**Functional Difference**
v5.3.5	The FODs use divide ratios consisting of an integer part and a fractional part. In cases when the integer part is toggling, phase transients of up to 50 ns (approximately) can occur randomly on the FOD output clock.
v5.4.1	The FODs operate as expected.

5. Renesas Documentation

Issue Number	Description
BRMBXR-3617 BRMBXR-3619 BRMBXR-3628 BRMBXR-3678 BRMBXR-3680 BRMBXR-3695 BRMBXR-3697	These issues are related to Renesas documentation and interim firmware versions.

6. Register Differences Between Version 5.4.1 and Version 5.3.5

Register Module Base Address: C014h		
Offset Address (Hex)	**Individual Register Name**	**Change**
011h	GENERAL_STATUS. MIN_REL	Default value is 4.
012h	GENERAL_STATUS. HOTFIX_REL	Default value is 1.
01Ch	JTAG_DEVICE_ID	Modified register description.
01Eh	PRODUCT_ID	Modified register description.

Register Module Base Address: C03Ch		
Offset Address (Hex)	Individual Register Name	Change
022h	DPLL0_INPUT	Added selection options.
023h	DPLL1_INPUT	Added selection options.
024h	DPLL2_INPUT	Added selection options.
025h	DPLL3_INPUT	Added selection options.
026h	DPLL4_INPUT	Added selection options.
027h	DPLL5_INPUT	Added selection options.
028h	DPLL6_INPUT	Added selection options.
029h	DPLL7_INPUT	Added selection options.
02Ah	DPLL_SYS_INPUT	Added selection options.

Register Module Base Address: CB40h		
Offset Address (Hex)	Individual Register Name	Change
009h	TOD_FRAME_ACCESS_EN	Modified register description.

Register Module Base Address: CD80h		
Offset Address (Hex)	Individual Register Name	Change
000h	PWM_RX_INFO.PWM_TOD	New register.
00Ch	PWM_RX_INFO.PWM_DECODER0_ERRORS	New register.
010h	PWM_RX_INFO.PWM_DECODER1_ERRORS	New register.
014h	PWM_RX_INFO.PWM_DECODER2_ERRORS	New register.
018h	PWM_RX_INFO.PWM_DECODER3_ERRORS	New register.
01Ch	PWM_RX_INFO.PWM_DECODER4_ERRORS	New register.
020h	PWM_RX_INFO.PWM_DECODER5_ERRORS	New register.
024h	PWM_RX_INFO.PWM_DECODER6_ERRORS	New register.
028h	PWM_RX_INFO.PWM_DECODER7_ERRORS	New register.
02Ch	PWM_RX_INFO.PWM_DECODER8_ERRORS	New register.
030h	PWM_RX_INFO.PWM_DECODER9_ERRORS	New register.
034h	PWM_RX_INFO.PWM_DECODER10_ERRORS	New register.
038h	PWM_RX_INFO.PWM_DECODER11_ERRORS	New register.
03Ch	PWM_RX_INFO.PWM_DECODER12_ERRORS	New register.
040h	PWM_RX_INFO.PWM_DECODER13_ERRORS	New register.
044h	PWM_RX_INFO.PWM_DECODER14_ERRORS	New register.
048h	PWM_RX_INFO.PWM_DECODER15_ERRORS	New register.

7. Revision History

Revision	Date	Description
1.00	May 1, 2024	Initial release.