8A3xxxx Firmware Version 5.2.3

This document describes changes in the functionality and register map between firmware version 5.2.2 and version 5.2.3.

Contents

1. Overview

This optional firmware update is an OTP hotfix to address an output alignment issue. There are several related documents listed in Table 1 that describe specific functions or details that would overly burden this document.

Table 1. Related Documents

Document Title	Document Description
8A3xxxx Device Datasheet	Contains a functional overview of a specific 8A3xxxx Family device and hardware design related details including pinouts, AC and DC specifications, and applications information related to power filtering and terminations.
8A3xxxx Family Programming Guide v5.2 dated September 30, 2020	Contain detailed register descriptions and address maps for all members of the family of devices. All devices use some subset of this register map.

Table 2. Affected Devices

List of Affected Devices			
8A34005-000NLG	8A34005NLG	8A35041-000NLG	8A35041NLG
8A34005-000NLG8	8A34005NLG#	8A35041-000NLG#	8A35041NLG#
8A34005-001NLG	8A34005NLG8	8A35041-000NLG8	8A35041NLG8
8A34005-001NLG8			

2. Compatibility with EEPROMs Created for Earlier Firmware Versions

The register maps are identical in firmware version 5.2.2 and 5.2.3.

3. Firmware Version Number

The firmware version can be read from the GENERAL_STATUS registers as shown in the following table.

Register Module Base Address: C014h			Firmware Version v5.2.3
Offset Address (Hex)	**Individual Register Name**	**Register Description**	**Default Value**
010h	GENERAL_STATUS.MAJ_REL	Major release number.	0Bh
011h	GENERAL_STATUS.MIN_REL	Minor release number.	02h
012h	GENERAL_STATUS.HOTFIX_REL	Hotfix release number.	03h

4. New Features Between v5.2.2 and v5.2.3

None.

5. Changes Between v5.2.2 and v5.2.3

BRMBXR-3349
Issue
The outputs may be misaligned after the configuration is loaded by host.
Root Cause
The outputs are aligned with the master divider by more than one SCSR handlers which correspond to trigger registers OUT_DIV_MUX and OUT_DIV. In 5.2.2 it was falsely assumed that the second handler (in chronological order) does not need to rearm the alignment if it follows within a master divider cycle since the first handler was executed. This wrong assumption was causing the output divider to be misaligned with the master divider if the actual alignment (master divider rollover) occurred between the two trigger events. Further analysis and tests proved that each handler must trigger an output divider alignment with the master divider regardless of the timing between the two events. This problem may occur only after the external host loads the configuration, and it never occurs if the configuration is loaded from EEPROM or OTP.
Workaround
With 5.2.2, this problem can be avoided by restarting all DPLLs after the host loads the configuration. For example, wait for 20 milliseconds after the configuration is loaded, and then rewrite the master divider values for all DPLLs.
Solution
The old SCSR handlers which correspond to OUT_DIV_MUX and OUT_DIV are replaced by the hotfix. The new handlers always apply the output divider alignment with the master divider..

6. Notice

All updates to the firmware version noted in this release document have been described above and subsequently validated with regression testing. These updates include Features and Changes related to the new firmware, in addition this includes changes to default Register Tables. Items with descriptions labeled as “Proprietary Information” or “Reserved” are deemed as Renesas confidential material and can be discussed by contacting the Renesas Sales team.

7. Revision History

Revision	Date	Description
1.00	Aug 27, 2021	Initial release.