RS-485: Transmitting Full-Duplex Data over Single Twisted-Pair Cable

The demand for higher data throughput lead to the full-duplex RS-485 interface allowing for the simultaneous receiving and transmitting of data using two twisted-pair cable (Figure 1). To reduce cable and installation cost even further, a new type of full-duplex interface has emerged that allows data transmission over a single twisted-pair cable (Figure 2).

In this new type of full-duplex interface, each transceiver connects to the bus using a 4-to-2 wire converter that passes the transmit data from the local transceiver onto the bus, while at the same time extracting the receiving data that is sent by the remote transceiver from the bus.

The interface is purely intended for point-to-point data links, as it requires two, permanently active signal sources. Therefore, idling a signal source requires it to idle in a bus-high or bus-low state, rather than disabling the driver.

This application note explains the design of the bus node circuitry.

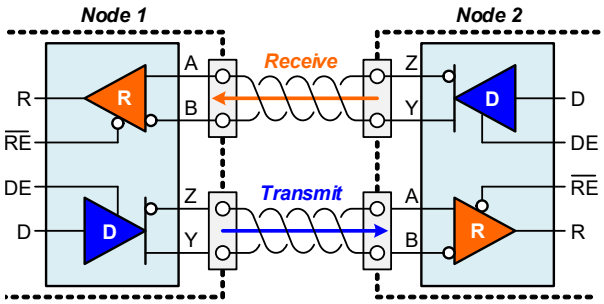

Figure 1. Traditional Full-Duplex Link with Enable Controls over Two Twisted-Pair Cables

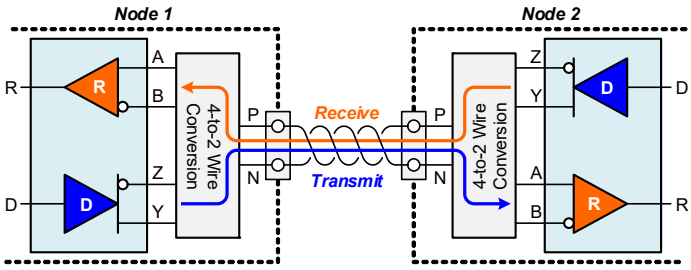

Figure 2. New permanent active Full-Duplex Link over Single Twisted-Pair Cable

Contents

1. Bus Node Circuit Design

There are three main aspects to be considered during the bus node design (Figure 3):

- **Current limiting:** As the full-duplex operation requires both transceivers to transmit and receive data at the same time, there are plenty of occasions where the signal polarities of both driver outputs are opposite to one another. This can cause large differential currents to flow, which overloads the drivers and eventually leads to thermal shutdown, a transceiver internal protection scheme required by EIA-485. Therefore, to prevent a driver from overloading, two series resistors, R_S, are placed into the driver output path that limit the current flow.
- **Bus node termination:** To minimize or even eliminate signal reflections on the bus line, the bus node impedance must match the characteristic impedance of the bus cable. This is accomplished with the termination resistor, R_T.
- **4-to-2 Wire conversion:** Resistive voltage dividers, consisting of the bus resistors, R_B, and the driver output resistors, R_D, are used to pass the local transmit data onto the bus and to extract the receive data that is sent by the remote transmitter from the bus.

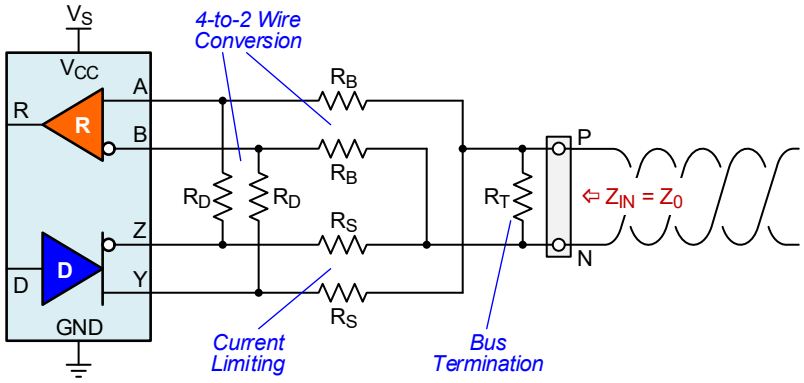

Figure 3. Three Main Aspects of the Bus Node Circuit Design

1.1 Current Limiting

To match the bus node impedance with the characteristic cable impedance, Z_0, the value of R_S should be close to half the value of Z_0:

(EQ. 1) $R_S \approx Z_0 / 2$

While it is possible to choose higher R_S values to reduce the output current, they also reduce the bus voltage, because of the voltage divider action with the termination resistor, R_T.

1.2 Bus Termination

The purpose of the termination resistor, R_T, is to adjust the input impedance of the bus node circuit such, that it matches the characteristic cable impedance: $Z_{IN} = Z_0$. As shown in Figure 4, the bus node input impedance is the parallel impedance of the termination resistor and the sum of the current limiting resistors and the driver output impedance.

(EQ. 2) $Z_{IN} = R_T \| (2R_S + R_O) = Z_0$

Before finding the value of R_T, it is necessary to establish the driver output impedance, R_O. R_O is usually not specified as a parametric value but can be derived from the V-I characteristic of the driver found in the datasheet.

Figure 5 shows a best-fit line drawn through the driver V-I characteristic curve. The slope of this line represents R_O. In this case, the output impedance of the RAA788153 transceiver is derived with $R_O \approx 25\Omega$.

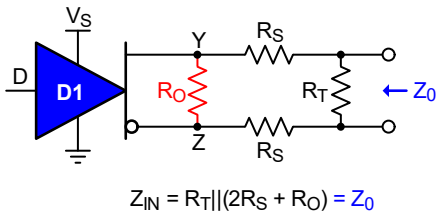

Figure 4. Bus Node Impedance Matching

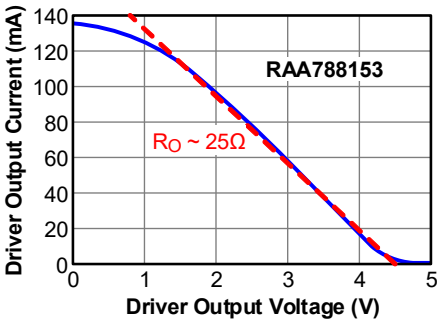

Figure 5. Deriving Driver Output Impedance

When the value of R_O is known, calculate the value of the termination resistor by solving Equation 3 for R_T:

(EQ. 3) $$R_T = \frac{(2R_S + R_O) \times Z_0}{2R_S + R_O - Z_0} = \frac{1}{1/Z_0 - 1/(2R_S + R_O)}$$

1.3 4-to-2 Wire Conversion

The 4-to-2 wire conversion not only passes transmit signals from the driver to the bus and receive signals from the bus to the receiver, but it must also cancel the portion of the transmit signal that is unavoidably looped back to the receiver (Figure 6).

Because of the design structure of the 4-to-2 wire conversion, a part of the transmit signal is looped back into the receiver path, where it is superimposed onto the receive signal. If not removed, the combined signal can cause false triggering of the receiver input thresholds, therefore, leading to data errors.

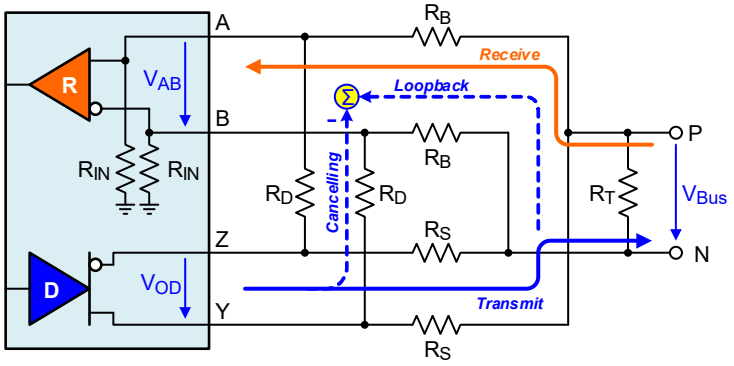

Figure 6. Deriving Driver Output Impedance

The canceling of the loopback signal is achieved by feeding an inverted portion of the transmit signal to the receiver inputs, where it adds to the loopback signal. To eliminate the loopback signal, the canceling signal must be of the same amplitude but inverted polarity as the loopback signal.

Inverting the canceling signal is accomplished by connecting the non-inverting receiver input (A) to the inverting driver output (Z), and the inverting receiver input (B) to the non-inverting driver output (Y). The amplitude of the canceling signal is set by the resistor ratio of the R_D-R_B voltage divider, which, in turn, depends on the ratio of bus voltage to driver output voltages.

1.4 Deriving the Bus Voltage to Driver Output Voltage Ratio

To determine the bus voltage, focus on the data link between the two drivers and ignore the 4-to-2 wire conversion network. This is done by ensuring that R_B and R_D are high-impedance enough to not cause any significant loading effects on the bus.

Figure 7 shows the data link with the driver output voltages V_{OD1} and V_{OD2} generating the bus voltage, V_{Bus}. Because of design symmetry, both driver output voltages are equally attenuated by the voltage diver action of $2R_S$ and R_T to generate V_{Bus}. Denoting the voltage divider gain as k, express the bus voltage using Equation 4:

(EQ. 4) $$V_{Bus} = V_{OD1} \times k + V_{OD2} \times k$$

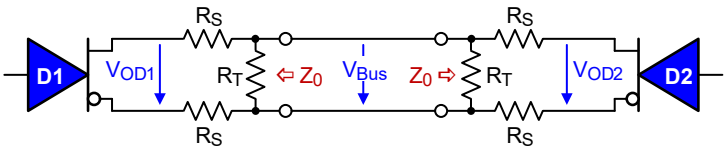

Figure 7. Design Symmetry Ensures Equal Attenuation

To determine k, convert the circuit in Figure 7 into the load circuits of both drivers (Figure 8). Because each bus node is terminated to match Z_0, the input impedance (Z_0) of one bus node is parallel to the termination resistor, R_T, of the other bus node. Therefore, each driver output sees a load resistance of $R_L = 2R_S + R_T||Z_0$.

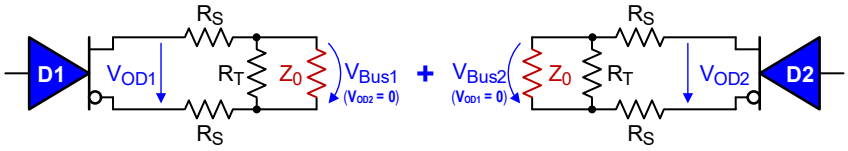

Figure 8. Each Driver has a V_{BUS} Contribution of VOD·k

From Figure 8, you can derive the gain of each bus node with:

$$k = \frac{V_{Bus1}}{V_{OD1}} = \frac{V_{Bus2}}{V_{OD2}} = \frac{R_T \| Z_0}{2R_S + R_T \| Z_0}$$

Then, multiplying out and collecting terms gives Equation 5:

(EQ. 5) $$k = \frac{1}{1 + 2R_S(1/Z_0 + 1/R_T)}$$

1.5 Deriving the R_B/R_D Ratio of the 4-to-2 Wire Conversion

From the differential 4-to-2 wire conversion network in Figure 9, construct its single-ended representation in Figure 10. Recall that V_{OD1} is inverted to $-V_{OD1}$ by the connections of the R_D resistors between the receiver inputs and the driver outputs (see also 4-to-2 Wire Conversion). To determine the R_B/R_D ratio that is necessary to prevent the local driver output (V_{OD1}) from appearing at the local receiver input (V_{AB1}) you must also include the receiver input resistance (R_{IN}) as it presents a common-mode load to the voltage divider output. R_{IN} is commonly specified in the datasheet.

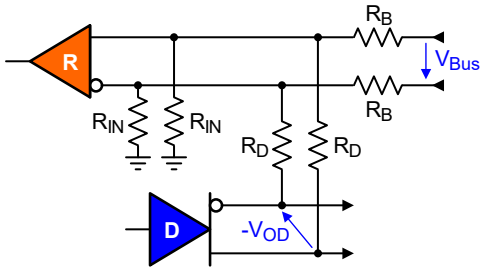

Figure 9. 2-to-4 Wire Conversion

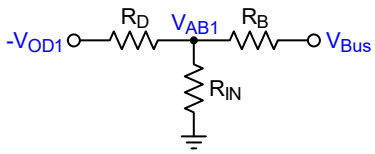

Figure 10. Single-Ended Representation

The differential receiver input voltage of Node 1, V_{AB1}, therefore, becomes:

$$V_{AB1} = V_{Bus} \times \frac{R_D \parallel R_{IN}}{R_B + R_D \parallel R_{IN}} - V_{OD1} \times \frac{R_B \parallel R_{IN}}{R_D + R_B \parallel R_{IN}}$$

Multiplying out then gives:

$$V_{AB1} = V_{Bus} \times \frac{R_D R_{IN}}{R_B R_{IN} + R_D R_{IN} + R_B R_D} - V_{OD1} \times \frac{R_B R_{IN}}{R_B R_{IN} + R_D R_{IN} + R_B R_D}$$

To arrive at an equation that includes the R_B/R_D, divide the numerators and denominators of both fractions by $R_D \times R_{IN}$:

$$V_{AB1} = V_{Bus} \times \frac{1}{1 + R_B/R_D + R_B/R_{IN}} - V_{OD1} \times \frac{R_B/R_D}{1 + R_B/R_D + R_B/R_{IN}}$$

As both fractions have the same denominators, combine both voltage terms onto one denominator:

$$V_{AB1} = \frac{V_{Bus} - V_{OD1} \times R_B/R_D}{1 + R_B/R_D + R_B/R_{IN}}$$

Now substitute V_{Bus} using Equation 4 ($V_{Bus} = V_{OD1} \times k + V_{OD2} \times k$) and get:

$$V_{AB1} = \frac{V_{OD1} \times k + V_{OD2} \times k - V_{OD1} \times R_B/R_D}{1 + R_B/R_D + R_B/R_{IN}}$$

After collecting terms, there are two separate voltage terms, one for V_{OD1} and another for V_{OD2}:

(EQ. 6) $$V_{AB1} = \frac{V_{OD1} \times (k - R_B/R_D) + V_{OD2} \times k}{1 + R_B/R_D + R_B/R_{IN}}$$

Equation 6 shows that to eliminate V_{OD1}, its bracket, k - R_B/R_D, must become zero. This is accomplished by making R_B/R_D equals k:

(EQ. 7) $$\frac{R_B}{R_D} = k$$

With the V_{OD1} component eliminated, the receiver input voltage is purely dependent of V_{OD2}:

$$V_{AB1} = \frac{V_{OD2}}{1 + \frac{1}{k} + \frac{R_D}{R_{IN}}}$$

Then, substituting k with Equation 7 gives Equation 8:

(EQ. 8) $$V_{AB1} = \frac{V_{OD2}}{1 + \frac{R_D}{R_B \| R_{IN}}} = \frac{V_{OD2}}{1 + R_D\left(\frac{1}{R_B} + \frac{1}{R_{IN}}\right)}$$

1.6 Deriving the R_B and R_D Resistor Values

Figure 11 shows that there are two leakage current paths parallel to the termination resistor. Their combined current value, I_{LK1} + I_{LK2}, should be about 10% of I_T, the current through the termination resistor, to minimize loading of the main signal path. This requires that the sum of the resistor values (R_B, R_D) is about 20 times that of the termination resistor:

(EQ. 9) $$R_B + R_D \approx 20R_T$$

At the same time, the gain requirement of Equation 7 demands that

(EQ. 10) $$R_B = R_D \times k$$

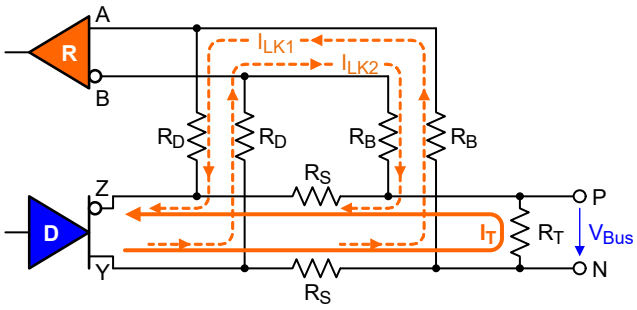

Figure 11. Leakage Currents must be ≤ 10% of Termination Current

Setting Equation 10 = Equation 9 and solving for R_D gives the first resistor value with:

$$R_D = \frac{20R_T}{k+1}$$

Substituting k with Equation 7 gives Equation 11:

(EQ. 11) $$R_D = 20 \times \{R_T \| [2(R_T + 2R_S)]\} = 20 \times \frac{R_T \times 2(R_T + 2R_S)}{R_T + 2(R_T + 2R_S)}$$

Then, applying Equation 10, calculate the resistor value for R_B:

$$R_B = R_D \times k$$

1.7 Deriving the Driver Output Voltage, V_{OD}

Knowing the magnitude of V_{OD} helps to estimate the receiver input voltage during circuit simulation. To find V_{OD}, calculate the load resistance of the driver in Figure 12 with:

(EQ. 12) $$R_L = 2R_S + R_T \| Z_0 = 2R_S + \frac{1}{1/R_T + 1/Z_0}$$

Then, drawing the R_L line into the driver V-I characteristic, V_{OD} is found at the crossing point of both curves (Figure 13).

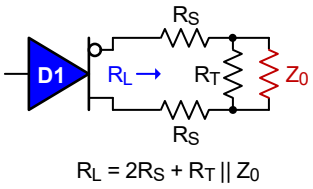

Figure 12. Driver Load Resistance

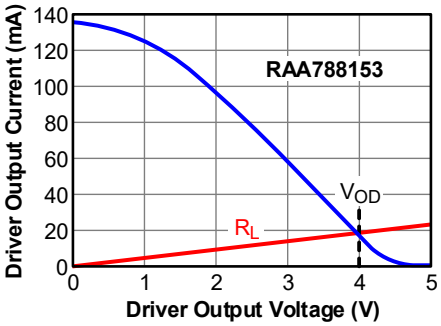

Figure 13. Deriving V_{OD} for a given R_L

2. Calculation Examples

Table 1 lists the sequence of steps for calculating the gain and resistor values for 100Ω and 120Ω Cables.

Table 1. Sequence of Calculation Steps

Parameter	Symbol	Equation / Comment		Value		Unit
Characteristic Cable Impedance	Z_0	RS-485 or CAT-5		120	100	Ω
Driver Output Impedance	R_O	Established from the driver V-I characteristic in the data sheet		25	25	Ω
Receiver Input Impedance	R_{IN}	Taken from the Electrical Specifications in the data sheet		96k	100	Ω
Current Limiting Resistor	R_S	$R_S = \frac{Z_0}{2}$	Calculated	60	50	Ω
			E-96 series	59	49.9	Ω
Termination Resistor	R_T	$R_T = \frac{1}{1/Z_0 - 1/(2R_S + R_O)}$	Calculated	746	503	Ω
			E-96 series	750	499	Ω
Forward Gain	k	$k = \frac{1}{1 + 2R_S(1/Z_0 + 1/R_T)}$		0.4671	0.455	
Driver Loopback Resistor	R_D	$R_D = 20 \times \{R_T \| [2(R_T + 2R_S)]\}$	Calculated	10.475k	7.045k	Ω
			E-96 series	10.5k	6.98k	Ω
Bus Resistor	R_B	$R_B = R_D \times k$	Calculated	4.905k	3.176k	Ω
			E-96 series	4.87k	3.16k	Ω

Table 1. Sequence of Calculation Steps (Cont.)

Parameter	Symbol	Equation / Comment	Value		Unit
Resistor Ratio	R_B/R_D		0.4638	0.4577	
Gain Error	ε	$\varepsilon = \frac{R_B/R_D}{k}$	0.71	0.49	%
Driver Load Resistance	R_L	$R_L = 2R_S + R_T \parallel Z_0$	221	183	Ω
Driver-2 Output Voltage	V_{OD2}	Established from the driver V-I characteristic in the data sheet	4.0	3.94	V
Receiver-1 Input Voltage	V_{AB1}	$V_{AB1} = \frac{V_{OD2}}{1 + R_D(1/R_B + 1/R_{IN})}$	1.23	1.20	V

3. Complete Interface Circuit and Waveforms

Figure 14 shows the complete interface circuit with a table listing the selected resistor values for bus nodes with 120Ω and 100Ω input impedance. The 1Mbps full-duplex transceivers, RAA788153, are permanently enabled by connecting the receiver enable pin, $\overline{RE}$, to ground and the driver enable pin, DE, to V_{CC}.

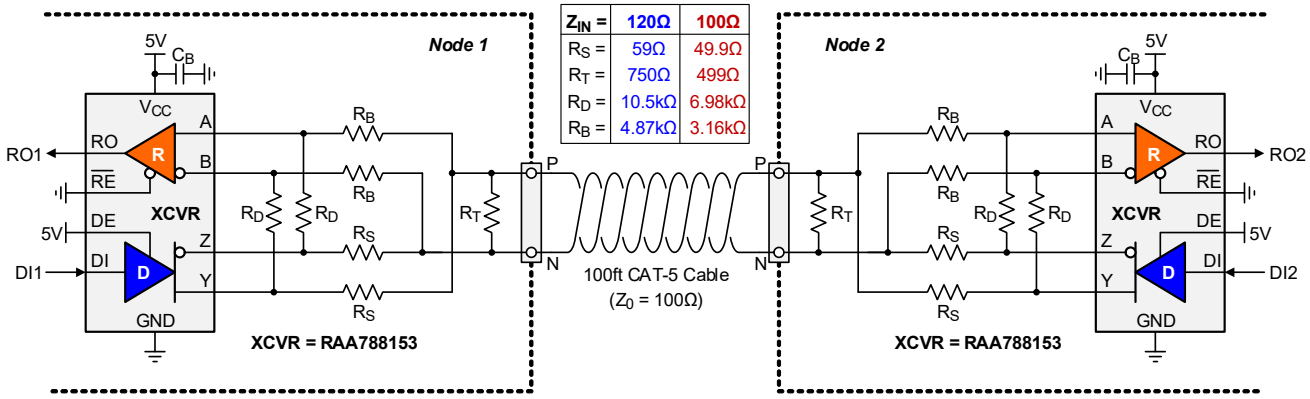

Figure 14. Complete Interface Circuit

Figure 15 and Figure 16 depict the input and output waveforms. Applying a 100kHz (200kbps) square wave to the data input pin of Node 1, DI1, results in a slightly delayed output of the same data rate at the receiver output of Node 2, RO2. In the opposite direction, applying a 400kHz (800kbps) square wave to the data input pin of Node 2, DI2, results in a slightly delayed output of the same data rate at the receiver output of Node 1, RO1.

The noisy signals in Figure 15, which also show overshoot and cross-coupling, are because of the mismatch between the nodes input impedance of Z_{IN} = 120Ω and the characteristic cable impedance of Z_0 = 100Ω. The noise free signals in Figure 16 reflect the effects of impedance matching, when the bus node design is changed to an input impedance of Z_{IN} = 100Ω, therefore, matching Z_0.

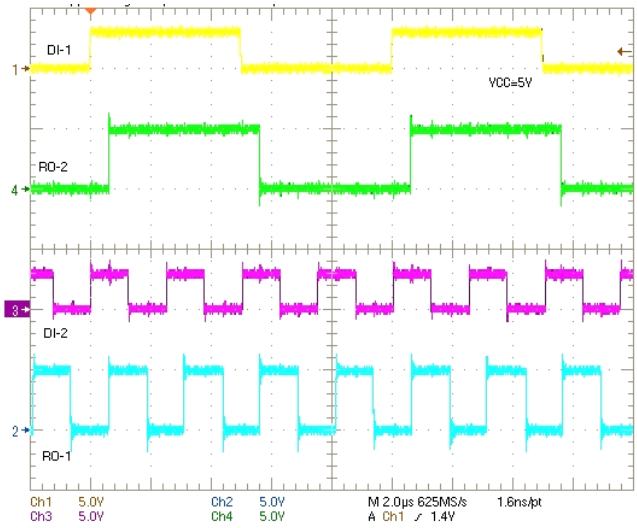

Figure 15. Bus Nodes with Z_{IN} = 120Ω Communicating Simultaneously over 100ft CAT-5 Cable (Z_0 = 100Ω)

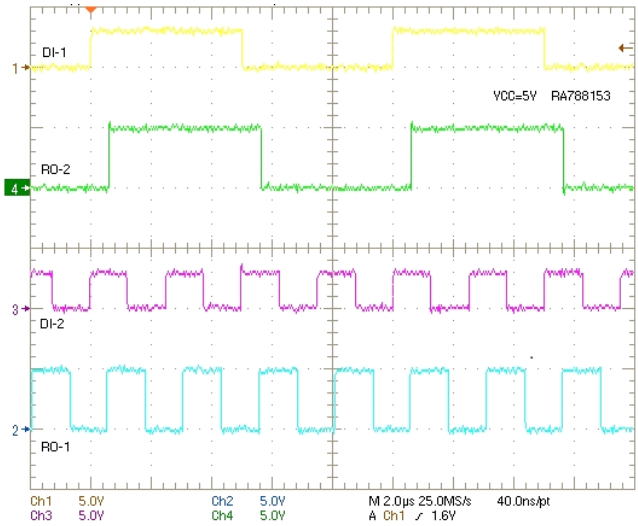

Figure 16. Bus Nodes with Z_{IN} = 100Ω Communicating Simultaneously over 100ft CAT-5 Cable (Z_0 = 100Ω)

4. Revision History

Revision	Date	Description
1.00	Mar 4, 2022	Initial release.

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