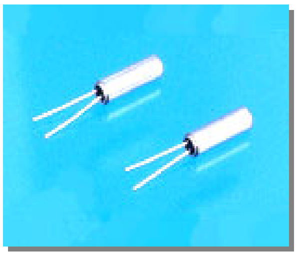
Evaluation of Subsystem Clock Oscillation Circuit

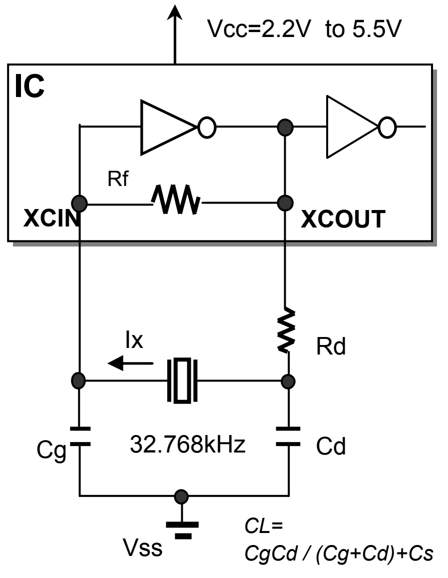
[R5F212D8SNFP-80P] LQFP(12x12) 0.5mm pitch

Measurement conditions :3.3V

SII



Model	:VT-200
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10^{6}
Load capacitance	:CL=12.5pF
Equivalent series resistance	:R1=50kohm max
Max. drive level	:DL=1x10^{-6}W max
Level of drive	:DL=0.1x10^{-6}W typ

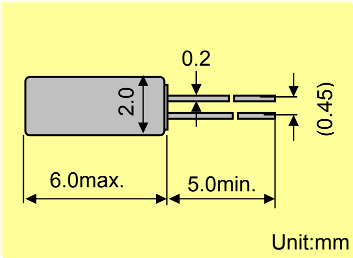


Remark) Ix : current through crystal

FEATURES

1. Compact tubular package
2. Photolithographic process
3. Excellent shock resistance and environmental characteristics.
4. Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



MODEL:VT-200 12.5pF with R5F212D8SNFP at 25°C

Key specifications	Low	High	Remarks
Negative feedback resistance : Rf (M ohm)	Built_in	Built_in	
Current control resistance : Rd (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	15	18	Optimal capacity in response to CL
Capacitance at drain : Cd (pF)	15	18	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Low	High	Remarks
Matching Accuracy : df / f (x10^{-6})	0.3	-0.4	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10^{-6})	0.2	0.2	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (x10^{-6}W)	0.13	0.12	DL=Ix^2 Re < 1x10^{-6}W,Re=R1(1 + Co / CL)^2
Negative resistance : | - RL | (kohm)	142	1132	5 times larger than R_{1MAX}
Oscillation allowance : M (times)	2.8	22.6	Judgemental standard of oscillation stability
Voltage of oscillation start : Vstrat (V)	1.77	1.77	
Voltage of oscillation stop : Vstop (V)	1.74	1.74	
Oscillation start up time : Ts (sec)	1.29	0.46	Time to reach 90% of output level

Temperature characteristics of circuit		Low	High	Remarks
at -40°C	Variation : df / T (x10^{-6})	-144	-143	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)
at +85°C	Variation : df / T (x10^{-6})	-123	-123	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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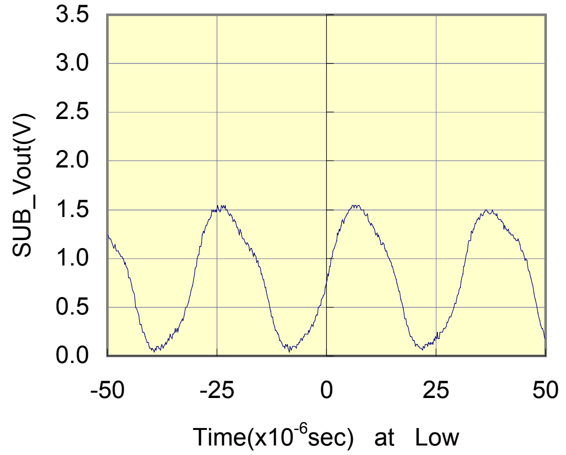
Evaluation of Subsystem Clock Oscillation Circuit

[R5F212D8SNFP-80P] LQFP(12x12) 0.5mm pitch

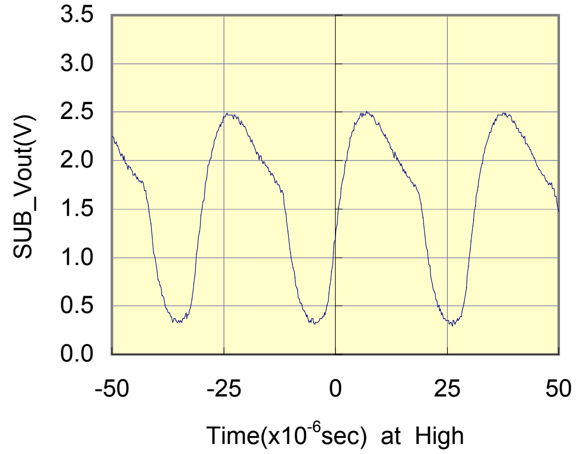
Measurement conditions :3.3V

Test Data at 25°C

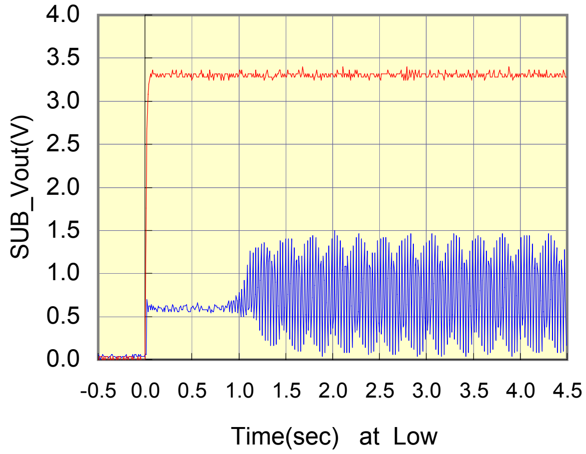
Output signal wave from the oscillator
MODEL : VT-200 12.5pF with R5F212D8SNFP



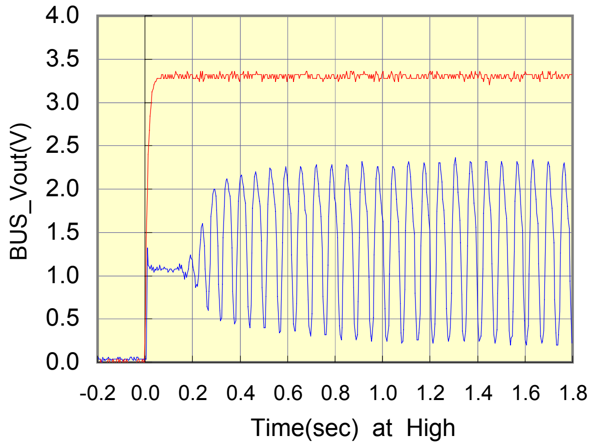
Output signal wave from the oscillator
MODEL : VT-200 12.5pF with R5F212D8SNFP



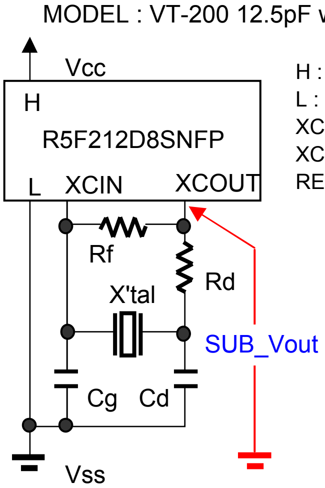
Start up time of SUB_Vout
MODEL : VT-200 12.5pF with R5F212D8SNFP



Start up time of SUB_Vout
MODEL : VT-200 12.5pF with R5F212D8SNFP



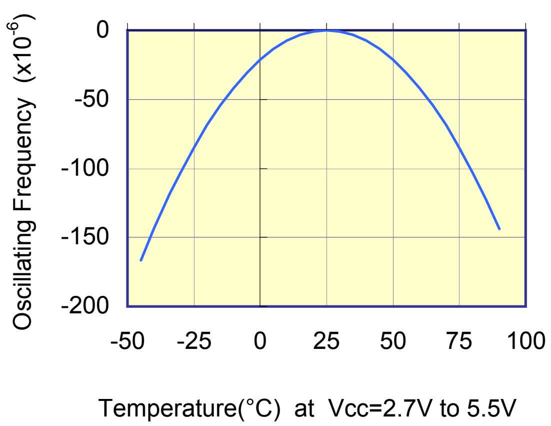
Test Circuit
MODEL : VT-200 12.5pF with R5F212D8SNFP



H : 13,78
L : 12,75
XCIN : 7
XCOUT : 8
RESET: 9

Recommended Values
X'tal :
VT-200 +/-20/12.5pF
Vcc=2.7V to 5.5V
Rf=open
Rd=0 ohm
Cg=15 to 18pF typ
Cd=15 to 18pF typ
Ta=-40 to 85°C

Temperature characteristics of oscillating frequency
MODEL : VT-200 12.5pF with R5F212D8SNFP



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[R5F212D8SNFP-80P] LQFP(12x12) 0.5mm pitch

Measurement conditions :3.3V

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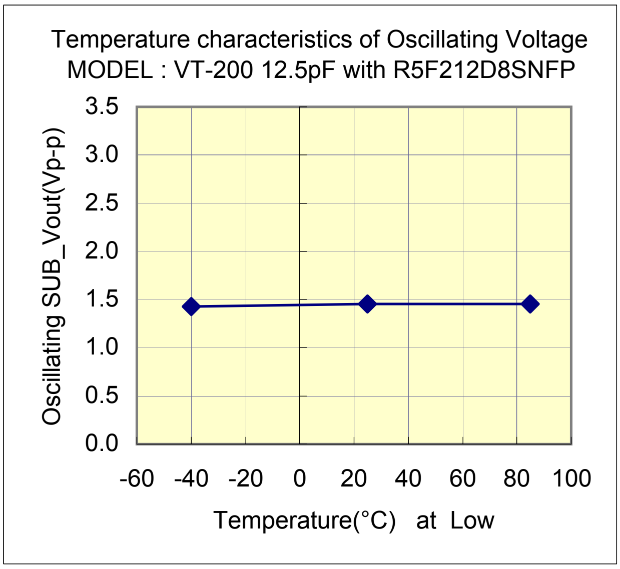
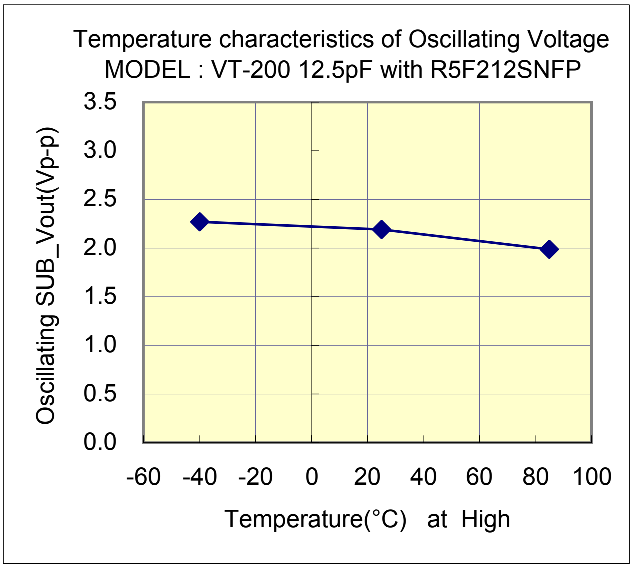
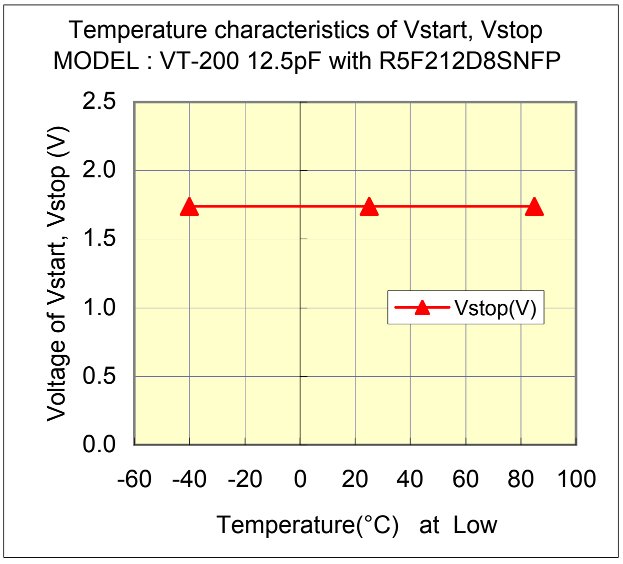
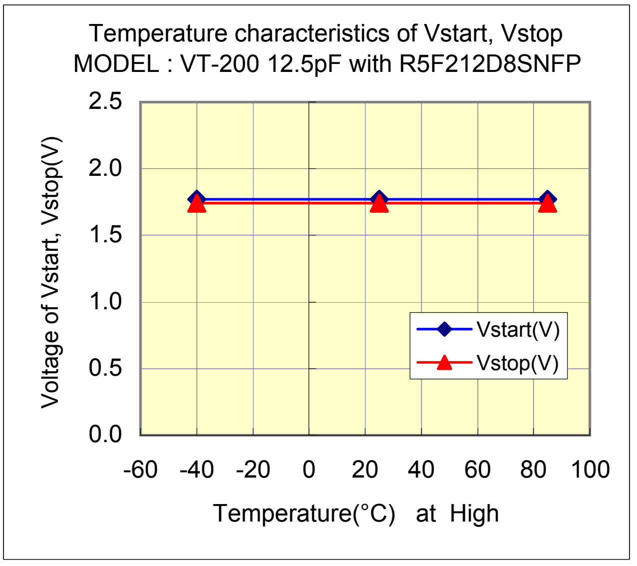
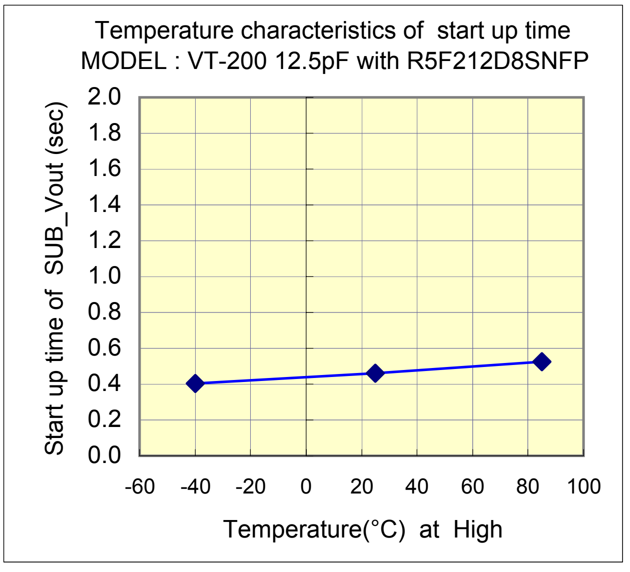
Test Data : Temperature characteristics











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Evaluation of Subsystem Clock Oscillation Circuit

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Measurement conditions :3.3V

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Referenicial components layout(see Figure 1)

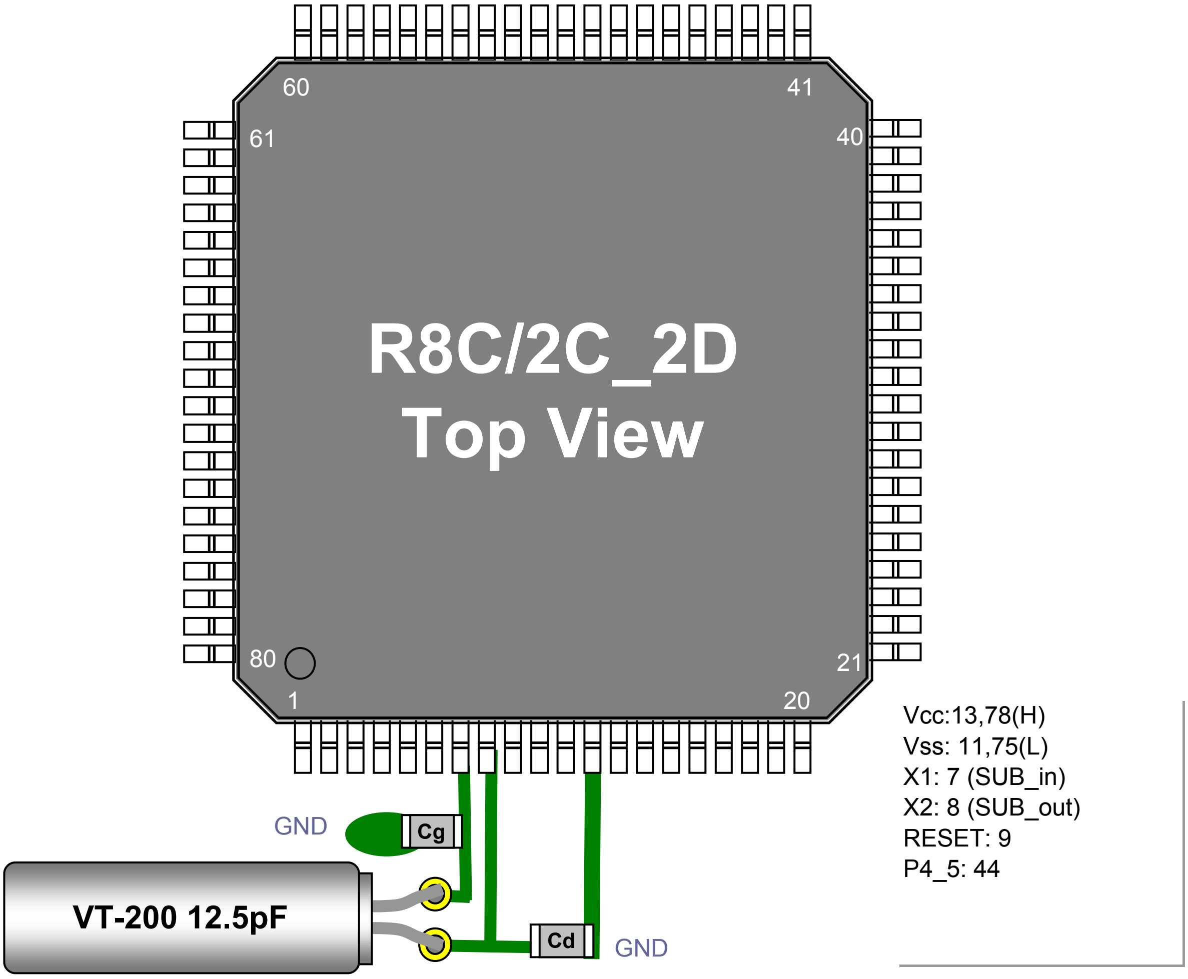


Figure 1 Referenicial components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.
Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

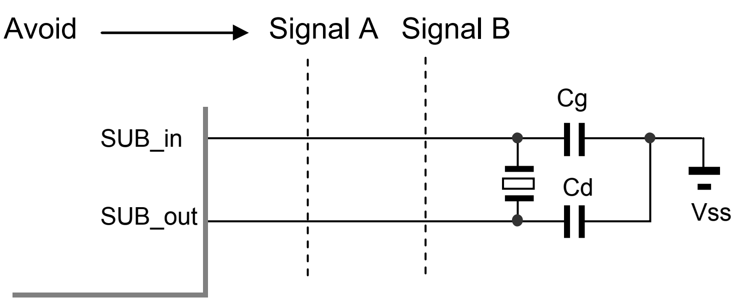


Figure 2 Example of Incorrect Board Design

Evaluation of Subsystem Clock Oscillation Circuit

[R5F212D8SNFP-80P] LQFP(12x12) 0.5mm pitch

Measurement conditions :3.3V

[Evaluation Sample : VT-200 12.5pF at 25°C]

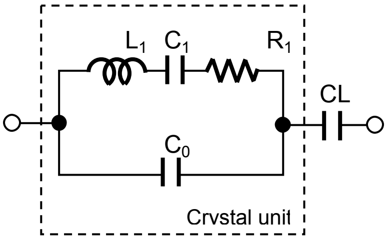
SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
VT-200 12.5pF	1	12.5	32768.30	32765.60	27.8	0.90	2.208	79.2
	2	12.5	32768.09	32765.24	26.9	0.89	2.333	77.4
	3	12.5	32768.34	32765.45	29.9	0.93	2.368	68.6

[IC Test Data : IC samples Rd=0 ohm,Cg=15 to 18pF,Cd=15 to 18pF at 25°C]

MODE	IC samples	Fosc(Hz)	df / f(x10^{-6})	DL(x10^{-6}W)	| -RL |(kohm)	Vstart(V)	Ts(sec)
High	TYP	32768.287	-0.40	0.12	1132	1.77	0.46
	HH	32768.270	-0.92	0.12	1232	1.77	0.43
	HL	32768.330	0.92	0.12	1232	1.70	0.43
	LH	32768.280	-0.61	0.12	1132	1.68	0.45
	LL	32768.279	-0.64	0.11	1132	1.72	0.43
Low	TYP	32768.310	0.31	0.13	142	1.77	1.29
	HH	32768.277	-0.70	0.14	132	1.77	1.20
	HL	32768.340	1.22	0.14	362	1.70	0.65
	LH	32768.280	-0.61	0.12	114	1.68	1.29
	LL	32768.300	0.00	0.11	212	1.72	1.10

Remark (see figure 3)

Fo = fr ×{ C1/ (2×(Co + CL)) + 1 } (Hz)



Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

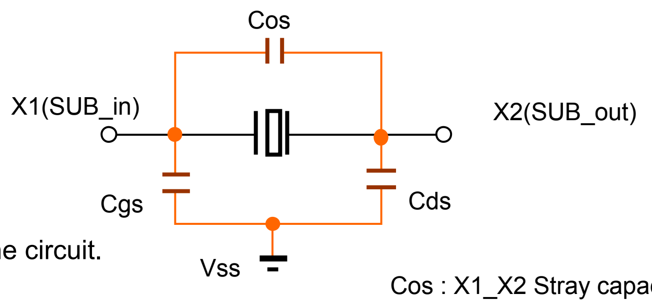
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

CL = Cg×Cd / (Cg + Cd) + Cs (pF)

Where Cs(=2 to 4pF) Stands for stray capacity of the circuit.



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

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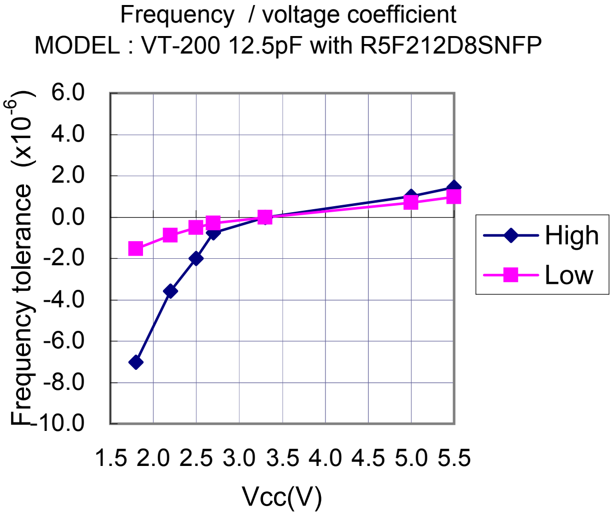
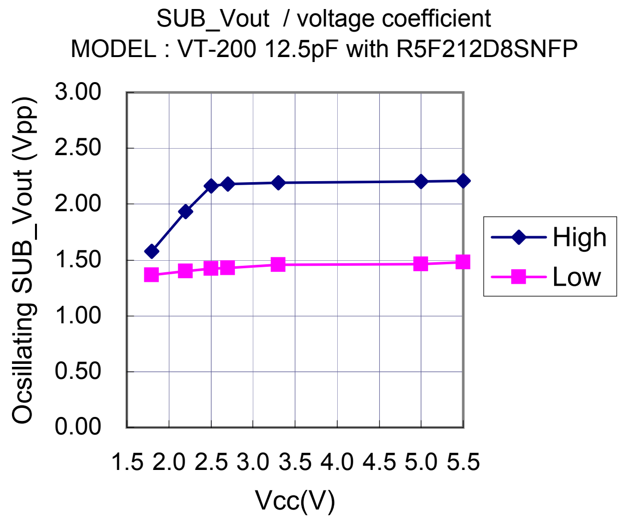
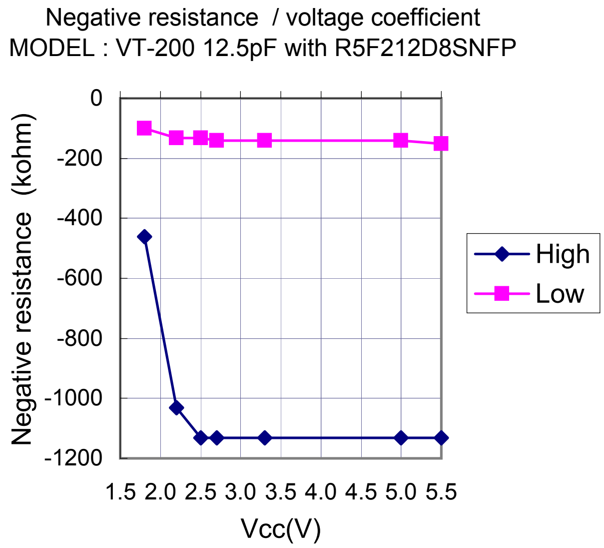
[R5F212D8SNFP-80P] LQFP(12x12) 0.5mm pitch

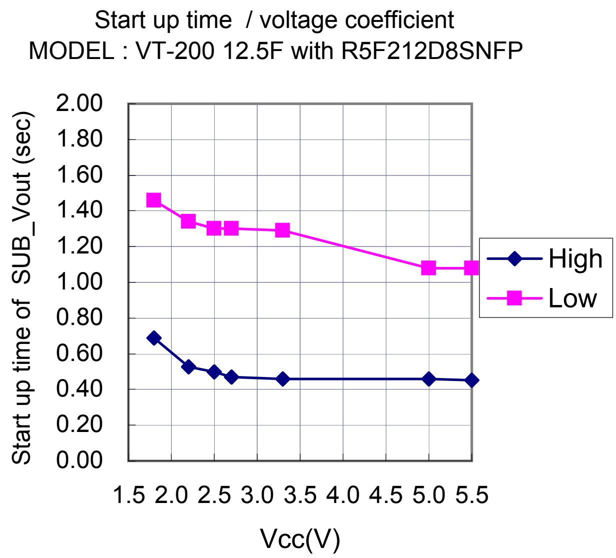
Measurement conditions : Vdd=1.8V to 5.5V at 25°C

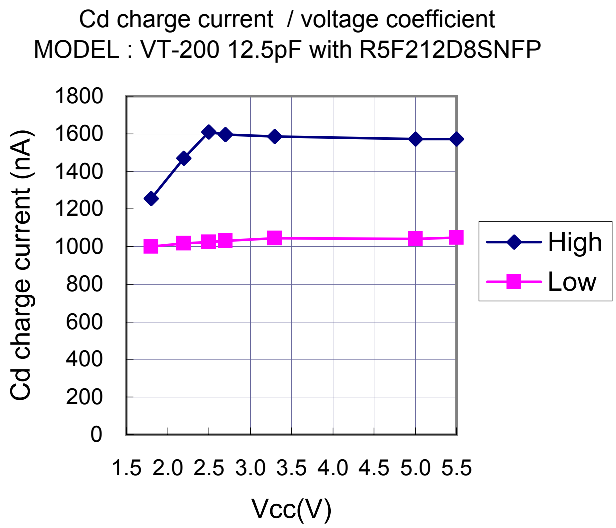
Referential Data : Voltage characteristics











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