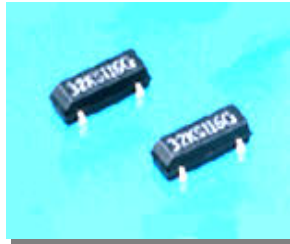


# Evaluation of Subsystem Clock Oscillation Circuit

[R5F212D8SNFP-80P] LQFP(12x12) 0.5mm pitch  
 Measurement conditions :3.3V

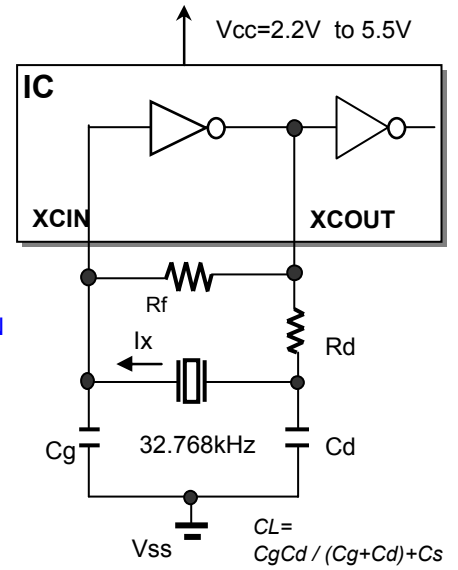
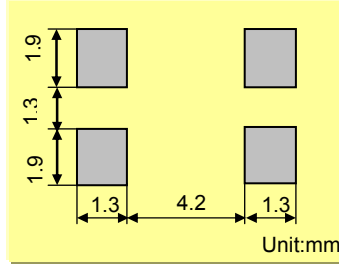


Model :SP-T2A  
 Frequency :Fo=32.768kHz  
 Frequency tolerance :dF/Fo= +/-20x10<sup>6</sup>  
 Load capacitance :CL=6.0pF  
 Equivalent series resistance :R1=50k ohm max  
 Max. Drive level :DL=1x10<sup>6</sup>W max  
 Recommended drive level :DL=0.1x10<sup>6</sup>W typ

## FEATURES

1. Plastic mold package incorporated tubular type quartz crystal.
2. Suitable for automatic and high density surface mounting.
3. Excellent shock and heat resistance
4. Real time clocks, Timers, Portable applications, Clock source for Micro-Computers

## RECOMMENDED SOLDERING PATTERN



Remark) Ix : current through crystal

MODEL:SP-T2A 6.0pF with R5F212D8SNFP at 25°C

Key specifications	Low	High	Remarks
Negative feedback resistance : Rf ( M ohm )	Built_in	Built_in	
Current control resistance : Rd ( k ohm )	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg ( pF )	1	6	Optimal capacity in response to CL
Capacitance at drain : Cd ( pF )	0	6	( CL = Cd // Cg + stray capacitance )

Circuit characteristics ( at 25°C )	Low	High	Remarks
Matching Accuracy : df / f ( x10 <sup>-6</sup> )	0.9	-0.9	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V ( x10 <sup>-6</sup> )	0.6	2.4	Vdd +/-10% ( Standard operating voltage range )
Drive Level : DL ( x10 <sup>-6</sup> W )	0.01	0.01	DL=Ix <sup>2</sup> Re < 1x10 <sup>-6</sup> W, Re=R1( 1 + Co / CL ) <sup>2</sup>
Negative resistance :   - RL   ( kohm )	597	717	5 times larger than R <sub>1MAX</sub>
Oscillation allowance : M ( times )	11.9	14.3	Judgemental standard of oscillation stability
Voltage of oscillation start : Vstart ( V )	1.77	1.77	
Voltage of oscillation stop : Vstop ( V )	1.74	1.74	
Oscillation start up time : Ts ( sec )	0.52	0.71	Time to reach 90% of output level

Temperature characteristics of circuit		Low	High	Remarks
at -40°C	Variation : df / T ( x10 <sup>-6</sup> )	-142	-143	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )
at +85°C	Variation : df / T ( x10 <sup>-6</sup> )	-123	-123	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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We value the "takumi" spirit.

Seiko Instruments Inc.  
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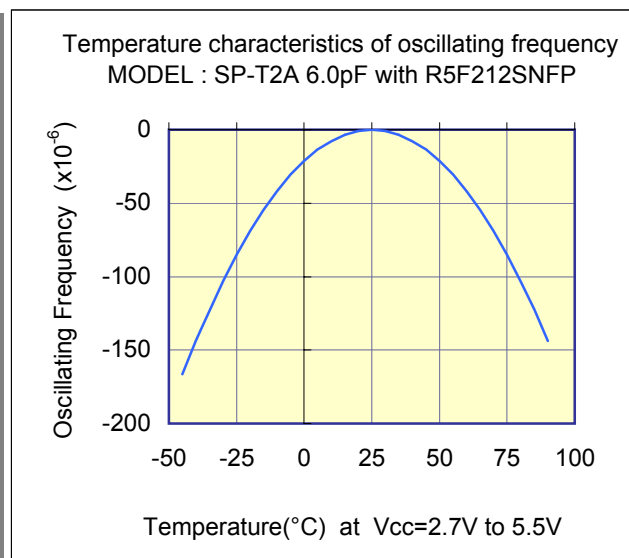
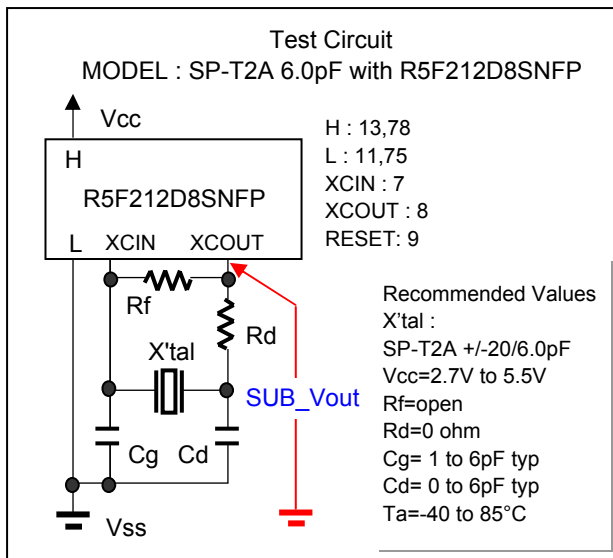
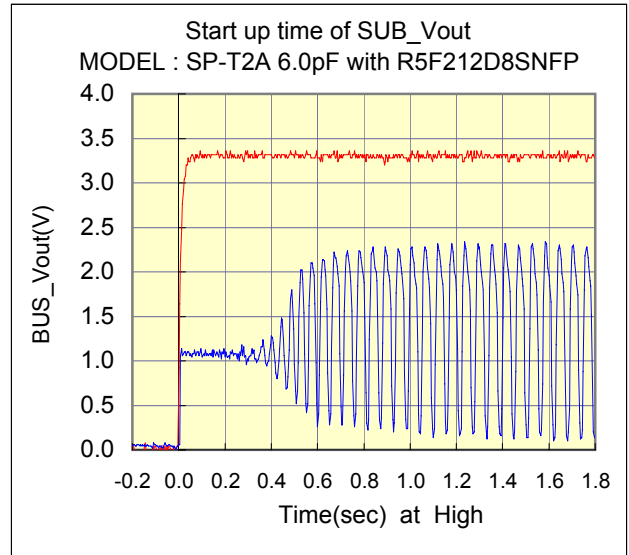
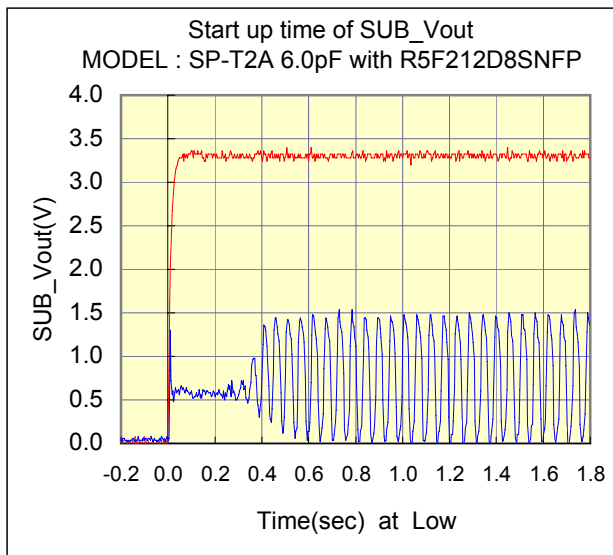
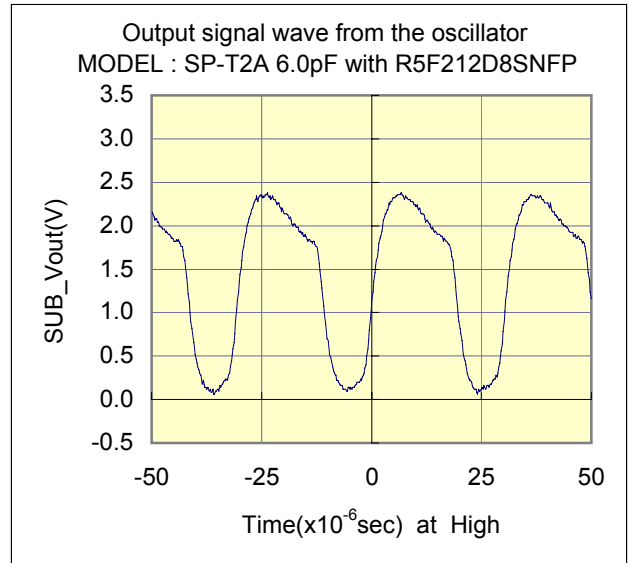
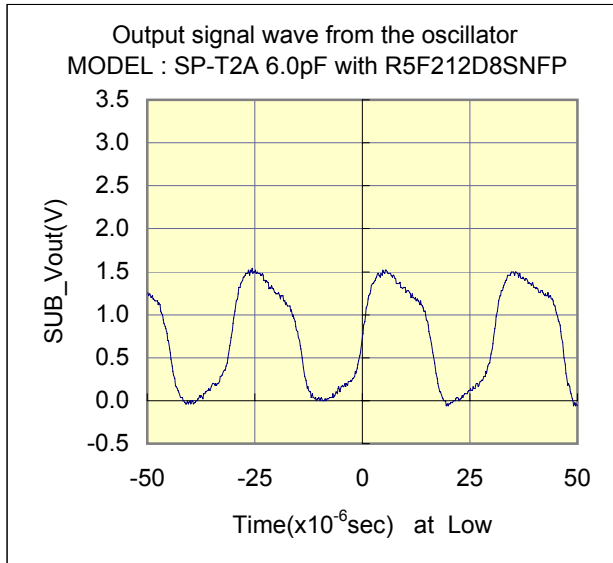
# Evaluation of Subsystem Clock Oscillation Circuit

[R5F212D8SNFP] LQFP(12x12) 0.5mm pitch

Measurement conditions :3.3V



## Test Data at 25°C



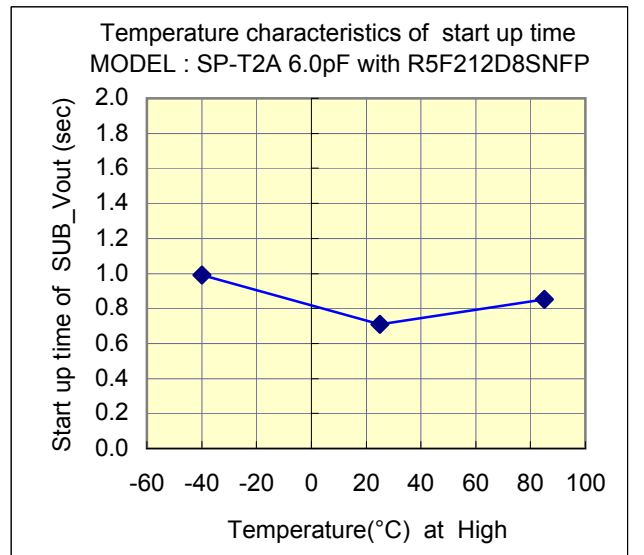
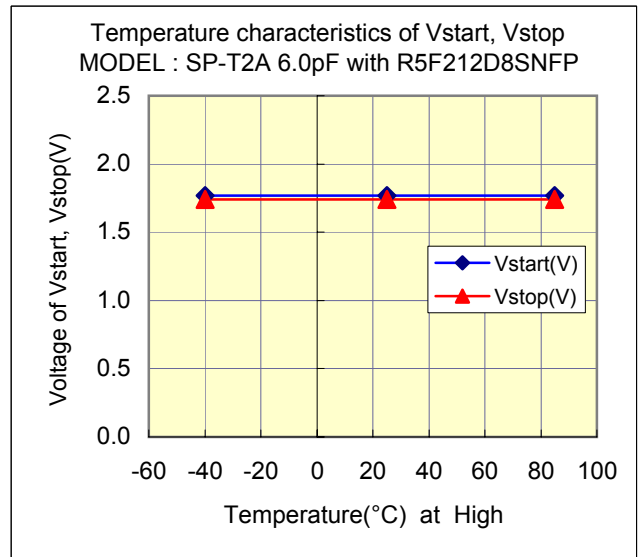
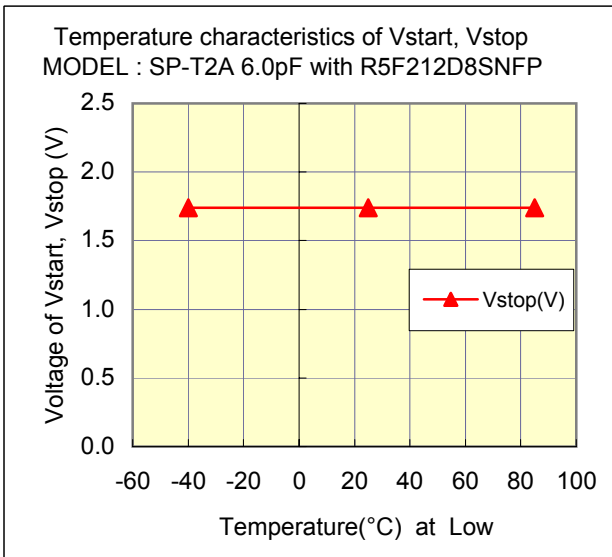
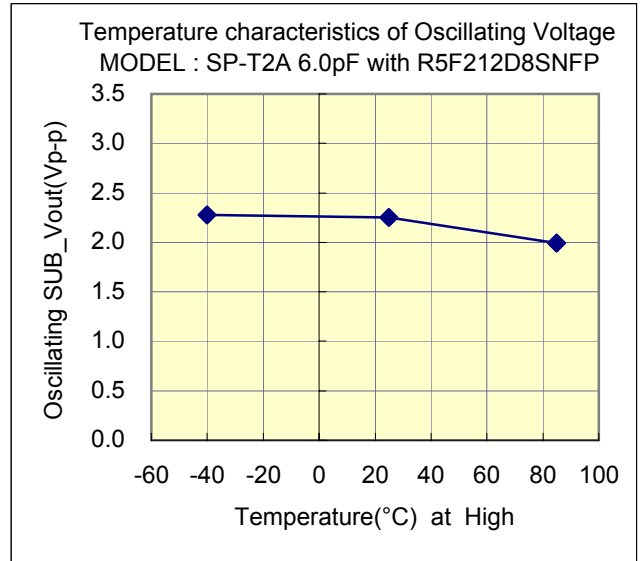
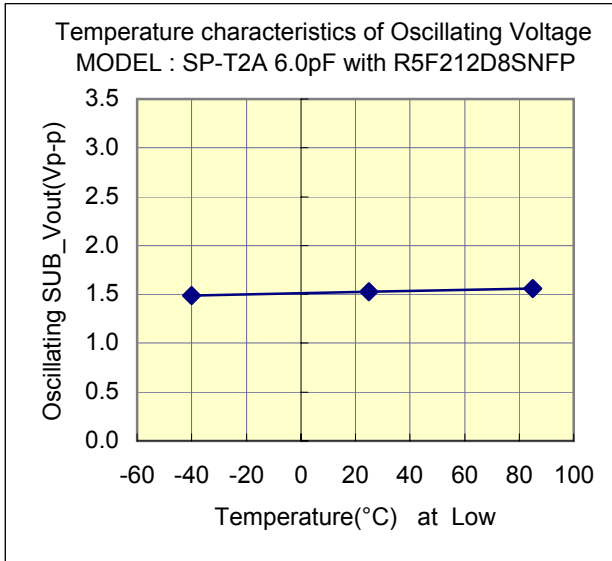
# Evaluation of Subsystem Clock Oscillation Circuit

[R5F212D8SNFP] LQFP(12x12) 0.5mm pitch

Measurement conditions :3.3V



## Test Data : Temperature characteristics



# Evaluation of Subsystem Clock Oscillation Circuit

[R5F212D8SNFP-80P] LQFP(12x12) 0.5mm pitch

Measurement conditions :3.3V



## Referential components layout(see Figure 1)

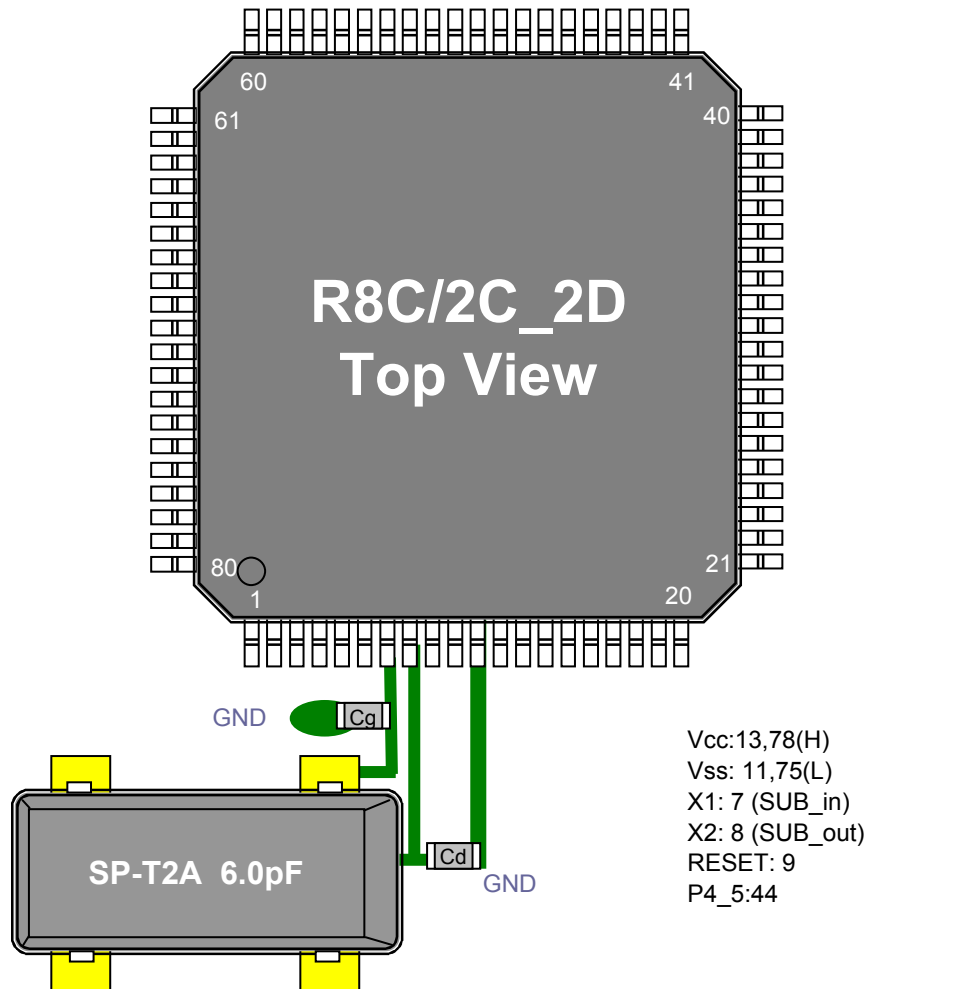


Figure 1 Referential components layout

## Notes for Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB\_in and SUB\_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

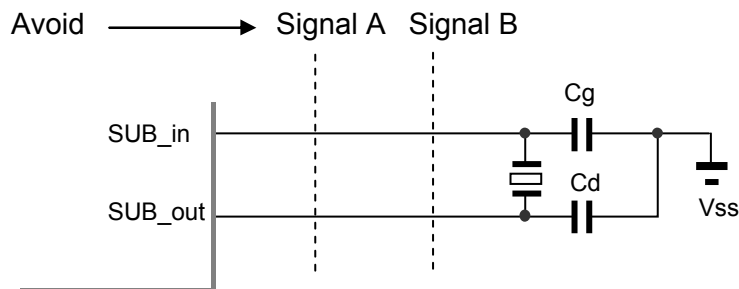


Figure 2 Example of Incorrect Board Design

# Evaluation of Subsystem Clock Oscillation Circuit

[R5F212D8SNFP-80P] LQFP(12x12) 0.5mm pitch

Measurement conditions :3.3V



## [Evaluation Sample : SP-T2A 6.0pF at 25°C]

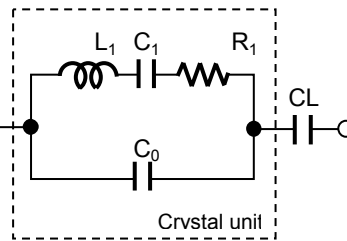
SAMPLE	No.	CL( pF )	Fo( Hz )	fr( Hz )	R1( kohm )	Co( pF )	C1( fF )	Q( k )
SP-T2A 6.0pF	1	6	32768.09	32762.69	27.3	1.02	2.314	76.9
	2	6	32767.76	32762.20	30.4	1.00	2.377	67.3
	3	6	32768.27	32762.68	31.5	1.02	2.394	64.4

## [IC Test Data : IC samples Rd=0 ohm,Cg=1 to 6pF,Cd=0 to 6pF at 25°C]

MODE	IC samples	Fosc( Hz )	df / f( x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm )	Vstart( V )	Ts(sec)
High	TYP	32768.060	-0.92	0.01	717	1.77	0.71
	HH	32768.330	7.32	0.01	717	1.77	0.99
	HL	32768.300	6.41	0.01	597	1.70	0.99
	LH	32767.307	-23.90	0.01	857	1.70	0.79
	LL	32768.093	0.09	0.01	787	1.72	0.80
Low	TYP	32768.120	0.92	0.01	597	1.77	0.52
	HH	32768.178	2.69	0.01	597	1.77	0.57
	HL	32768.350	7.93	0.01	947	1.70	0.56
	LH	32768.115	0.76	0.01	507	1.70	0.57
	LL	32768.191	3.08	0.01	857	1.72	0.56

### Remark ( see figure 3 )

$$F_o = f_r \times \{ C_1 / ( 2 \times ( C_o + C_L ) ) + 1 \} \text{ ( Hz )}$$



- Fo : Load resonance frequency
- fr : Resonance frequency
- R1 : Motional resistance
- C1 : Motional capacitance
- Co : Shunt capacitance
- CL : Load Capacitance

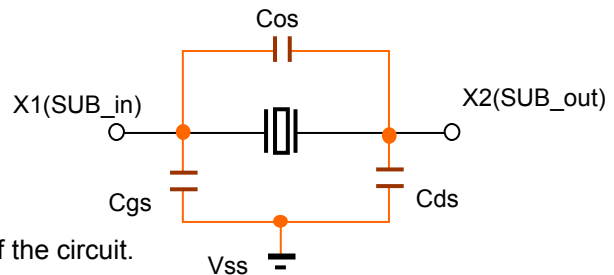
Figure 3 Equivalent circuit of crystal unit, and CL

### Remark ( see figure 4 )

Approximate formula of the load capacitance of the circuit CL.

$$C_L = C_g \times C_d / ( C_g + C_d ) + C_s \text{ ( pF )}$$

Where Cs(=2 to 4pF) Stands for stray capacitance of the circuit.



- Cos : X1\_X2 Stray capacitance
- Cgs : X1\_Vss Stray capacitance
- Cds : X2\_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

# Evaluation of Subsystem Clock Oscillation Circuit

[R5F212D8SNFP] LQFP(12x12) 0.5mm pitch

Measurement conditions : V<sub>dd</sub>=1.8V to 5.5V at 25°C

## Referential Data : Voltage characteristics

