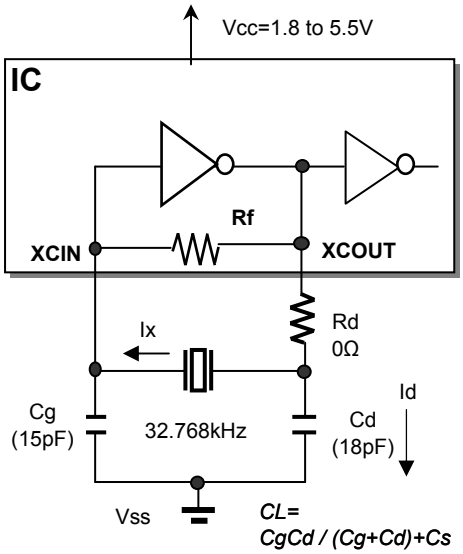
Evaluation of a Low Frequency Clock Oscillation Circuit

SSP-T7-F 12.5pF with R5F2LA88ANFP-80P [LQFP(12x12) 0.50mm pitch]

Measurement conditions : 3.3V ,5.0V

Super low power consumption MCU

Model	:SSP-T7-F
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10^{-6}
Load capacitance	:CL=12.5pF
Equivalent series resistance	:R1=65kΩ max
Max. drive level	:DL=1μW max
Level of drive	:DL=0.1μW typ

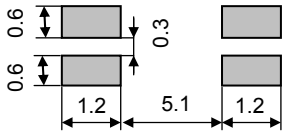


Remark) Ix : current through crystal

FEATURES

1.Ultra thin type with 1.4mm Max.
2.SMD type suitable for automatic & high density surface mounting.
3.Plastic mold package containing highly reliable tubular type quartz crystal.
4.Excellent shock and heat resistance.
5.Cellular phones,PDA,Radio communication equipment, Portable applications etc.

RECOMMENDED SOLDERING PATTERN



Unit:mm

MODEL:SSP-T7-F 12.5pF with R5F2LA88ANFP at 25°C

Key specifications	Vcc=3.3V	Vcc=5.0V	Remarks
Current control resistance : Rd (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	15	15	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	18	18	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vcc=3.3V	Vcc=5.0V	Remarks
Matching Accuracy : df / f (x10^{-6})	4.9	5.5	Frequency offset volume at specified Vcc
Voltage Fluctuation : +/-df / V (x10^{-6})	0.2	0.4	Vcc +/-10% (Standard operating voltage range)
Drive Level : DL (μW)	0.07	0.10	DL=Ix^2 Re < 1x10^{-6}W,Re=R1(1 + Co / CL)^2
Negative resistance : | - RL | (kΩ)	392	442	5 times larger than R_{1MAX}
Oscillation allowance : M (times)	6	7	Judgmental standard of oscillation stability
Current consumption : Id (μA)	0.518	0.605	Cd charge current, Id = f*Cd*Vd
Voltage of oscillation start : Vstart (V)	1.13	1.13	
Voltage of oscillation stop : Vstop (V)	1.10	1.10	
Oscillation start up time : Ts (sec)	1.34	1.19	Time to reach 90% of output level, Ts < 1.5sec

Temperature characteristics of circuit		Vcc=3.3V	Vcc=5.0V	Remarks
at -40°C	Variation : df / T (x10^{-6})	-141	-141	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)
at +85°C	Variation : df / T (x10^{-6})	-129	-129	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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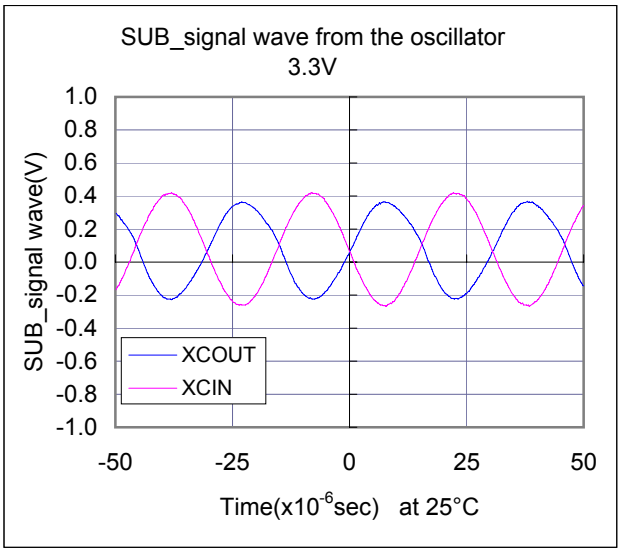
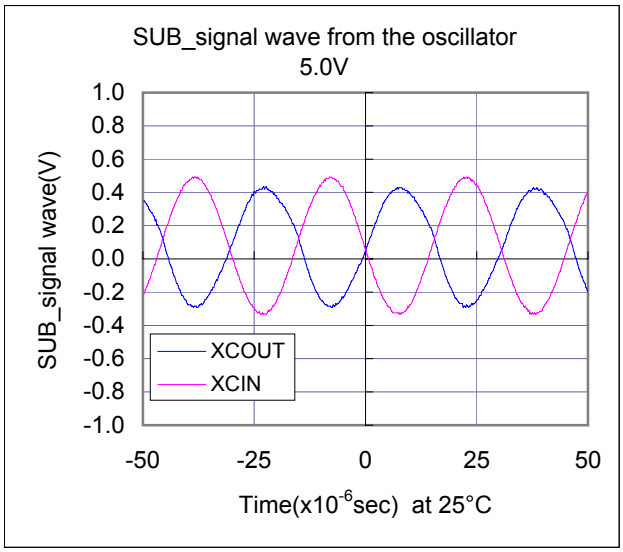
Evaluation of a Low Frequency Clock Oscillation Circuit

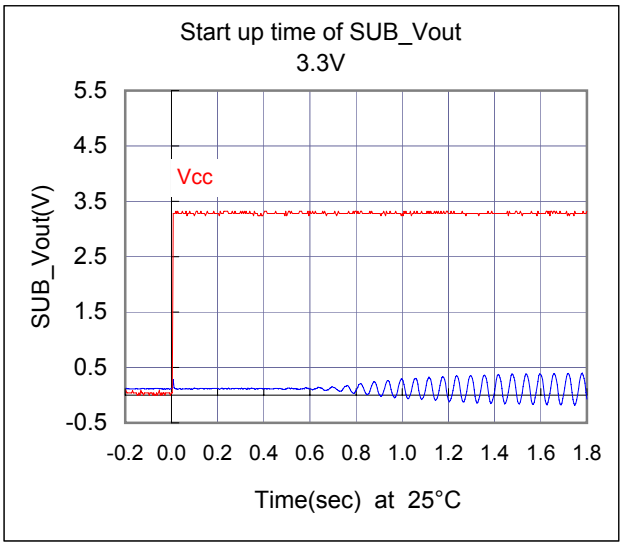
SSP-T7-F 12.5pF with R5F2LA88ANFP-80P [LQFP(12x12) 0.50mm pitch]

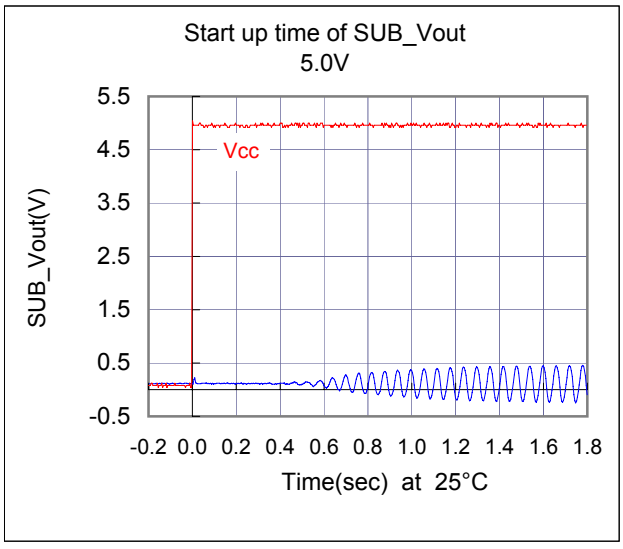
Measurement conditions : 3.3V ,5.0V

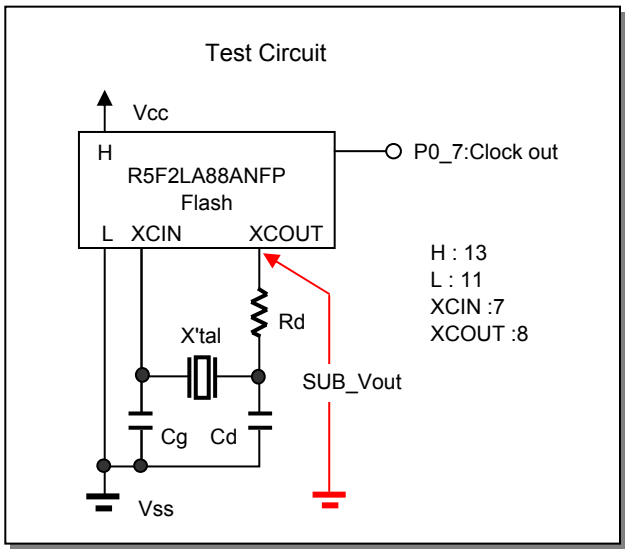
Test Data

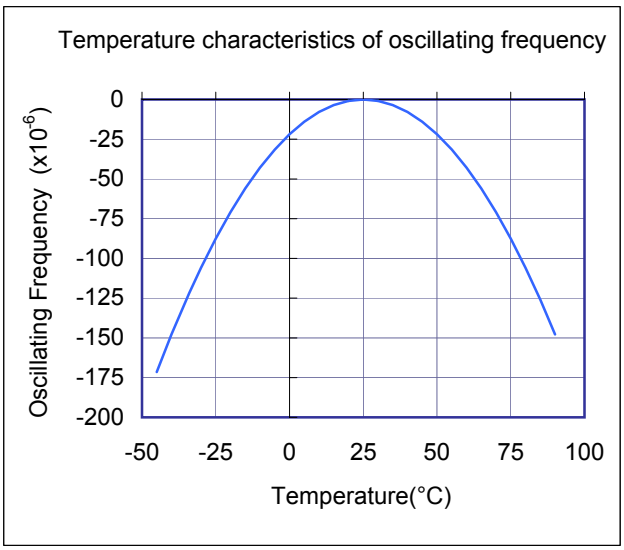










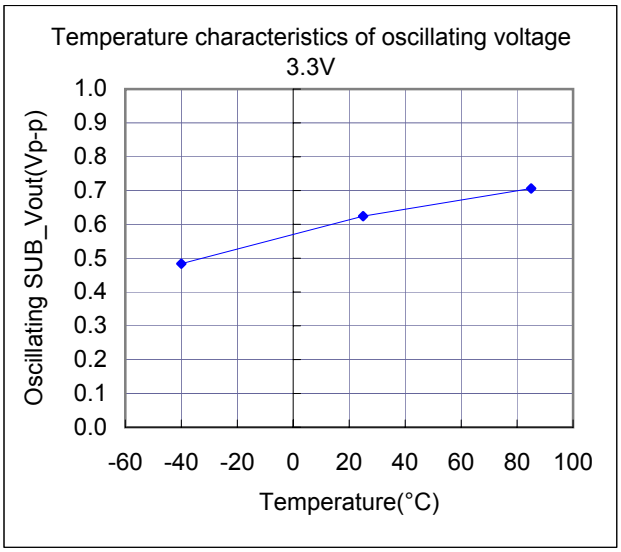


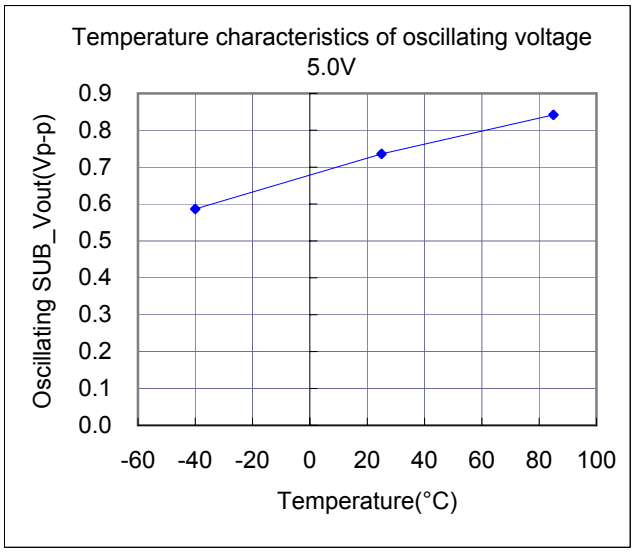
Evaluation of a Low Frequency Clock Oscillation Circuit

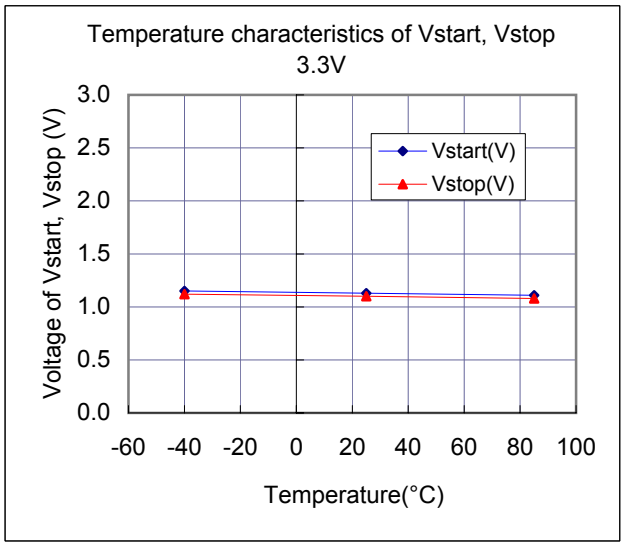
SSP-T7-F 12.5pF with R5F2LA88ANFP-80P [LQFP(12x12) 0.50mm pitch]

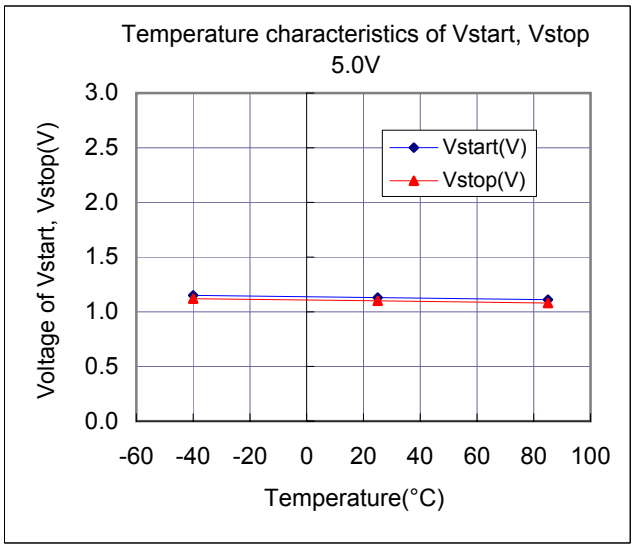
Measurement conditions : 3.3V ,5.0V

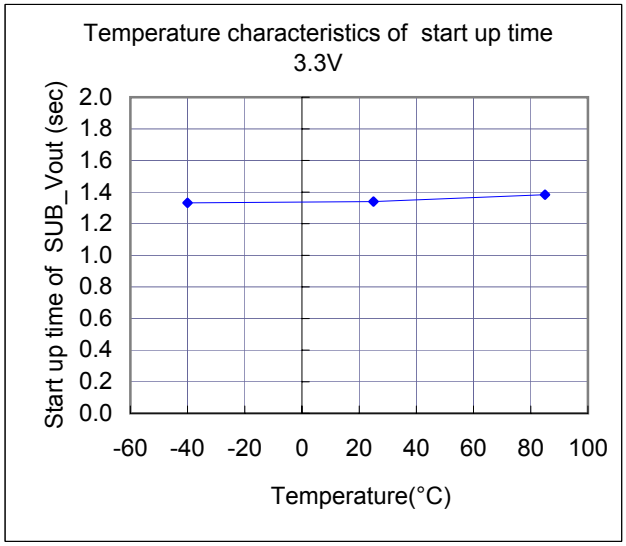
Test Data : Temperature characteristics

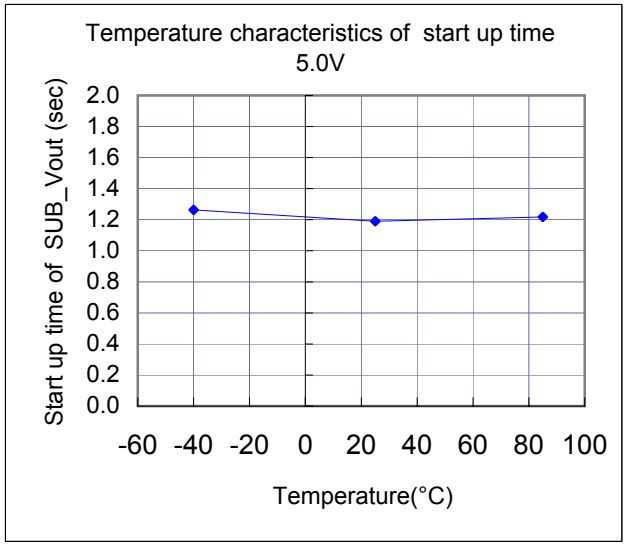




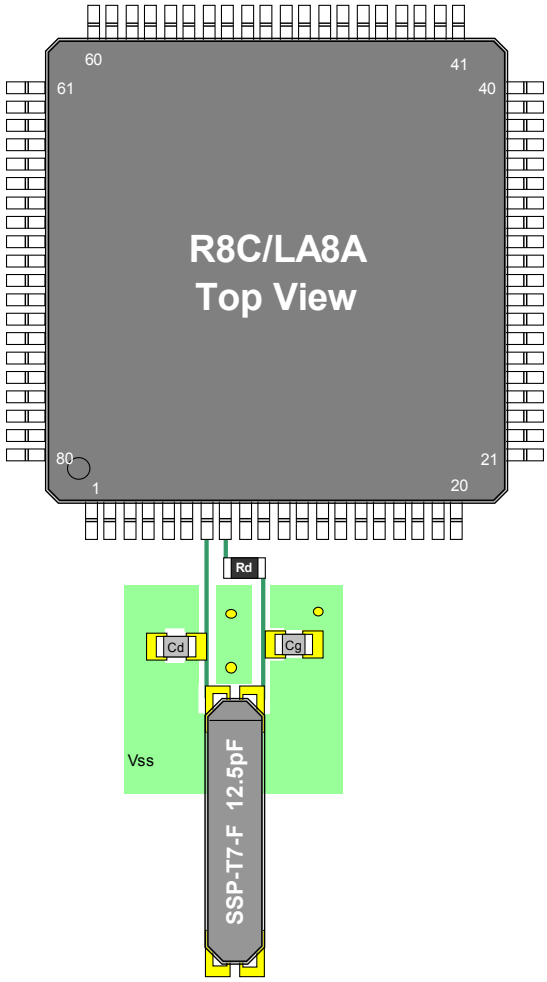








Referential components layout(see Figure 1)



R8C/Lx series

R8C/LAxA group
R8C/LA3A-32P
R8C/LA5A-52P
R8C/LA6A-64P
R8C/LA8A-80P

Figure 1 Referential components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.
Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

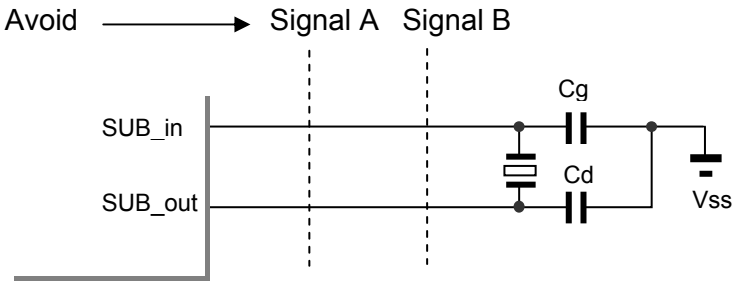


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert a resistor, Rd, in series on the SUB_out side.

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SSP-T7-F 12.5pF with R5F2LA88ANFP-80P [LQFP(12x12) 0.50mm pitch]

Measurement conditions : 3.3V ,5.0V

[Evaluation Sample at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kΩ)	Co(pF)	C1(fF)	Q(k)
SSP-T7-F	1	12.5	32768.02	32765.44	42.3	0.89	2.108	54.5
	2	12.5	32768.04	32765.45	35.8	0.89	2.116	64.1
	3	12.5	32768.00	32765.40	36.9	0.89	2.125	62.0

[IC Test Data : IC Sample Rd=0Ω,Cg=15pF,Cd=18pF at 25°C]

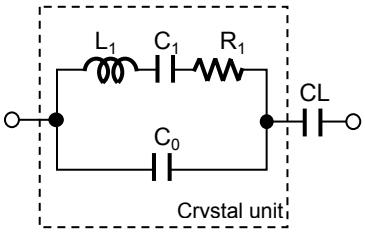
Vcc(V)	IC Sample	Fosc(Hz)	df / f(x10^{-6})	DL(μW)	| -RL |(kΩ)	Id (μA)	DC_Bias(V)	Vstart(V)	Ts(sec)
5.0	CC	32768.18	5.49	0.10	442	0.605	1.08	1.13	1.19
	HH	32768.17	5.10	0.07	372	0.498	1.10	1.14	1.31
	HL	32768.20	5.98	0.06	372	0.476	1.15	1.27	1.30
	LH	32768.19	5.71	0.09	432	0.589	1.09	1.12	1.28
	LL	32768.20	6.10	0.12	472	0.689	1.10	1.13	1.06
	AVG.	32768.19	5.68	0.09	418	0.571	1.10	1.16	1.23

[IC Test Data : IC Sample Rd=0Ω,Cg=15pF,Cd=18pF at 25°C]

Vcc(V)	IC Sample	Fosc(Hz)	df / f(x10^{-6})	DL(μW)	| -RL |(kΩ)	Id (μA)	DC_Bias(V)	Vstart(V)	Ts(sec)
3.3	CC	32768.16	4.88	0.07	392	0.518	1.08	1.13	1.34
	HH	32768.15	4.58	0.05	312	0.415	1.10	1.14	1.57
	HL	32768.18	5.37	0.05	312	0.409	1.15	1.27	1.44
	LH	32768.16	5.00	0.06	372	0.487	1.09	1.12	1.43
	LL	32768.18	5.52	0.07	402	0.524	1.10	1.13	1.21
	AVG.	32768.17	5.07	0.06	358	0.470	1.10	1.16	1.40

Remark (see figure 3)

Fo = fr ×{ C1/ (2×(Co + CL)) + 1 } (Hz)



Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

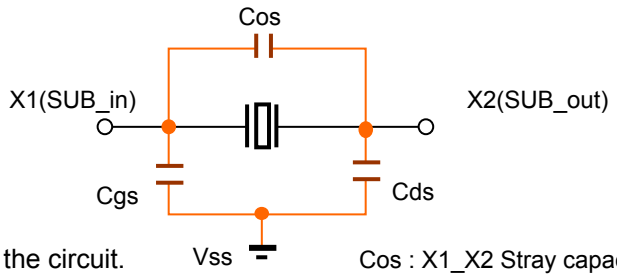
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL,

CL = Cg×Cd / (Cg + Cd) + Cs (pF)
Cs = Cgs×Cds / (Cgs + Cds) + Cos (pF)

where Cs(=3 to 5pF) stands for stray capacitance of the circuit.



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

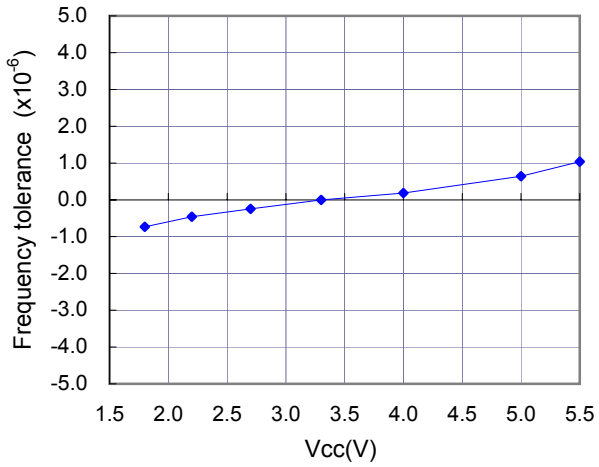
Evaluation of a Low Frequency Clock Oscillation Circuit

SSP-T7-F 12.5pF with R5F2LA88ANFP-80P [LQFP(12x12) 0.50mm pitch]

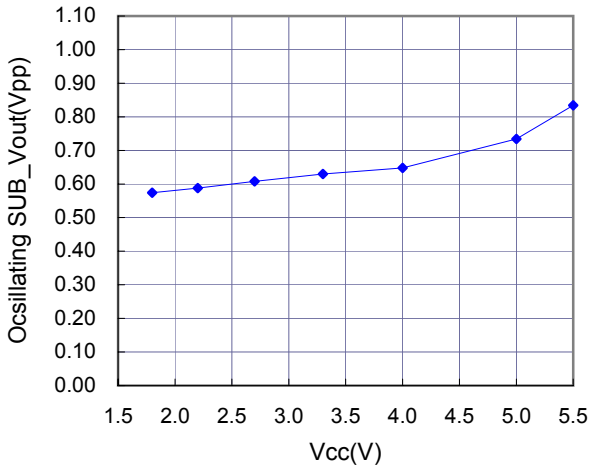
Measurement conditions : Vcc=1.8V to 5.5V at 25°C

Referential Data(1): Voltage characteristics

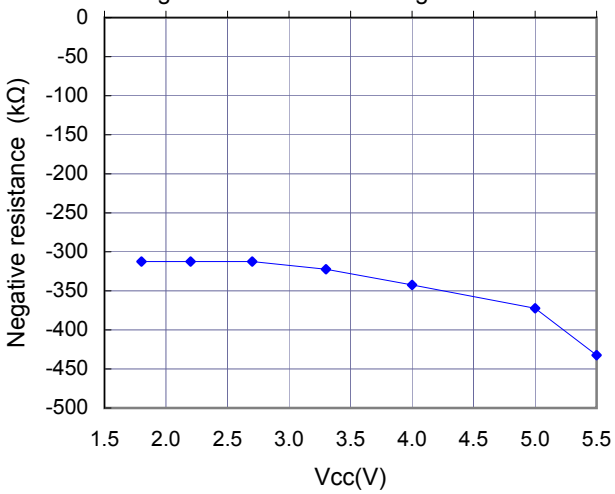
Frequency / voltage coefficient



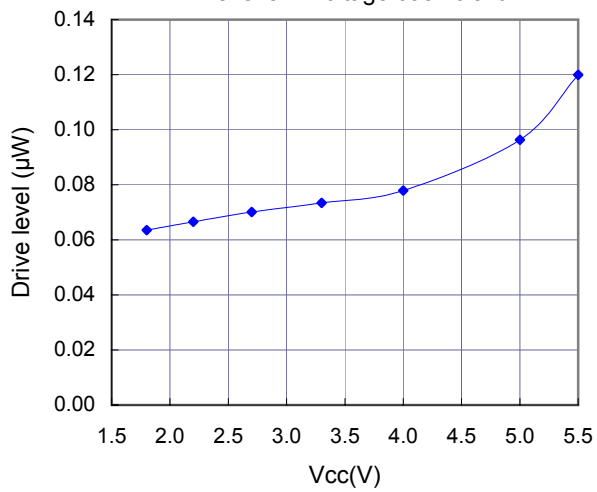
SUB_Vout / voltage coefficient



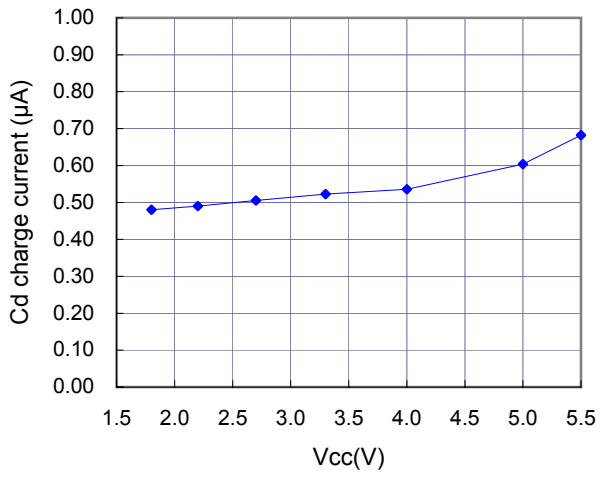
Negative resistance / voltage coefficient



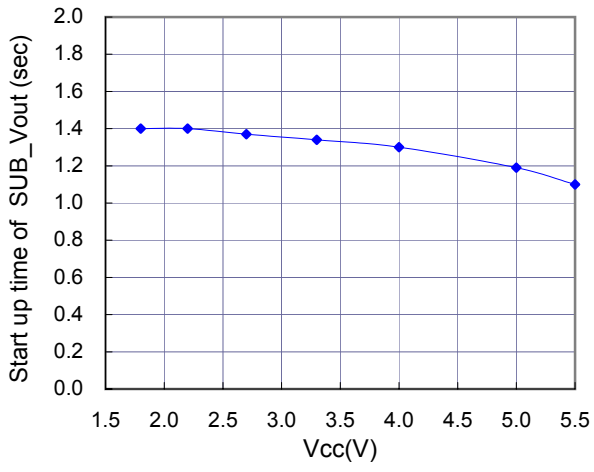
Drive level / voltage coefficient



Cd charge current / voltage coefficient



Start up time / voltage coefficient



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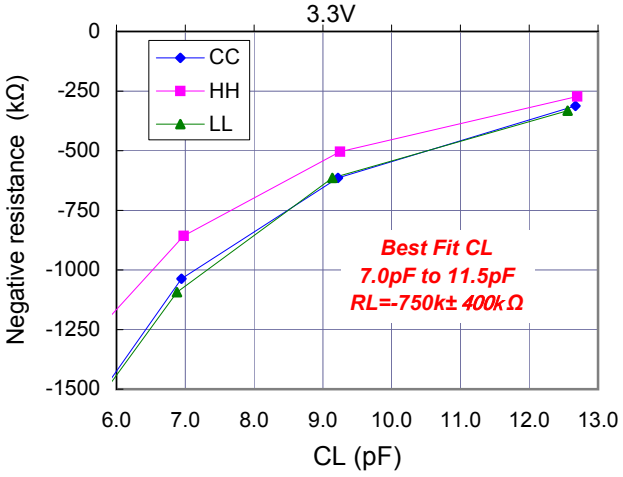
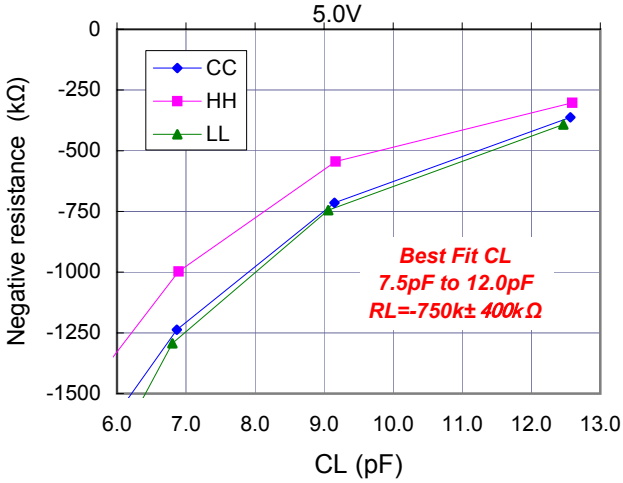
Measurement conditions : Vdd=3.3V,5.0V at 25°C

Referential Data(2) : Load capacitance characteristics

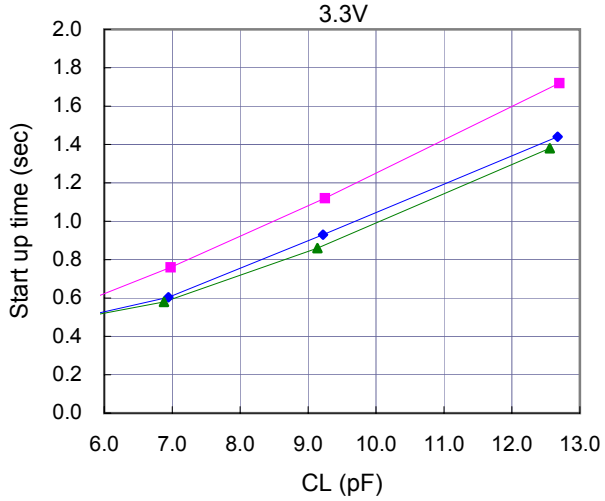
Negative resistance / load capcitance coefficient
3.3V



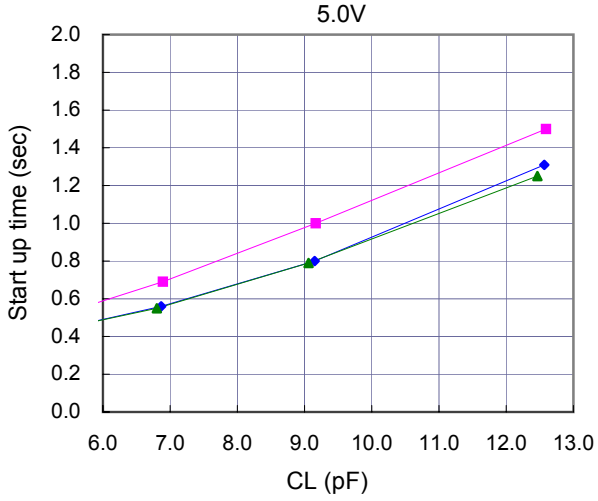
Negative resistance / load capcitance coefficient
5.0V



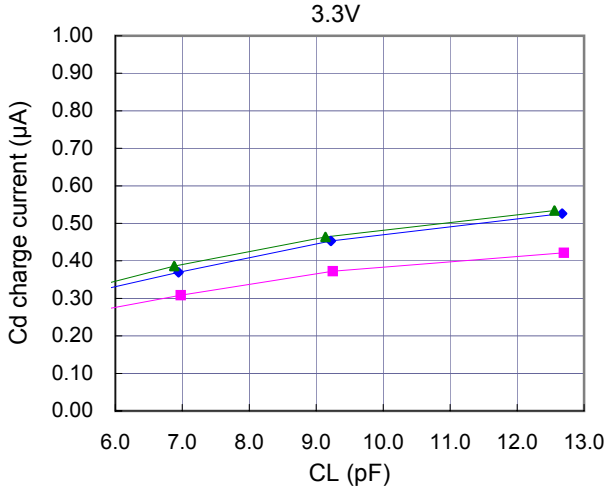
Start up time / load capacitance coefficient
3.3V



Start up time / load capacitance coefficient
5.0V



Cd charge current / load capacitance coefficient
3.3V



Cd charge current / load capacitance coefficient
5.0V