## Evaluation of a low frequency clock oscillation circuit

SSP-T7-FL 6.0pF with R5F2LA58ANFP-52P [LQFP(10x10) 0.65mm pitch]

Measurement conditions : Vcc=1.8V to 5.5V at 25℃

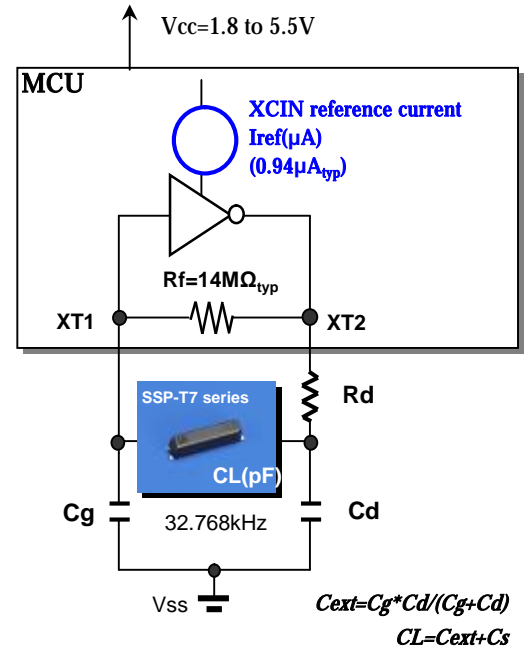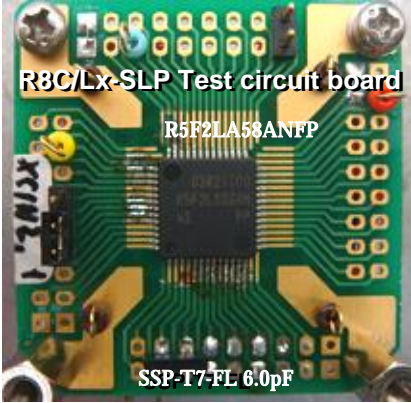**SII**

**Super Low Power consumption MCU**

# R8C/Lx-SLP XCIN1 oscillation circuit and recommended load capacitance

### For R8C/LA5x,LA3x

XCIN1 oscillation circuit consists of an excellent power saving circuit which realizes stable oscillation at low amplitude.

R8C/Lx-SLP Test circuit board
R5F2LA58ANFP
SSP-T7-FL 6.0pF

For your design reliability, please refer to Table 1 which shows the performance of the XCIN1 oscillation circuit and the recommended load capacitance for each resonator.

### SSP-T7 series

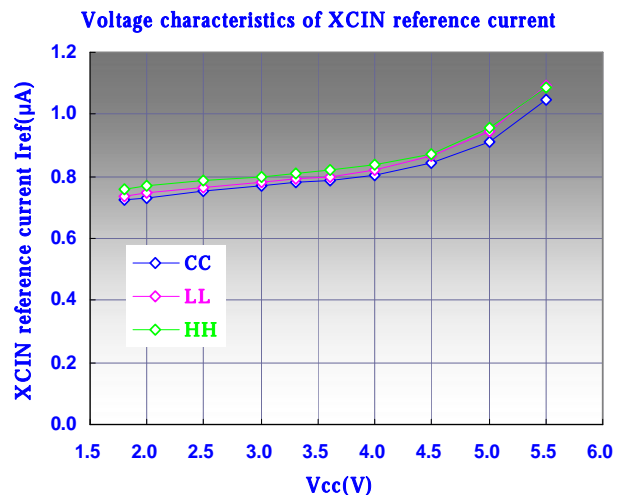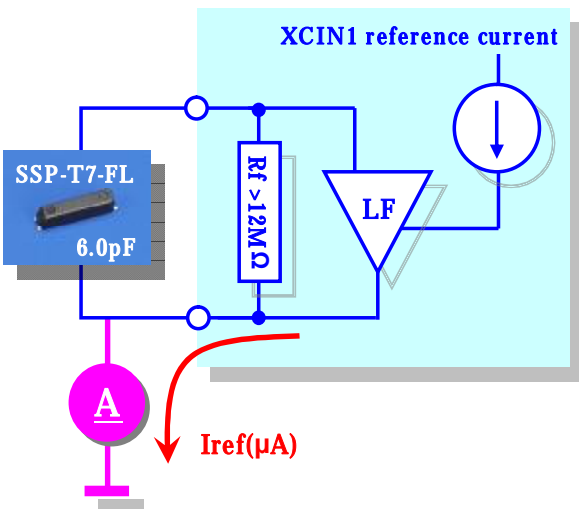SSP-T7-FL CL=3.7pF,4.4pF,6.0pF and SSP-T7-F CL=7.0pF,9.0pF,12.5pF
VT-200-FL CL=3.7pF,4.4pF,6.0pF and VT-200-F CL=12.5pF

Vcc=1.8 to 5.5V

**MCU**

XCIN reference current
$Iref(\mu A)$
$(0.94\mu A_{typ})$

$Rf=14M\Omega_{typ}$

XT1  XT2

SSP-T7 series
Rd
CL(pF)
Cg  32.768kHz  Cd

Vss

$Cext=Cg*Cd/(Cg+Cd)$
$CL=Cext+Cs$

### Table 1 XCIN low current oscillation circuit and load capacitance for a resonator

| XCIN_OSC | CL | Vcc | IC test sample | dF/Cext[*1] $(*10^{-6})$ | Iref $(\mu A)$ | Ts (sec) |
|---|---|---|---|---|---|---|
| XCIN1 | 6.0pF Cg=6pF,Cd=6pF | 5.0V± 10% | CC | 3.51 | 0.904 | 0.64 |
| | | | LL | 3.52 | 0.944 | 0.58 |
| | | | HH | 3.52 | 0.954 | 0.58 |
| | | 2.0V± 10% | CC | 3.34 | 0.726 | 0.73 |
| | | | LL | 3.34 | 0.745 | 0.64 |
| | | | HH | 3.34 | 0.767 | 0.65 |

* )GRM1552C1HxR0CZ01D1 and GRM1552C1H100JZ01D(±5% .

### Super-low power consumption R8C/Lx -SLP and SSP-T7-FL 6.0pF

**XCIN1 reference current**

SSP-T7-FL
6.0pF

$Rf >12M\Omega$

LF

A

$Iref(\mu A)$

**Voltage characteristics of XCIN reference current**

XCIN reference current Iref(μA)

- CC
- LL
- HH

Vcc(V)

**R8C/Lx (LA5x,LA3x)**

# Evaluation of a low frequency clock oscillation circuit

SSP-T7-FL 6.0pF with R5F2LA58ANFP-52P [LQFP(10x10) 0.65mm pitch]

Measurement conditions : Vcc=3.3V,5.0V

**SII**

**An external resistor,Rf >12MΩ_ Built-in**

**New**

**SSP-T7-FL**

**CL=6.0pF**

| Model | :SSP-T7-FL |
|---|---|
| Frequency | :Fo=32.768kHz |
| Frequency tolerance | :dF/Fo=±20x10⁻⁶ |
| Load capacitance | :CL=6.0pF |
| Equivalent series resistance | :R1=65kΩ max |
| Max. drive level | :DL=1µW max |
| Level of drive | :DL=0.01µW typ |

Model : $SSP\text{-}T7\text{-}FL$
Frequency : $Fo=32.768kHz$
Frequency tolerance : $dF/Fo=\pm20\times10^{-6}$
Load capacitance : $CL=6.0pF$
Equivalent series resistance : $R1=65k\Omega$ max
Max. drive level : $DL=1\mu W$ max
Level of drive : $DL=0.01\mu W$ typ

Vcc=1.8 to 5.5V

MCU

XCIN reference current Iref(µA)

**Rf>12MΩ**

XCIN         XCOUT

Rd (Ω)

Cg    32.768kHz    Cd

Vss    *CL=CgCd / (Cg+Cd)+Cs*

FEATURES

1. Ultra thin type with 1.4mm Max.
2. SMD type suitable for automatic & high density surface mounting.
3. Plastic mold package containing highly reliable tubular type quartz crystal.
4. Excellent shock and heat resistance.

RECOMMENDED SOLDERING PATTERN

0.6    0.3
0.6
1.2    5.1    1.2

Unit:mm
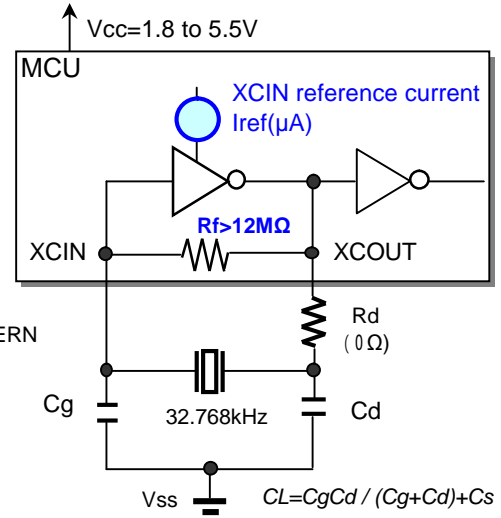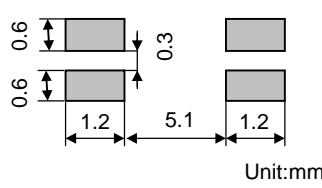
*Super-low power consumption R8C/Lx-SLP and Low CL SSP-T7-FL 6pF*

*XCIN1 oscillation circuit consists of an excellent power saving circuit which realizes stable oscillation at low amplitude.*

MODEL:SSP-T7-FL 6pF with R5F2LA58ANFP at 25°C

| Key specifications | Vcc=3.3V | Vcc=5.0V | Remarks |
|---|---|---|---|
| Load capacitance : CL(pF) | 6.0 | 6.0 | Recommended value of CL |
| Current control resistance : Rd ( k ohm ) | 0 | 0 | Control drive level & secure phase margin |
| Capacitance at gate : Cg ( pF ) | 6 | 6 | Optimal capacitance in response to CL |
| Capacitance at drain : Cd ( pF ) | 6 | 6 | ( CL = Cd // Cg + stray capacitance ) |

| Circuit characteristics ( at 25°C ) | Vcc=3.3V | Vcc=5.0V | Remarks |
|---|---|---|---|
| Matching Accuracy : dF / F ( x10⁻⁶ ) | 1.9 | 3.5 | Frequency offset volume at specified Vcc |
| Vdd Fluctuation : +/-dF / V ( x10⁻⁶ ) | 0.2 | 1.0 | Vdd +/-10% ( Standard operating voltage range ) |
| Cext Fluctuation : +/-dF / C ( x10⁻⁶ ) | 3.4 | 3.5 | Cext ±5% ( Standard operating Cg,Cd range ) |
| **Total Fluctuation : +/-dF / Total ( x10⁻⁶ )** | **3.66** | **4.51** | **Clock accuracy: dF/Total=dF/V+dF/C < ±11.7sec/M** |
| **Oscillation start up time : Ts ( sec )** | **0.69** | **0.64** | **Time to reach 90% of output level, Ts < 0.8sec** |
| **XCIN reference current : Iref (µA)** | **0.77** | **0.90** | **Low powe consumption, Iref < 1.1µA** |
| Negative resistance : | - RL | ( kΩ ) | 1050 | 1106 | RL = -1050±750kΩ at Rf>12MΩ |
| Oscillation allowance : M ( times ) | 16 | 17 | Judgmental standard of oscillation stability |
| Drive Level : DL (nW ) | 42 | 55 | DL=Ix² Re < 1x10⁻⁶W,Re=R1( 1 + Co / CL )² < 0.1µW |
| Voltage of oscillation start : Vstart (V ) | 1.15 | 1.15 | |
| Voltage of oscillation stop : Vstop (V ) | 1.13 | 1.13 | |

| Temperature characteristics of circuit | | Vcc=3.3V | Vcc=5.0V | Remarks |
|---|---|---|---|---|
| at -40°C | Variation : df / T ( x10⁻⁶ ) | -137 | -137 | Typ.Tp=25°C ( K = -3.5×10⁻⁸ / °C² ) |
| at +85°C | Variation : df / T ( x10⁻⁶ ) | -128 | -128 | Typ.Tp=25°C ( K = -3.5×10⁻⁸ / °C² ) |

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

**We value the "takumi" spirit.**

# Evaluation of a low frequency clock oscillation circuit

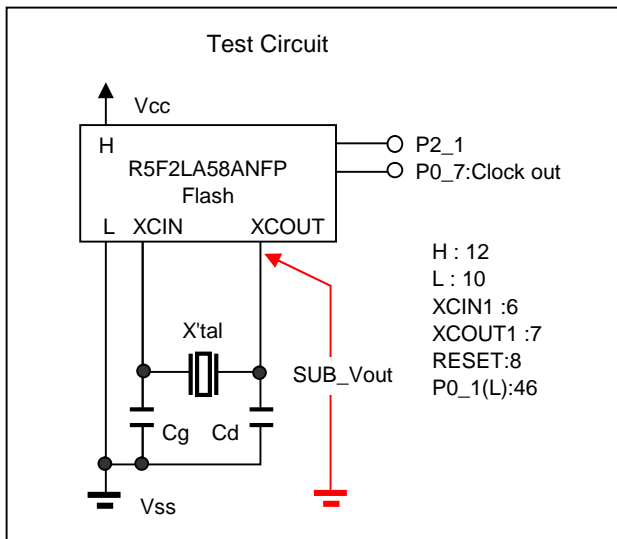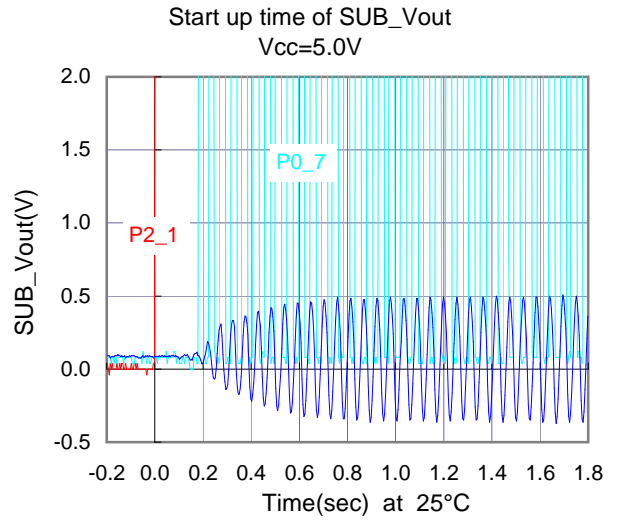SSP-T7-FL 6.0pF with R5F2LA58ANFP-52P [LQFP(10x10) 0.65mm pitch]

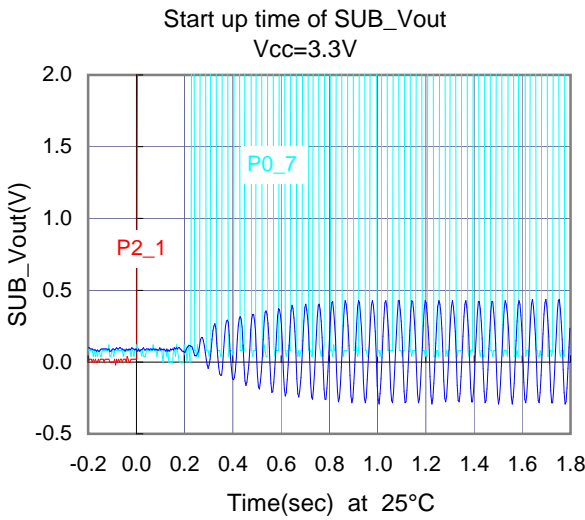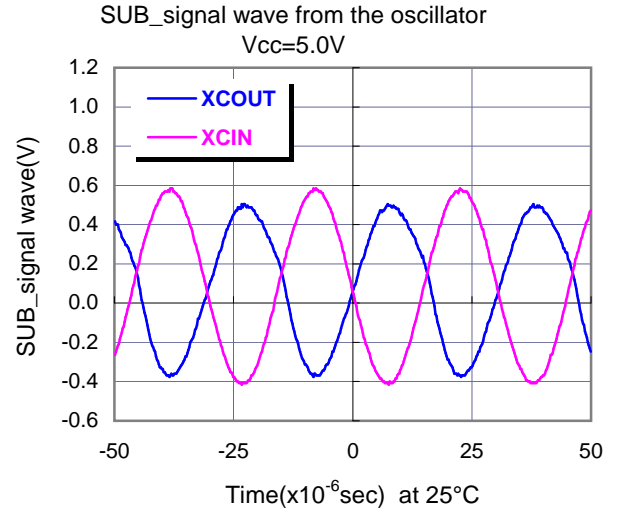Measurement conditions : Vcc=3.3V,5.0V

**SII**

**An external resistor,Rf >12MΩ_ Built-in**

Test Data

| CL(pF) | Vcc(V) | Cs(pF) | Cg(pF) | Cd(pF) |
|--------|--------|--------|--------|--------|
| 6.0    | 5.0    | 2.84   | 6.02   | 5.98   |
|        | 3.3    | 2.91   | 6.02   | 5.98   |

SUB_signal wave from the oscillator
Vcc-3.3V



SUB_signal wave from the oscillator
Vcc=5.0V



Start up time of SUB_Vout
Vcc=3.3V



Start up time of SUB_Vout
Vcc=5.0V



Test Circuit



H : 12
L : 10
XCIN1 :6
XCOUT1 :7
RESET:8
P0_1(L):46
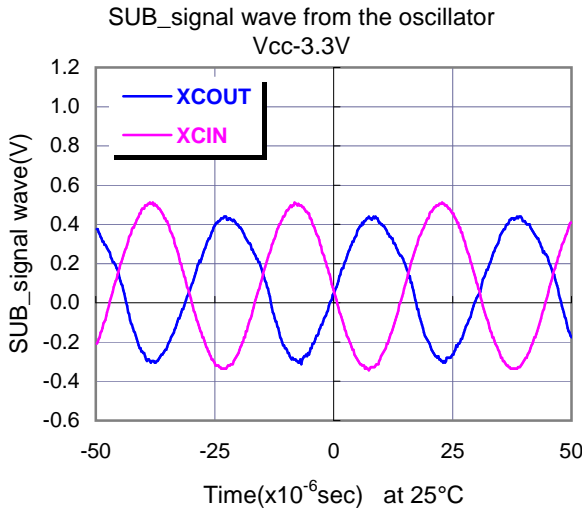
Temperature characteristics of oscillating frequency
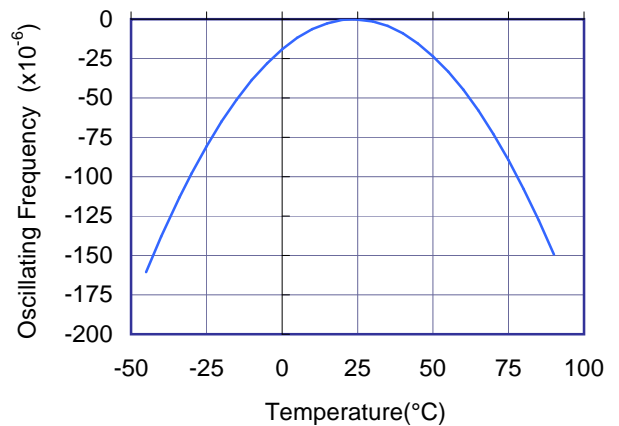
We value the "takumi" spirit.

# Evaluation of a low frequency clock oscillation circuit

SSP-T7-FL 6.0pF with R5F2LA58ANFP-52P [LQFP(10x10) 0.65mm pitch]

Measurement conditions : Vcc=3.3V,5.0V
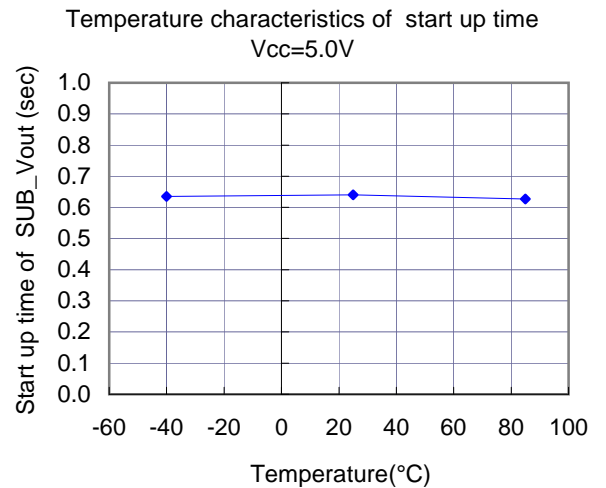
**SII**

**An external resistor,Rf >12MΩ_ Built-in**

Test Data : Temperature characteristics

| CL(pF) | Vcc(V) | Cs(pF) | Cg(pF) | Cd(pF) |
|--------|--------|--------|--------|--------|
| 6.0 | 5.0 | 2.84 | 6.02 | 5.98 |
| | 3.3 | 2.91 | 6.02 | 5.98 |
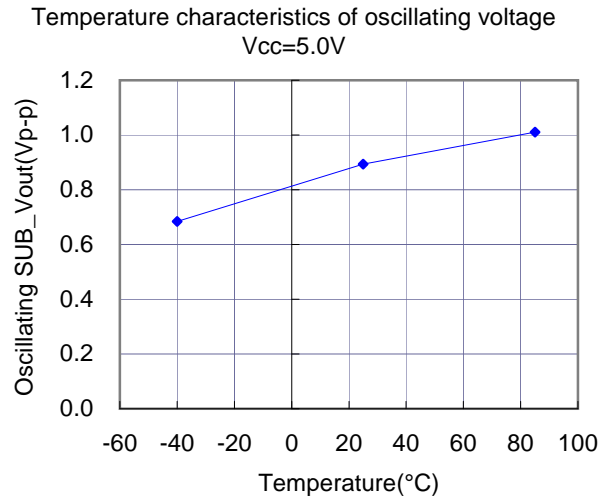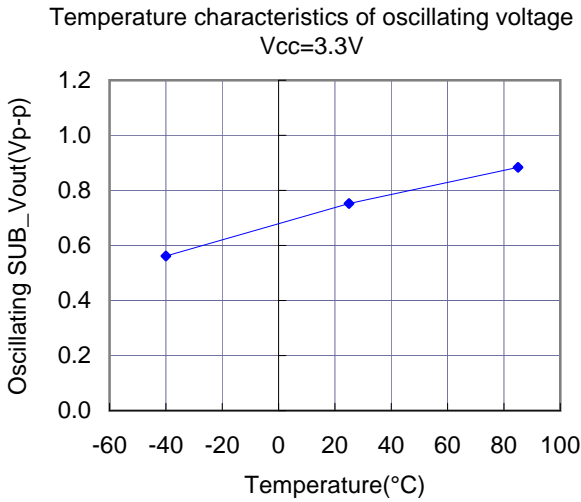
Temperature characteristics of oscillating voltage
Vcc=3.3V



Temperature characteristics of oscillating voltage
Vcc=5.0V



Temperature characteristics of Vstart, Vstop
Vcc=3.3V



Temperature characteristics of Vstart, Vstop
Vcc=5.0V



Temperature characteristics of start up time
Vcc=3.3V



Temperature characteristics of start up time
Vcc=5.0V

## Evaluation of a low frequency clock oscillation circuit

SSP-T7-FL 6.0pF with R5F2LA58ANFP-52P [LQFP(10x10) 0.65mm pitch]

Measurement conditions : Vcc=3.3V,5.0V
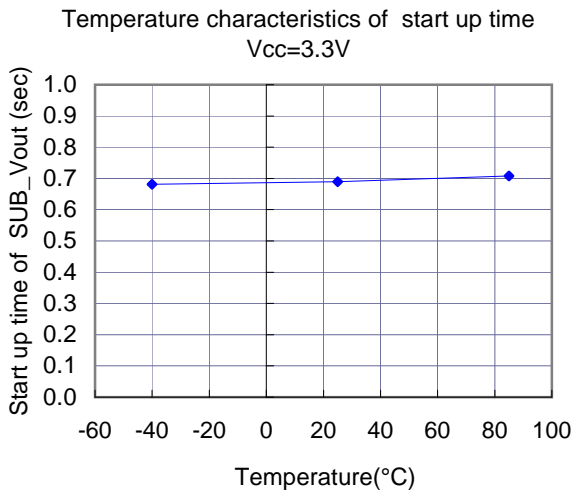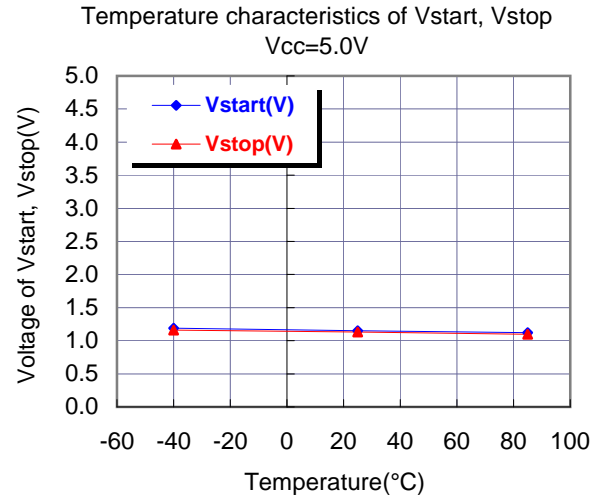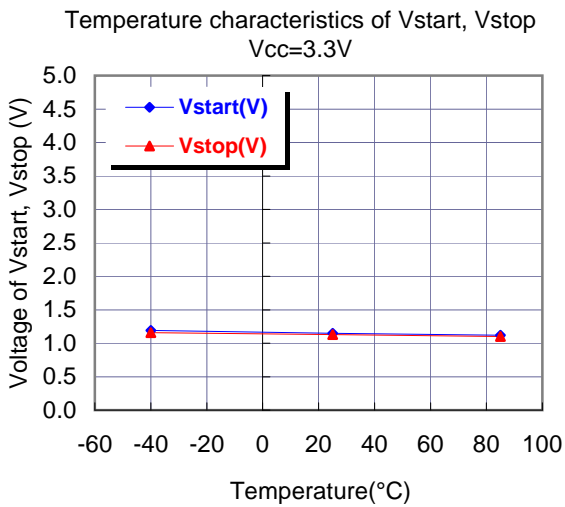
**SII**

**An external resistor,Rf >12MΩ_ Built-in**

### Referential components layout(see Figure 1)
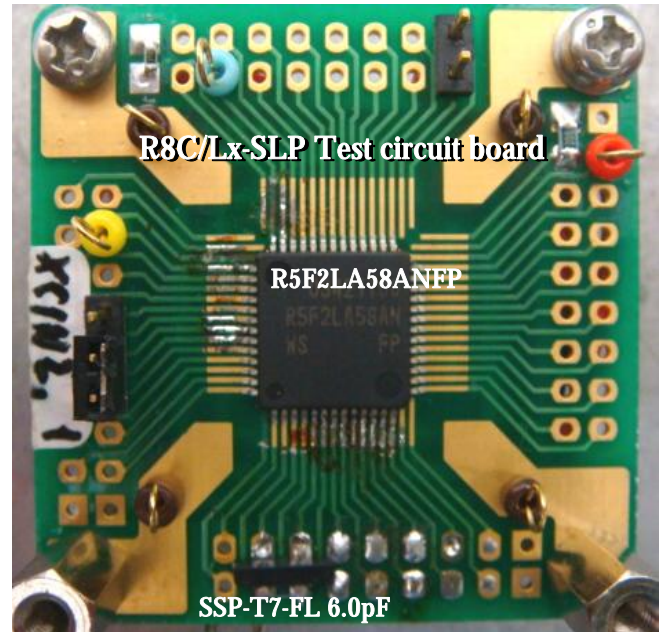
| CL(pF) | Vcc(V) | Cs(pF) | Cg(pF) | Cd(pF) |
|--------|--------|--------|--------|--------|
| 6.0 | 5.0 | 2.84 | 6.02 | 5.98 |
| | 3.3 | 2.91 | 6.02 | 5.98 |



R8C/Lx-SLP Top View

XCIN1

**R8C/Lx-SLP Test circuit board**

**R5F2LA58ANFP**

**SSP-T7-FL 6.0pF**

**Reference land pattern that SII recommends**

The reference pattern can decrease stray capacity Cos between terminals XCIN.

The reference pattern can be excellent in the noise-proof, and an efficient oscillation circuit be achieved.

Especially, it is a composition that is appropriate for the low CL oscillation circuit.

**Figure 1 Referential components layout**

### Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).



**Figure 2 Example of Incorrect Board Design**

**Remark** When using the subsystem clock, insert a resistor, Rd, in series on the SUB_out side.
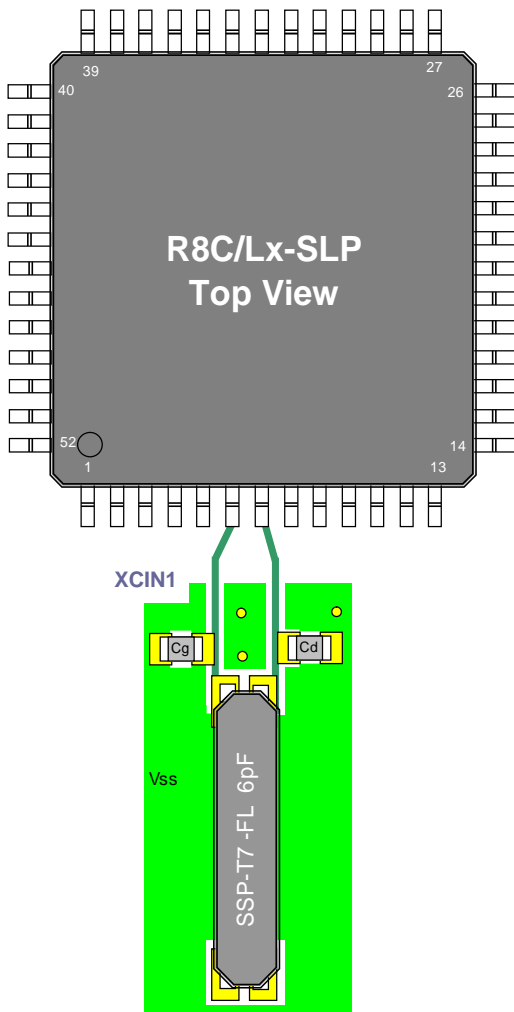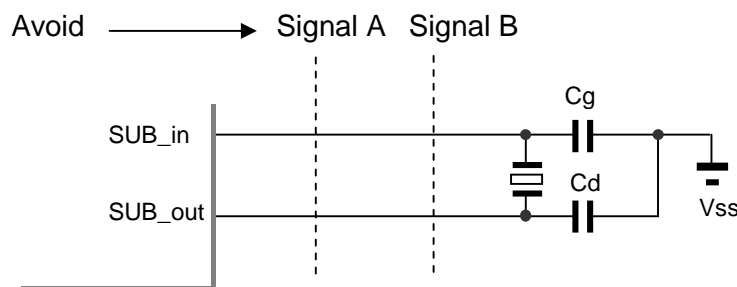
## Evaluation of a low frequency clock oscillation circuit

SSP-T7-FL 6.0pF with R5F2LA58ANFP-52P [LQFP(10x10) 0.65mm pitch]

Measurement conditions : Vcc=1.8V to 5.5V at 25°C

**SII**

**An external resistor,Rf >12MΩ_ Built-in**

### [Evaluation Sample at 25°C]

| No. | SAMPLE | CL( pF ) | Fo( Hz ) | fr( Hz ) | R1( kΩ) | Co( pF ) | C1( fF ) | Co/C1 | Q( k ) |
|---|---|---|---|---|---|---|---|---|---|
| | 1 | 6.0 | 32768.04 | 32763.07 | 37.7 | 0.91 | 2.096 | 433 | 61.5 |
| SSP-T7-FL | 2 | 6.0 | 32768.20 | 32763.26 | 39.7 | 0.90 | 2.081 | 433 | 58.8 |
| | 3 | 6.0 | 32767.80 | 32762.82 | 36.7 | 0.91 | 2.101 | 433 | 63.0 |

### [XCIN1 Test circuit data : Rd=0Ω,Cg=6pF,Cd=6pF and Cs at 6.0pF,25°C]

| Vcc | MCU SAMPLE | Matching Accuracy | | Clock accuracy of +shift (×10⁻⁶) | | | AC characteristics | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Cs(pF) | df / f( x10⁻⁶ ) | dF/V(10%) | dF/C(-5%) | Total | Iref(µA) | Ts(sec) | RL(kΩ) |
| 5.0V± 10% | CC | 2.84 | 3.51 | 0.99 | 3.51 | 4.51 | 0.904 | 0.64 | -1106 |
| | LL | 2.84 | 3.70 | 1.18 | 3.52 | 4.70 | 0.944 | 0.58 | -1400 |
| | LH | 2.84 | 3.50 | 1.26 | 3.51 | 4.77 | 0.970 | 0.57 | -1320 |
| | HL | 2.85 | 3.30 | 1.09 | 3.50 | 4.59 | 0.849 | 0.55 | -1320 |
| | HH | 2.84 | 3.70 | 1.03 | 3.52 | 4.55 | 0.954 | 0.58 | -1430 |
| 2.0V± 10% | CC | 3.01 | 0.31 | 0.54 | 3.34 | 3.88 | 0.726 | 0.73 | -1050 |
| | LL | 3.02 | 0.04 | 0.42 | 3.34 | 3.76 | 0.745 | 0.64 | -1250 |
| | LH | 3.01 | 0.13 | 0.45 | 3.34 | 3.80 | 0.763 | 0.70 | -1090 |
| | HL | 3.01 | 0.31 | 0.61 | 3.34 | 3.95 | 0.688 | 0.68 | -1150 |
| | HH | 3.02 | 0.11 | 0.48 | 3.34 | 3.82 | 0.767 | 0.65 | -1270 |

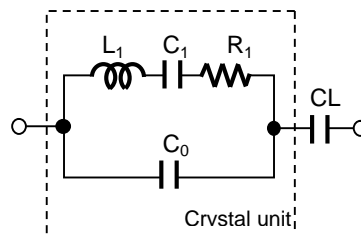### Remark ( see figure 3 )

$$Fo = fr \times \{ C_1 / ( 2 \times ( C_0 + CL )) + 1 \} \quad ( Hz )$$

$$( fa - fr ) / fr = 1/2 \times C_1 / C_0$$

$$Q = \omega L_1 / R_1 = 1/\omega C_1 R_1 = C_0 / C_1 \times 1/2\pi fr C_0 R_1$$

$$\gamma = C_0 / C_1 \qquad Q$$



Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

**Figure 3 Equivalent circuit of crystal unit, and CL**

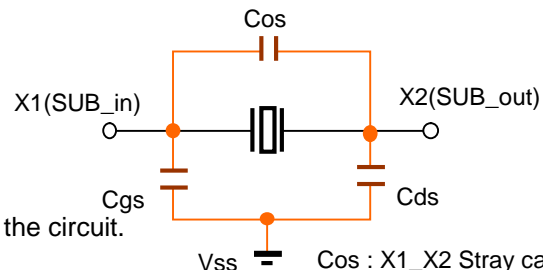### Remark ( see figure 4)

Approximate formula of the load capacitance of the circuit CL,

$$CL = Cg \times Cd / (Cg + Cd) + Cs \quad (pF)$$
$$Cs = Cgs \times Cds / (Cgs + Cds) + Cos \quad (pF)$$

where Cs(=2.7 to 3.1pF) stands for stray capacitance of the circuit.

| Vcc=0V | XCIN1 |
|---|---|
| Cos(pF) | 1.10 |
| Cgs(pF) | 4.10 |
| Cds(pF) | 4.00 |



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

**Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit**

Resonator circuit constants differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

# Evaluation of a low frequency clock oscillation circuit

SSP-T7-FL 6.0pF with R5F2LA58ANFP-52P [LQFP(10x10) 0.65mm pitch]

Measurement conditions : Vcc=1.8V to 5.5V at 25°C

**SII**

**An external resistor,Rf >12MΩ_ Built-in**

## Referential Data(1): Voltage characteristics

**Clock accuracy**

### Frequency / voltage coefficient



**High-speed**

### Start up time / voltage coefficient



**Power saving**

### XCIN reference current / voltage coefficient



### Drive level / voltage coefficient



### Negative resistance / voltage coefficient



### Cd charge current / voltage coefficient

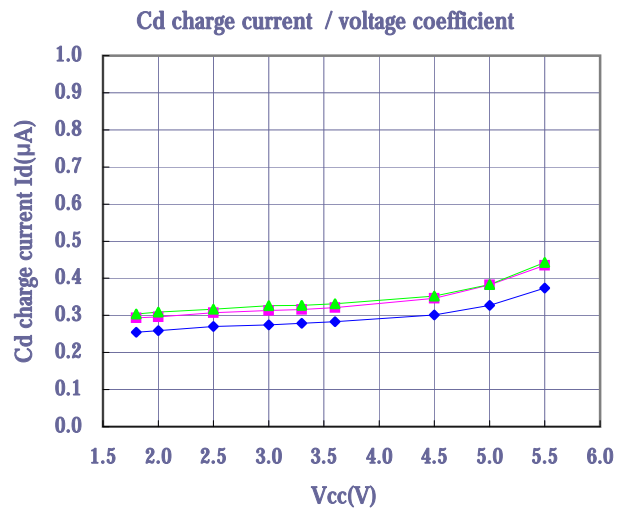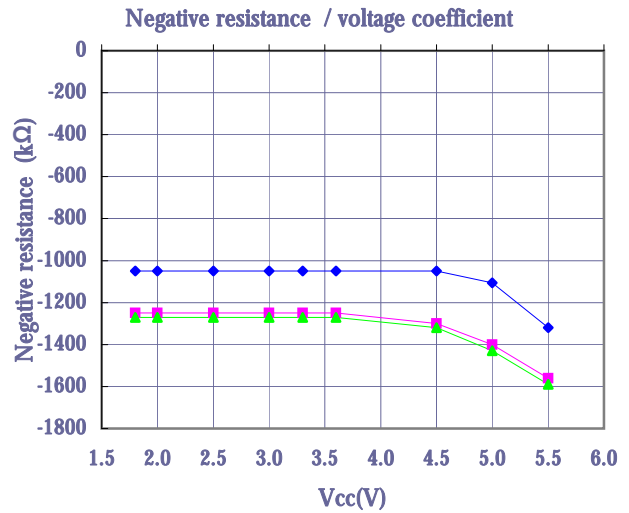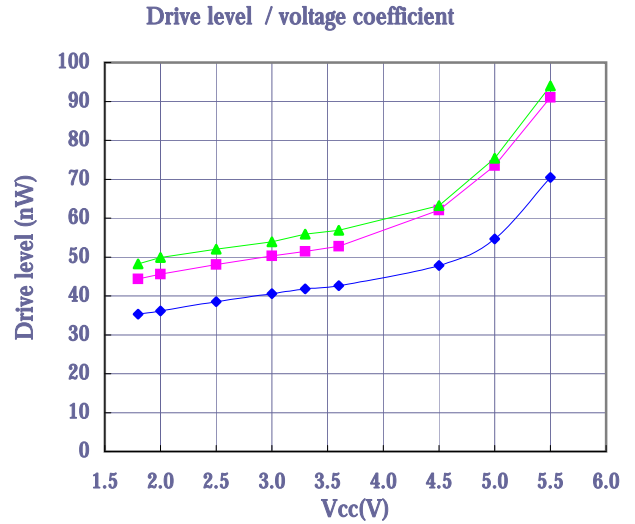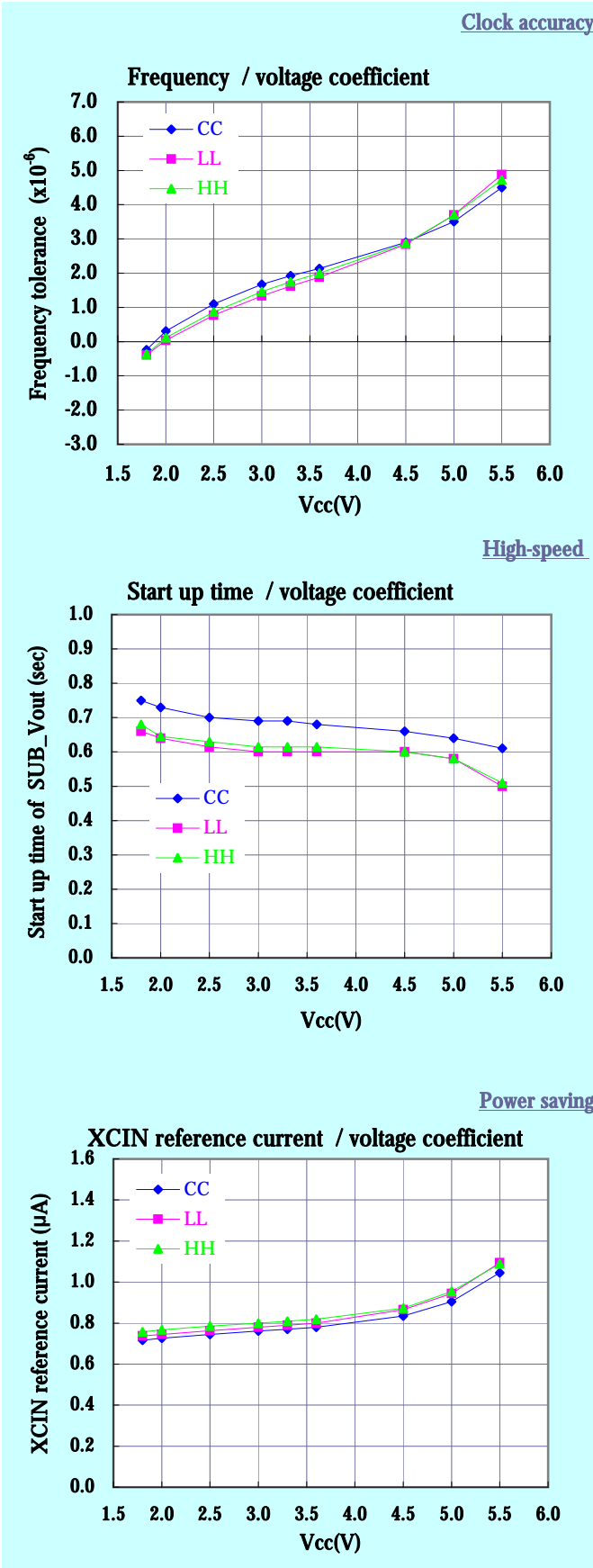## Evaluation of a low frequency clock oscillation circuit

SSP-T7-FL 6.0pF with R5F2LA58ANFP-52P [LQFP(10x10) 0.65mm pitch]

Measurement conditions : Vcc=5.0V at 25°C

**SII**

**An external resistor,Rf >12MΩ_ Built-in**

### Referential Data(2): Value tolerance of external capacitors (±5%) and frequency stability

Figure 5 shows the association chart of maximum deviation, $(\Delta)_{CL}$, with capacitance tolerance of Cext (±5%).

$$CL \quad Cs \quad Cext \quad Cs \quad \frac{Cg \times Cd}{Cg \quad Cd} \quad pF$$

$$f \quad fosc \quad Fo \quad fr \times \left[ \frac{C1}{2(Co \quad Cs \quad Cext)} \quad \frac{C1}{2(Co \quad CL)} \right]$$

$$)_{CL} = \left( — \right)_{max} - \left( — \right)_{min}$$

$$\left( — \right)_{max} \quad \frac{C1}{Co \quad Cs \quad Cext \quad Cext)}$$

$$\left( — \right)_{min} \quad \frac{C1}{Co \quad Cs \quad Cext \quad Cext)}$$

$$— = \frac{C1}{Co \quad CL)}$$

$$\begin{cases} CL = Cs + Cext \\ Cext = \frac{Cg \times Cd}{Cg \quad Cd} \end{cases}$$

$(—)_{max}$

$)_{CL}$

Max. dispersion range

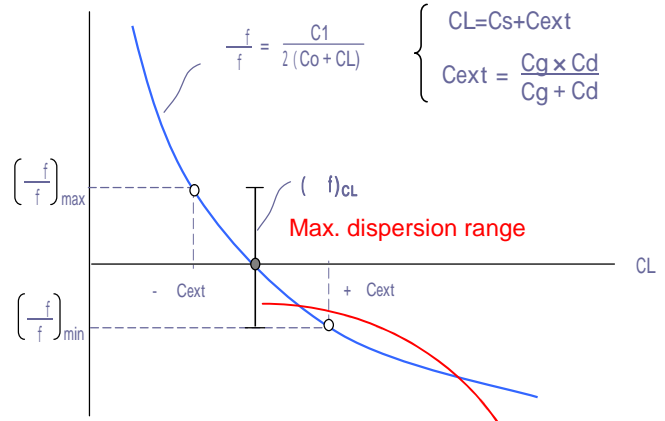Cext

$(—)_{min}$

+ Cext

CL

**Figure 5  Load capacitance characteristics of frequency**

**Table 3  Maximum frequency deviations with capacitance tolerance of cext (±5%)**

| Vcc(V) | Cext_5% | Cg(pF) | Cd(pF) | Cs(pF) | CL(pF) | df/CL(*10^{-6}) | $\Delta f_{CL}$(*10^{-6}) |
|---|---|---|---|---|---|---|---|
| 5.0 | Cext_min. | 5.72 | 5.68 | 2.84 | 5.69 | 7.02 | 6.90 |
| | Cext_typ. | 6.02 | 5.98 | 2.84 | 5.84 | 3.50 | |
| | Cext_max. | 6.32 | 6.28 | 2.84 | 5.99 | 0.12 | |
| 3.3 | Cext_min. | 5.72 | 5.68 | 2.91 | 5.76 | 5.36 | 6.76 |
| | Cext_typ. | 6.02 | 5.98 | 2.91 | 5.91 | 1.91 | |
| | Cext_max. | 6.32 | 6.28 | 2.91 | 6.06 | -1.39 | |

**Table 4  Maximum frequency deviations with capacitance tolerance of Cext (±5%)**

| CL(pF) | Cs(pF) | / _max | / _min | $\Delta f_{CL}$(*10^{-6}) |
|---|---|---|---|---|
| 12.0 | 2.8 | 2.98 | -2.78 | 5.77 |
| 9.0 | 2.8 | 3.39 | -3.19 | 6.58 |
| 8.0 | 2.8 | 3.51 | -3.31 | 6.81 |
| 7.0 | 2.8 | 3.58 | -3.39 | 6.97 |
| 6.0 | 2.8 | 3.55 | -3.39 | 6.93 |
| 5.8 | 2.8 | 3.53 | -3.37 | 6.90 |
| 5.0 | 2.8 | 3.30 | -3.18 | 6.48 |
| 4.4 | 2.8 | 2.94 | -2.85 | 5.79 |
| 3.7 | 2.8 | 2.13 | -2.09 | 4.23 |

**Cext; Combined capacitance of external capacitors**

Cg

**Cs**

Cd

Rf

CL

Cs=2.8pF

P0_7

Maximum deviations of frequency ,$(\Delta f)_{CL}$, with capacitance tolerance of Cext (±5%)

at Cs=0pF,Co/C1=433

CL=6.0pF

at Cs=2.8pF,Co/C1=433

$(\Delta f)_{CL}$(ppm)
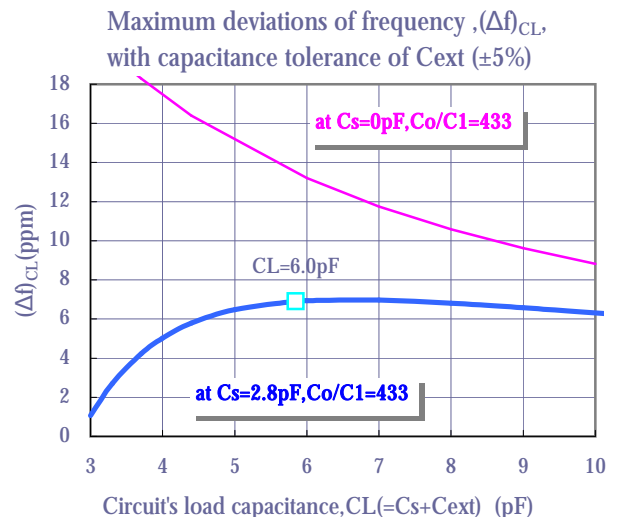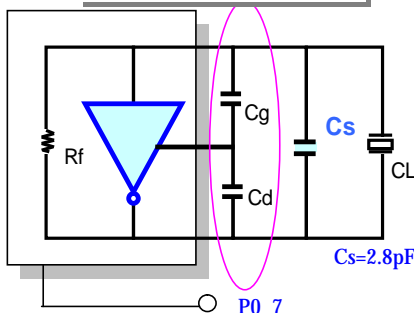
Circuit's load capacitance,CL(=Cs+Cext)  (pF)

**Figure 6  Maximum frequency deviations with capacitance tolerance**

We value the "takumi" spirit.