ISL71831SEH

Combined Neutron and TID Testing of the ISL71831SEH 32-Channel Analog Multiplexer

Introduction

This report summarizes results of combined 1MeV equivalent neutron testing and High Dose Rate (HDR) Total Ionizing Dose (TID) testing of the ISL71831SEH 32-channel low voltage analog multiplexer. The test was conducted to determine the sensitivity of the part to displacement damage (DD) and total dose effects caused by neutron or proton environments. Neutron fluences ranged from 5×10^{11}n/cm^2 to 1×10^{13}n/cm^2. HDR testing was completed through 100krad(Si).

Product Description

The ISL71831SEH is a radiation tolerant 32-channel analog multiplexer that is fabricated using Renesas' proprietary P6SOI process technology to provide excellent latch-up performance. The part operates over a single supply range from 3V to 5.5V and has five digital address inputs plus an enable pin that can be driven with adjustable logic thresholds to select one of 32 available channels. Inactive channels are isolated from the active channel by high impedance which inhibits any interaction between them.

The ISL71831SEH's low switch ON-resistance allows for improved signal integrity and reduced power losses. The part is also designed for cold sparing, making it compatible with redundancy techniques in high reliability applications. It is designed to provide a high impedance to the analog source in a powered OFF condition, making it easy to add additional backup devices without incurring extra power dissipation. The ISL71831SEH also has analog overvoltage protection on the switch inputs that disables the switch during an overvoltage event to protect upstream and downstream devices. All inputs are electrostatic discharge (ESD) protected to 5kV Human Body Model (HBM).

The ISL71831SEH is available in a 48 Ld ceramic Quad Flatpack (CQFP) and operates across the extended temperature range of -55°C to +125°C.

A typical application schematic or the ISL71831SEH is shown in Figure 1

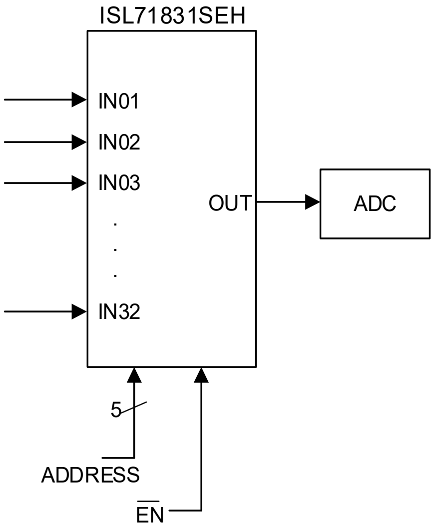


Figure 1. ISL71831SEH Typical Application Schematic

Contents

1. Test Description

1.1 Irradiation Facility

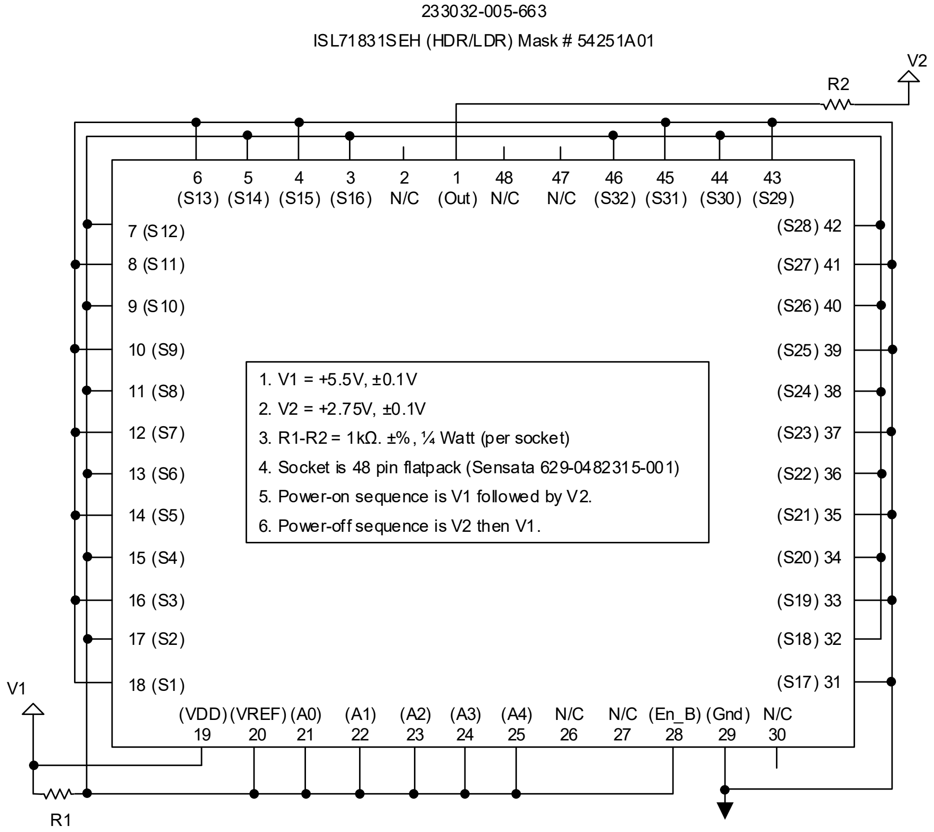
Neutron fluence irradiations were performed on the test samples on August 31, 2021, at the University of Massachusetts, Lowell (UMASS Lowell) fast neutron irradiator per Mil-STD-883G, Method 1017.2, with each part unpowered during irradiation. The target irradiation levels were 5 x 10^{11}n/cm^2, 2 x 10^{12}n/cm^2, and 1 x 10^{13}n/cm^2. As neutron irradiation activates many of the heavier elements found in a packaged integrated circuit, the parts exposed at the higher neutron levels required (as expected) some cooldown time before being shipped back to Renesas (Palm Bay, FL) for electrical testing.

HDR testing was performed on January 25, 2022, using a Gammacell 220 gamma-ray irradiator located in the Renesas Palm Bay, Florida facility. The HDR irradiations were performed at 77rad(Si)/s per MIL-STD-883 Method 1019.7. A PbAl box was used to shield the test fixture and devices under test against low energy, secondary gamma radiation.

1.2 Test Fixturing

No formal irradiation test fixturing is involved for the neutron testing, as these DD tests are bag tests in the sense that the parts are irradiated with all leads unbiased.

Figure 2 shows the configuration used for the TID testing.



1. V1 = +5.5V, ±0.1V
2. V2 = +2.75V, ±0.1V
3. R1-R2 = 1kΩ. ±%, ¼ Watt (per socket)
4. Socket is 48 pin flatpack (Sensata 629-0482315-001)
5. Power-on sequence is V1 followed by V2.
6. Power-off sequence is V2 then V1.

Figure 2. Irradiation Bias Configuration and Power Supply Sequencing for the ISL71831SEH

1.3 Radiation Dosimetry

Table 1 shows dosimetry from UMASS Lowell indicating the total accumulated gamma dose and actual neutron fluence exposure levels for each set of samples.

Table 1. ISL71831SEH Neutron Fluence Dosimetry Data

Irradiation	Requested Fluence (n/cm^2)	Reactor Power (kW)	Time (s)	Fluence Rate (n/cm^2-s)[1][2]	Gamma Dose (rad(Si))[3]	Measured Fluence (n/cm^2)[4]
CRF#62106-A	5.00E+11	10	617	8.10E+08	70	5.38E+11
CRF#62106-B	2.00E+12	100	247	8.10E+09	281	2.05E+12
CRF#62106-C	1.00E+13	1000	123	8.10E+10	1401	1.14E+13

1. Dosimetry method: ASTM E-265.
2. The neutron fluence rate is determined from *Initial Testing of the New Ex-Core Fast Neutron Irradiator at UMass Lowell (6/18/02)*. Validated on 6/07/2011 under the Trident II D5LE neutron facility study by Navy Crane.
3. Based on reactor power at 1000kW, the gamma dose is 41krad(Si)/hr ±5.3% as mapped by TLD-based dosimetry
4. Validated by S-32 flux monitors.

1.4 Characterization Equipment and Procedures

Electrical testing for the neutron test was performed before and after neutron irradiation using the Renesas production automated test equipment (ATE). All electrical testing was performed at room temperature.

All electrical testing for the HDR test was performed outside the irradiator using the ATE with datalogging at each downpoint. Downpoint electrical testing was performed at room temperature.

1.5 Experimental Matrix

Neutron testing proceeded in general accordance with the guidelines of MIL-STD-883 TM 1017. The experimental matrix consisted of five samples to be irradiated at 5×10^{11}n/cm^2, five to be irradiated at 2×10^{12}n/cm^2, and five to be irradiated at 1×10^{13}n/cm^2. The actual levels achieved, which are shown in Table 2, were 5.38×10^{11}n/cm^2, 2.05×10^{12}n/cm^2, and 1.14×10^{13}n/cm^2. Following neutron testing, each set of samples underwent HDR TID testing. Each set of samples was irradiated under bias to 100krad(Si) with downpoints at 30krad(Si), 50krad(Si), and 100krad(Si). Five control units were used.

The 15 ISL71831SEH samples were drawn from lot 5STWBEH. Samples were packaged in the standard hermetic 48 Ld ceramic Quad Flatpack (CQFP). Samples were processed through burn-in before irradiation and were screened to the SMD limits at room, low, and high temperatures before the start of neutron testing.

2. Results

Combined neutron and high dose rate total ionizing dose testing of the ISL71831SEH is complete and the results are reported in the balance of this report. It should be understood when interpreting the data that each neutron irradiation was performed on a different set of samples; the damage from neutron testing was not cumulative. Following neutron testing, each set of samples underwent HDR TID testing in which the damage was cumulative.

2.1 Attributes Data

Table 2. ISL71831SEH Attributes Data

1MeV Fluence, (n/cm^2)		TID (krad(Si))	Sample Size	Pass[1]	Fail	Notes
Planned	Actual					
5×10^{11}	5.38×10^{11}	30	5	5	0	[2]
		50				
		100				
2×10^{12}	2.05×10^{12}	30	5	5	0	All passed
		50				
		100				
1×10^{13}	1.14×10^{13}	30	5	5	0	All passed
		50				
		100				

1. A pass indicates a sample that passes all SMD limits.
2. One sample experienced data corruption and was removed from switch ON-resistance match (Fig. 4), Break-Before-Make delay (Fig. 22), and enable turn - OFF time (Fig. 24) measurements.

2.2 Variables Data

The plots in Figure 3 through Figure 24 show data for key parameters before and after irradiation to each level. The plots show the mean of each parameter as a function of neutron and total dose irradiation. Each set of samples was irradiated to a different neutron fluence and is plotted as a distinct line. Each line only has markers at the radiation levels to which the corresponding set of samples was exposed. For example, the line representing a parameter of the set of samples irradiated to 5×10^{11}n/cm^2 has a marker at 5×10^{11}n/cm^2, but not at 2×10^{12}n/cm^2 or 1×10^{13}n/cm^2. All lines have makers at the pre-irradiation level and the total dose levels of 30krad(Si), 50krad(Si), and 100krad(Si).

For the switch measurements, the ATE program recorded the measurements for each of the 32 switches (such as leakage current), however, it was chosen to plot the average of the measurements. Therefore, if the graph and captions state that it is the average, the average of the 32 channels is plotted. Similarly, for the address and enable pins measurements, the average of A0-A4 and enable is plotted when the graph and captions state that it is the average. The plots also include error bars at each downpoint, representing the minimum and maximum measured values of the samples, although in some plots the error bars might not be visible because of their values compared to the scale of the graph. While the applicable electrical limits taken from the SMD are also shown, it should be noted that these limits are provided for guidance only as the ISL71831SEH is not specified for the neutron environment.

All samples passed the post-irradiation SMD limits after all three neutron exposures up to and including 1.14×10^{13}n/cm^2 and after HDR irradiation through 100krad(Si). One sample, which was exposed to 5.38×10^{11}n/cm^2, experienced data corruption of three parameter measurements either during test datalogging or transferring the data to a spreadsheet as evidenced by the sample's apparent return to normal functionality during the subsequent TID testing; those data were removed from switch ON-resistance match (Figure 4), Break-Before-Make delay (Figure 22), and enable turn-off time (Figure 24) measurements.

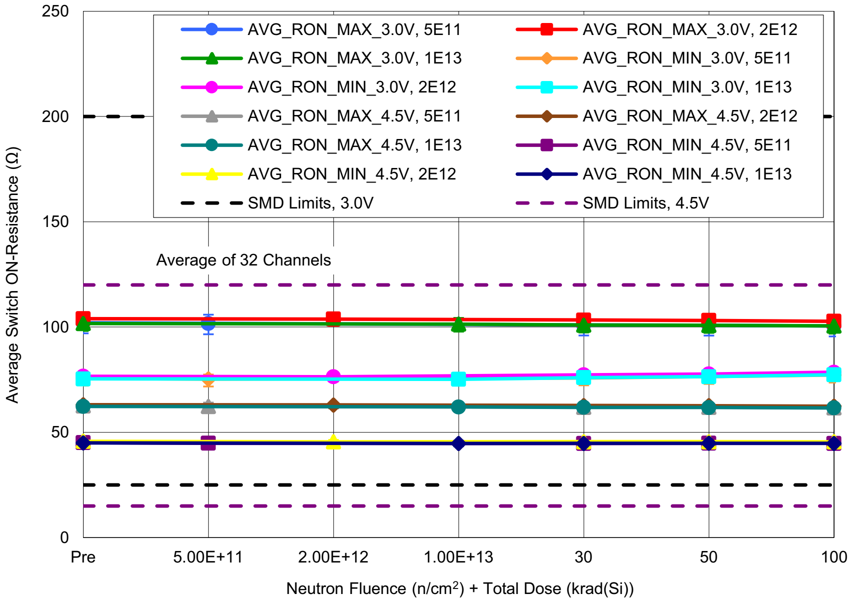


Figure 3. ISL71831SEH average switch ON-resistance minimum and maximum ($r_{DS(ON)}$) with V+ = 4.5V and 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limits are a minimum of 15Ω with a maximum 120Ω for a supply voltage of 4.5V, and a minimum of 25Ω with a maximum of 200Ω for a supply voltage of 3.0V.

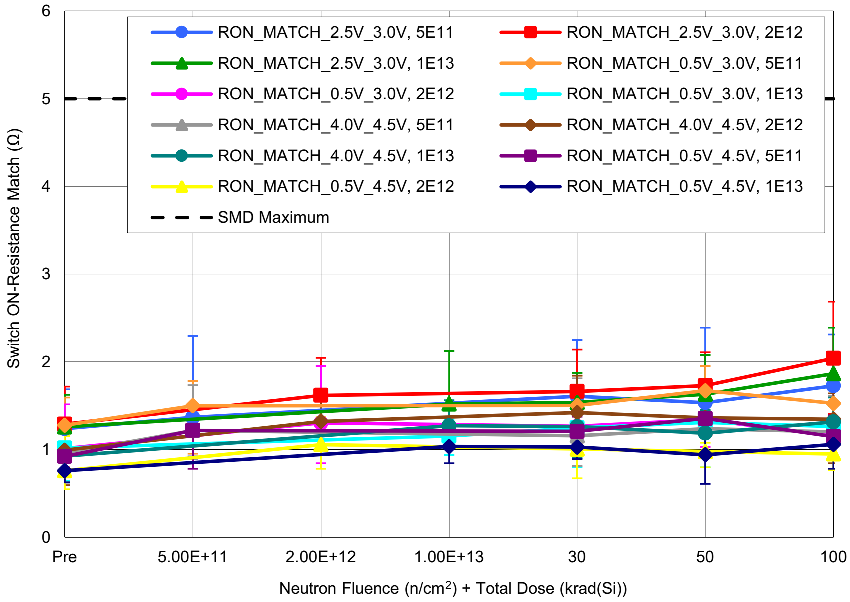


Figure 4. ISL71831SEH switch ON-resistance match ($\Delta r_{DS(ON)}$) with V+ = 4.5V and V_{IN} = 4.0V and 0.5V or V+ = 3.0V and V_{IN} = 2.5V and 0.5V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 5Ω for both supply voltages.

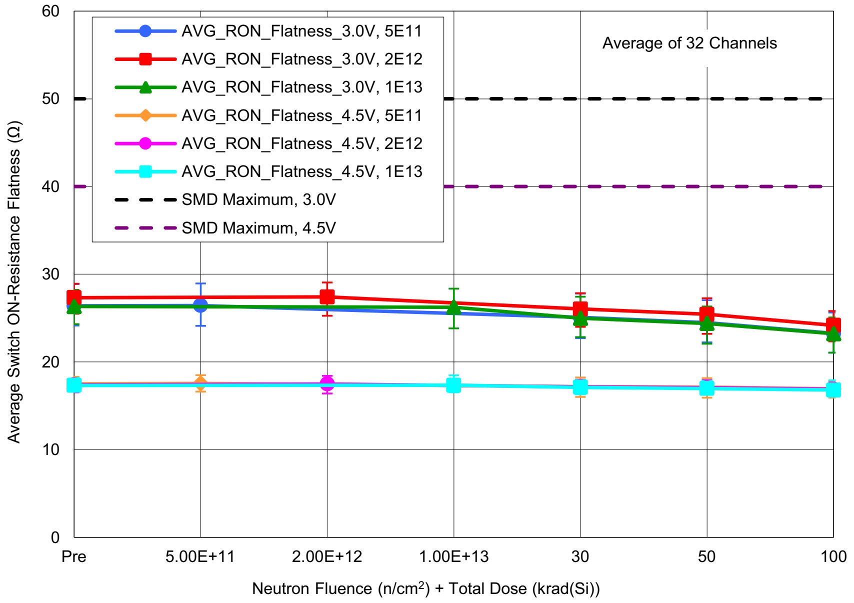


Figure 5. ISL71831SEH average ON-resistance flatness ($r_{FLAT(ON)}$) with V+ = 4.5V and 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limits are maximums of 40Ω for supply voltage 4.5V, and 50Ω for supply voltage 3.0V.

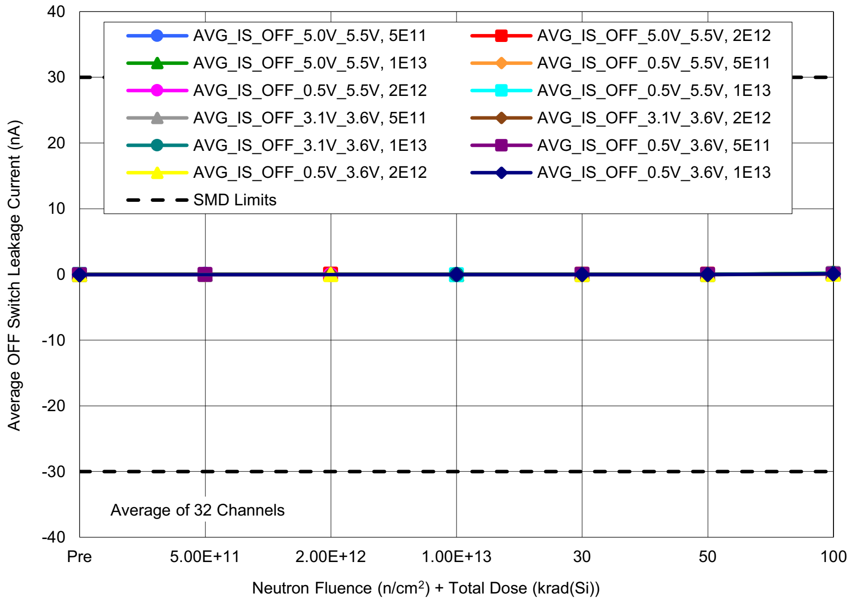


Figure 6. ISL71831SEH average switch input OFF leakage ($I_{IN(OFF)}$) with V+ = 5.5V, V_{IN} = 5.0V, V_{OUT} = 0.5V, or V+ = 5.5V, V_{IN} = 0.5V, V_{OUT} = 5.0V, or V+ = 3.6V, V_{IN} = 3.1V, V_{OUT} = 0.5V, or V+ = 3.6V, V_{IN} = 0.5V, V_{OUT} = 3.1V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limits are a minimum of -30nA with a maximum of 30nA for both supply voltages.

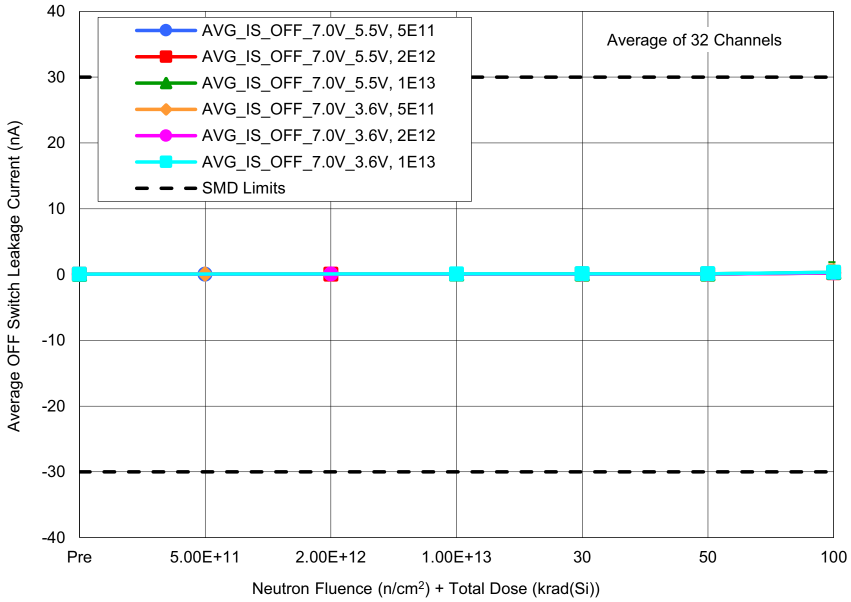


Figure 7. ISL71831SEH average switch input OFF Overvoltage leakage ($I_{IN(OFF-0V)}$) with V+ = 5.5V, 3.6V, V_{IN} = 7.0V, and unused inputs and V_{OUT} = 0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limits are a minimum of -30nA with a maximum of 30nA for both supply voltages.

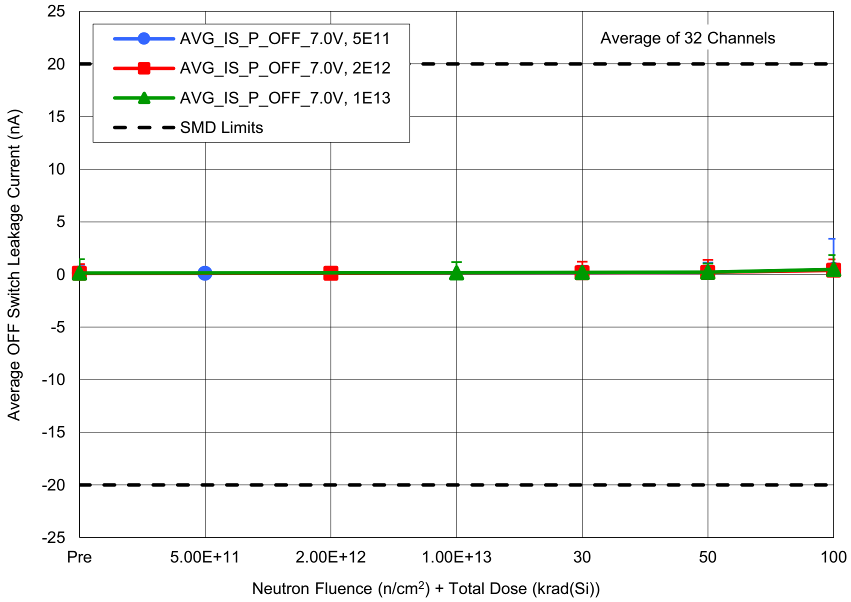


Figure 8. ISL71831SEH average switch input OFF leakage with supply voltage grounded ($I_{IN(POWER-OFF)}$) with V_{IN} = 7V and V+ = V_{OUT} = V_{EN} = V_{REF} = 0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limits are a minimum of -20nA with a maximum of 20nA.

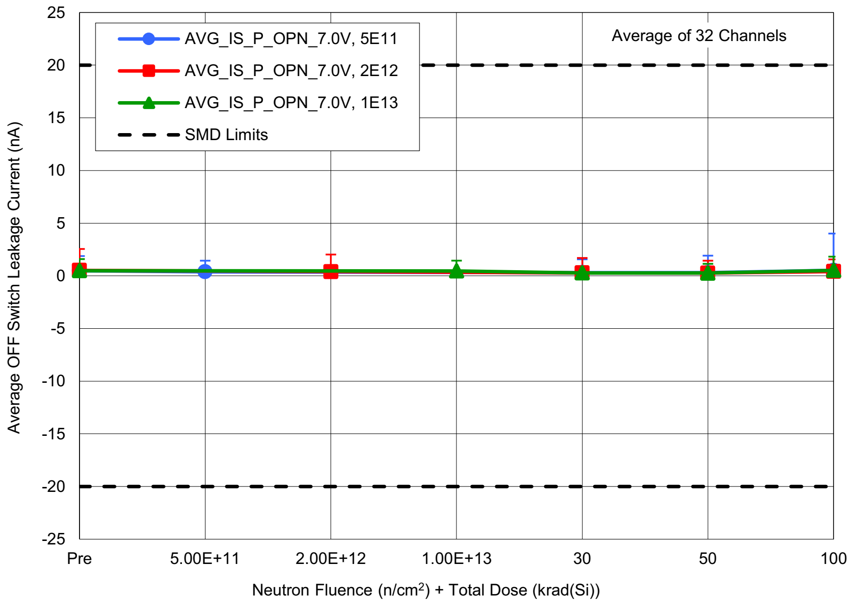


Figure 9. ISL71831SEH average switch input OFF leakage with supply voltage open ($I_{IN(POWER\text{-}OFF)}$) with V_{IN} = 7V, V_{OUT} = 0V, and V+ = V_{EN} = V_{REF} = Open following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limits are a minimum of -20nA with a maximum of 20nA.

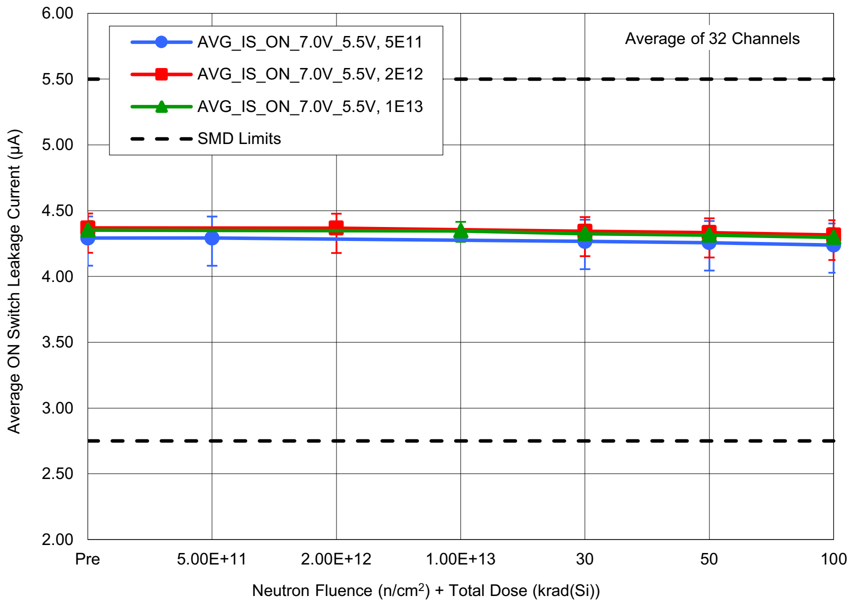


Figure 10. ISL71831SEH average switch ON input leakage with overvoltage applied to the input ($I_{IN(ON\text{-}0V)}$) with V+ = 5.5V, V_{IN} = 7.0V, and V_{OUT} = Open following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limits are a minimum of 2.75µA with a maximum of 5.50µA.

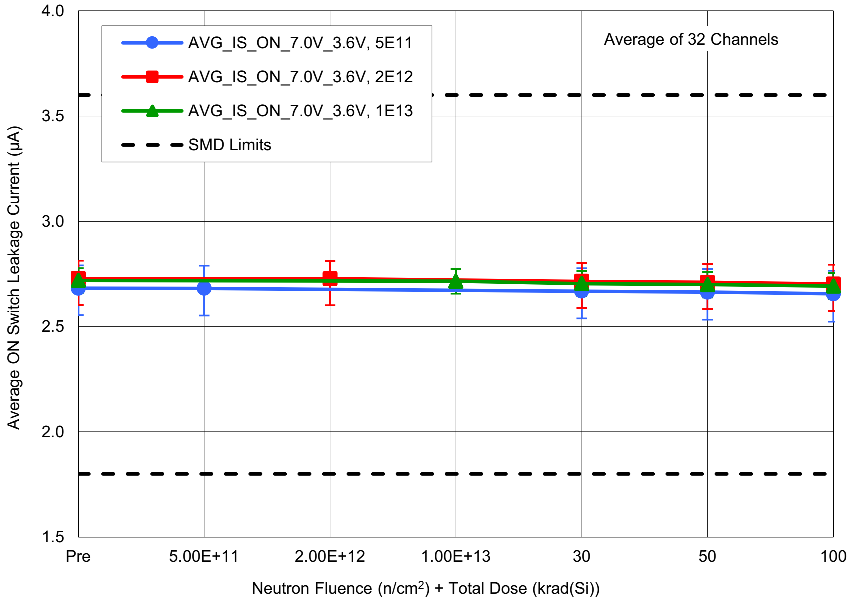


Figure 11. ISL71831SEH average switch ON input leakage with overvoltage applied to the input ($I_{IN(ON-0V)}$) with V+ = 3.6V, V_{IN} = 7.0V, and V_{OUT} = Open following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limits are a minimum of 1.8µA with a maximum of 3.6µA.

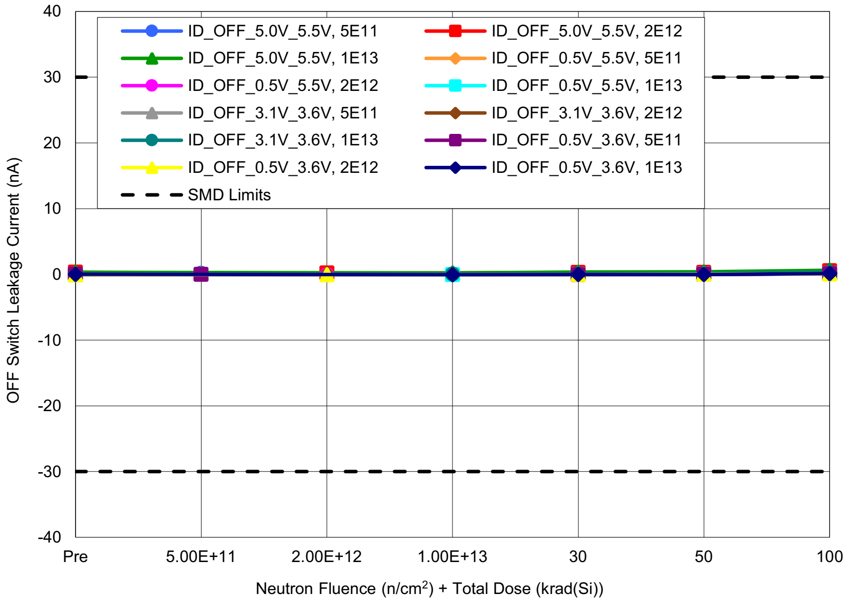


Figure 12. ISL71831SEH average switch output off leakage ($I_{OUT(OFF)}$) with V+ = 5.5V, V_{IN} = 5.0V, V_{OUT} = 0.5V, or V+ = 5.5V, V_{IN} = 0.5V, V_{OUT} = 5.0V, or V+ = 3.6V, V_{IN} = 3.1V, V_{OUT} = 0.5V, or V+ = 3.6V, V_{IN} = 0.5V, V_{OUT} = 3.1V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all channels. The post-TID irradiation SMD limits are a minimum of -30nA with a maximum of 30nA for both supply voltages.

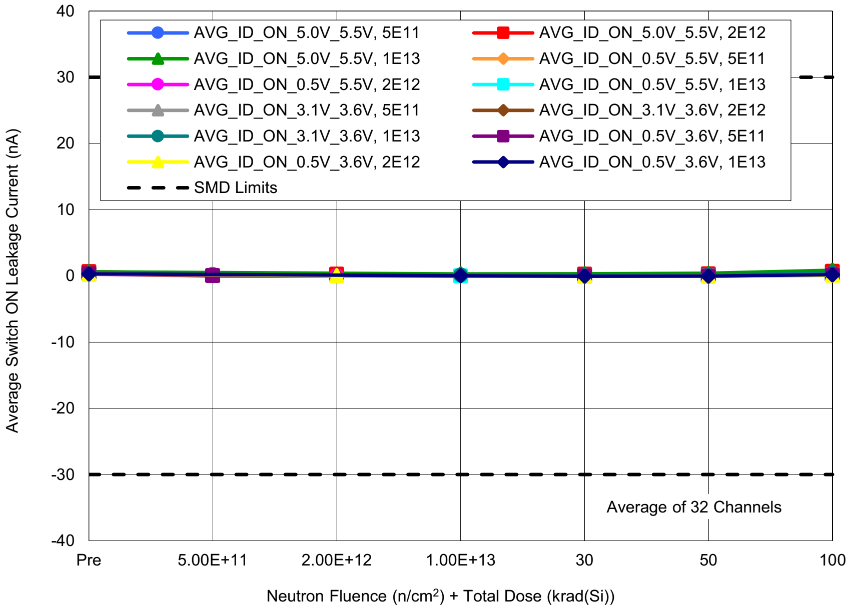


Figure 13. ISL71831SEH average switch output leakage with switch enabled (IOUT(ON)) with V+ = 5.5V, $V_{IN} = V_{OUT}$ = 5V, and all unused inputs at 0.5V, or V+ = 5.5V, $V_{IN} = V_{OUT}$ = 0.5V, and all unused inputs at 5V, or V+ = 3.6V, $V_{IN} = V_{OUT}$ = 3.1V, and all unused inputs at 0.5V, or V+ = 3.6V, $V_{IN} = V_{OUT}$ = 0.5V, and all unused inputs at 3.1V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all the channels. The post-TID irradiation SMD limits are a minimum of -30nA with a maximum for 30nA for both supply voltages.

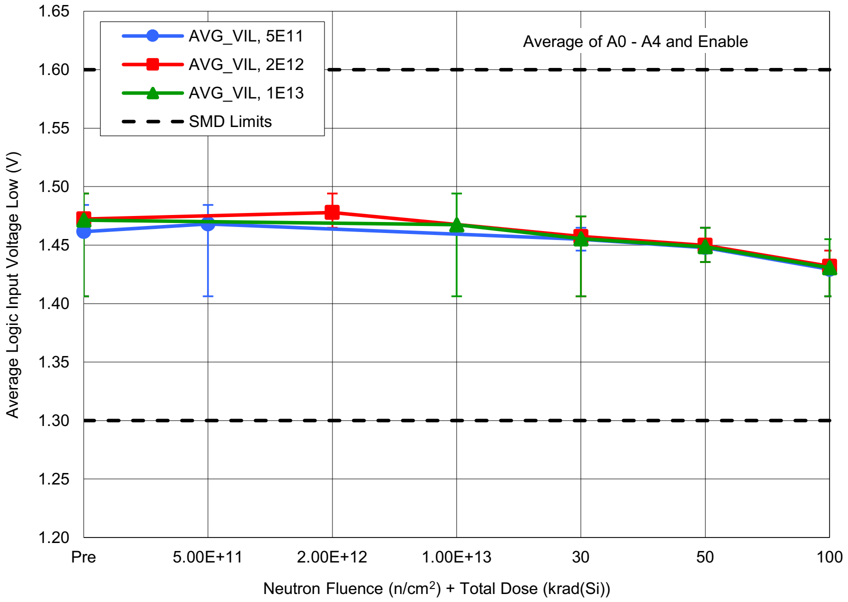


Figure 14. ISL71831SEH average logic input voltage low (V_{IL}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all pins. The post-TID irradiation SMD limits are a minimum of 1.3V with a maximum of 1.6V.

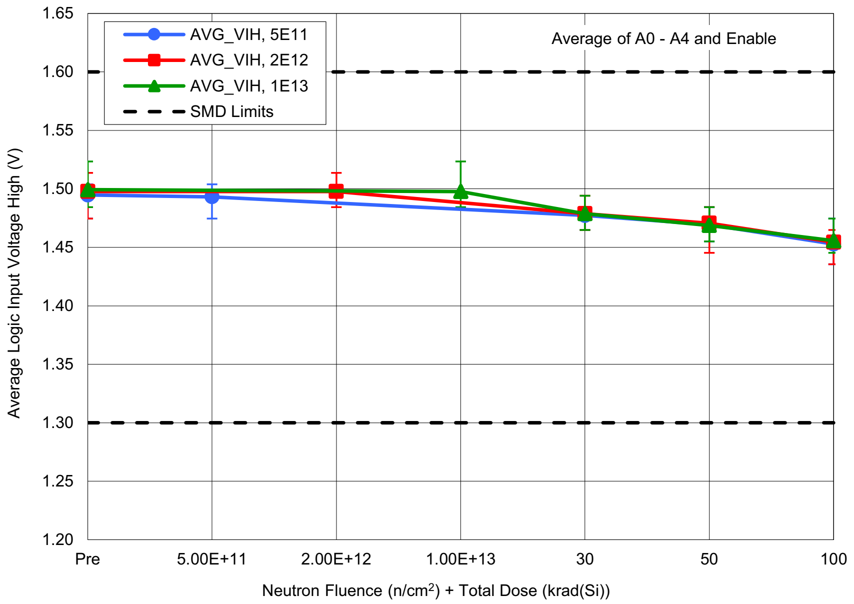


Figure 15. ISL71831SEH average logic input voltage high (V_{IH}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all pins. The post-TID irradiation SMD limits are a minimum of 1.3V with a maximum of 1.6V.

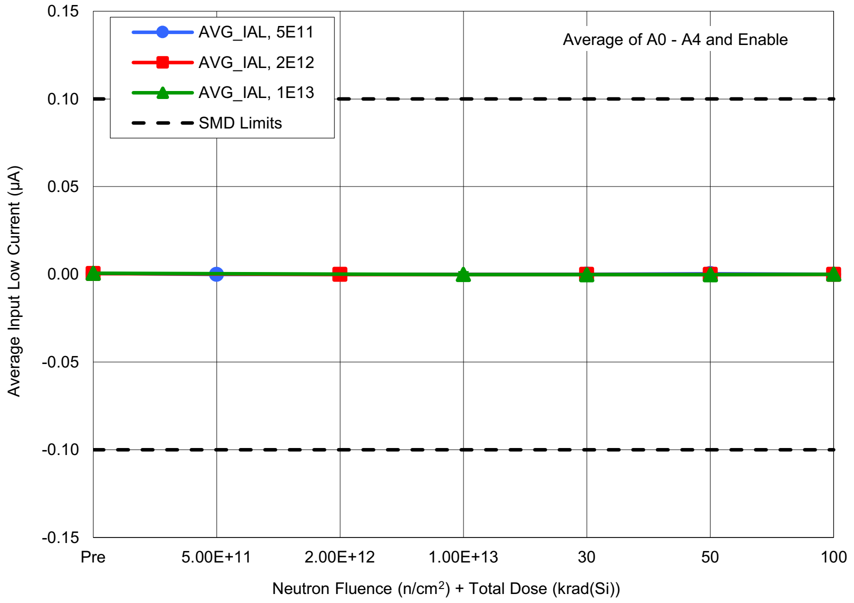


Figure 16. ISL71831SEH average input current with V_{AL}, V_{ENL} (I_{AL}, I_{ENL}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all pins. The post-TID irradiation SMD limits are a minimum of -0.1µA with a maximum of 0.1µA.

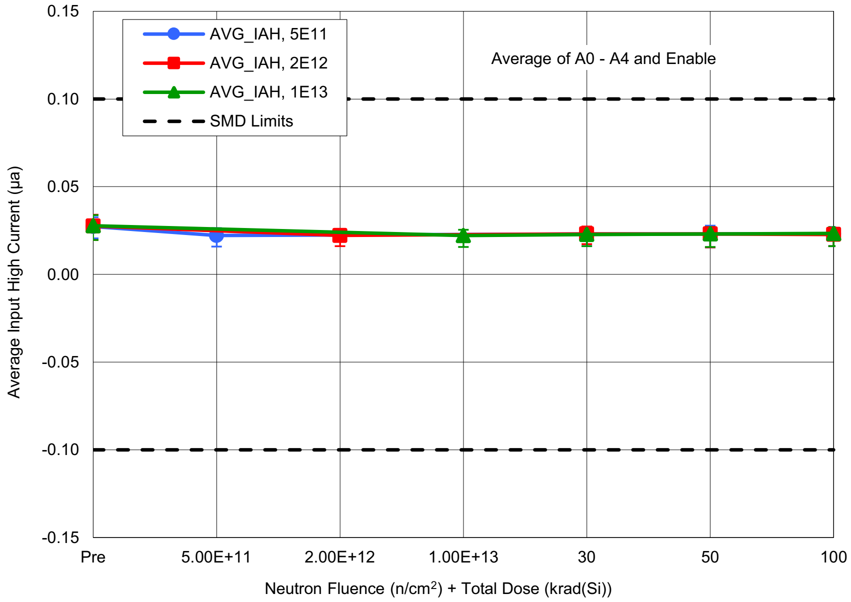


Figure 17. ISL71831SEH average input current with V_{AH}, V_{ENH} (I_{AH}, I_{ENH}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values across all pins. The post-TID irradiation SMD limits are a minimum of -0.1µA with a maximum of 0.1µA.

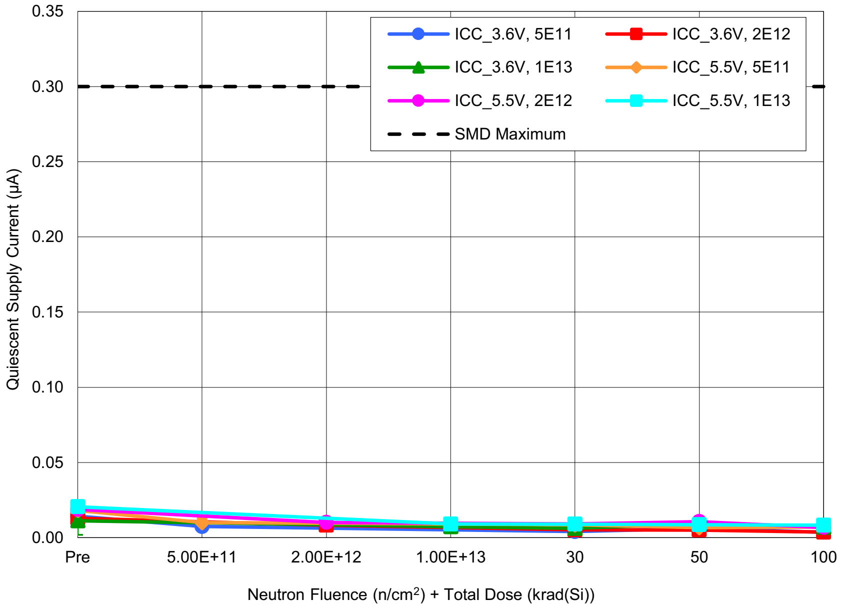


Figure 18. ISL71831SEH quiescent supply current (I_{SUPPLY}) with V+ = V_{REF} = 5.5V and 3.6V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post TID-irradiation SMD limit is a maximum of 0.3µA for both voltages.

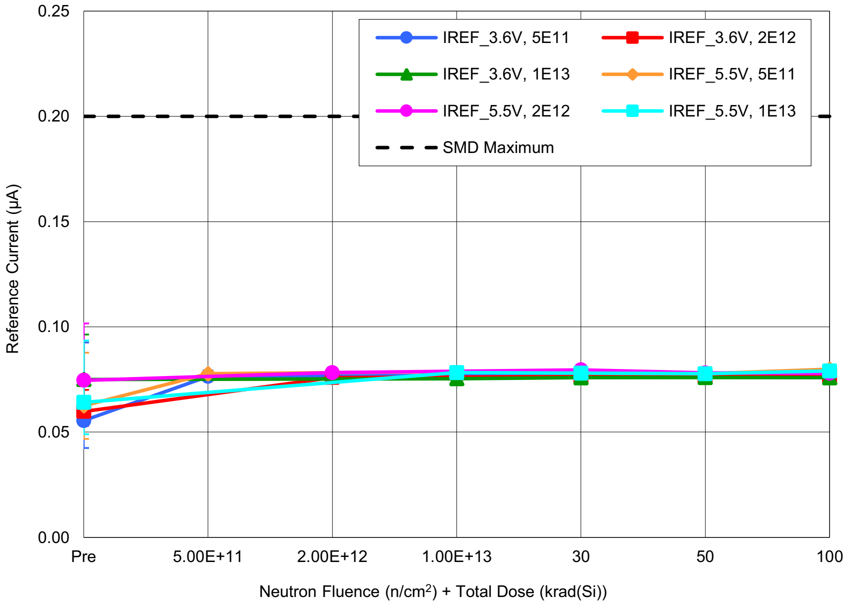


Figure 19. ISL71831SEH reference quiescent supply current (I_{REF}) with V+ = V_{REF} = 5.5V and 3.6V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 0.2µA for both voltages.

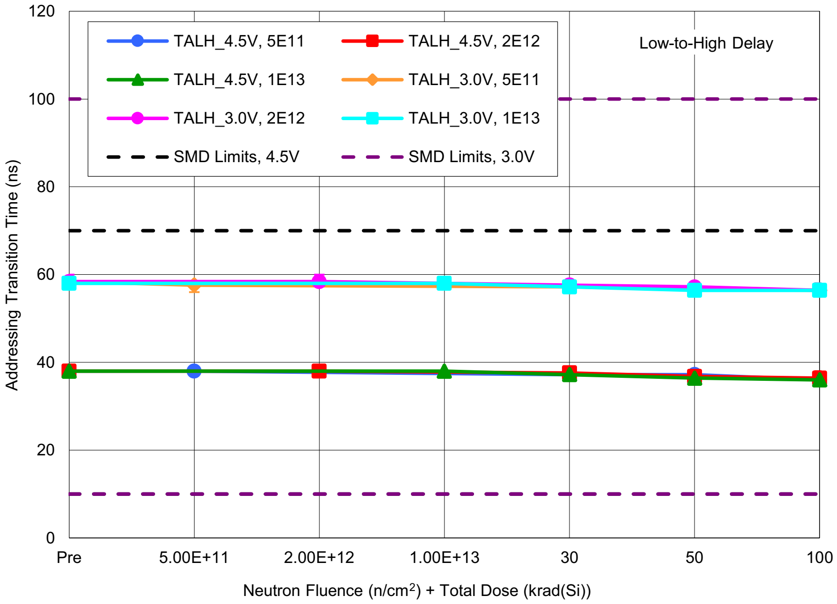


Figure 20. ISL71831SEH addressing transition time (Low to High) (t_{ALH}) with V+ = 4.5V and 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 10ns with a maximum of 70ns for a supply voltages of 4.5V, and a minimum of 10ns with a maximum of 100ns for a supply voltages of 3.0V.

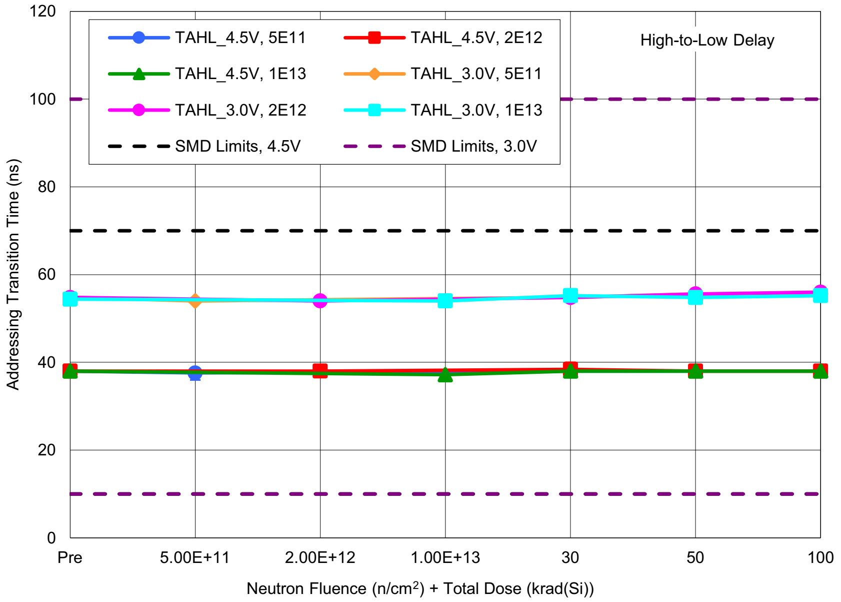


Figure 21. ISL71831SEH addressing transition time (High to Low) (t_{AHL}) with V+ = 4.5V, 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 10ns with a maximum of 70ns for a supply voltage of 4.5Vand a minimum of 10ns with a maximum of 100ns for a supply voltage of 3.0V.

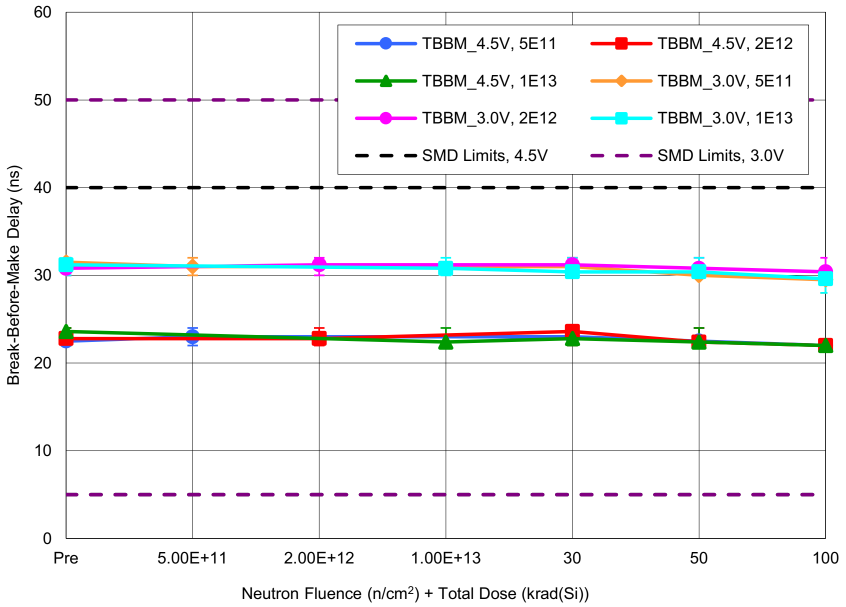


Figure 22. ISL71831SEH Break-Before-Make delay (t_{BBM}) with V+ = 4.5V and 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 5ns with a maximum of 40ns for a supply voltage of 4.5V, and a minimum of 5ns with a maximum of 50ns for a supply voltage of 3.0V.

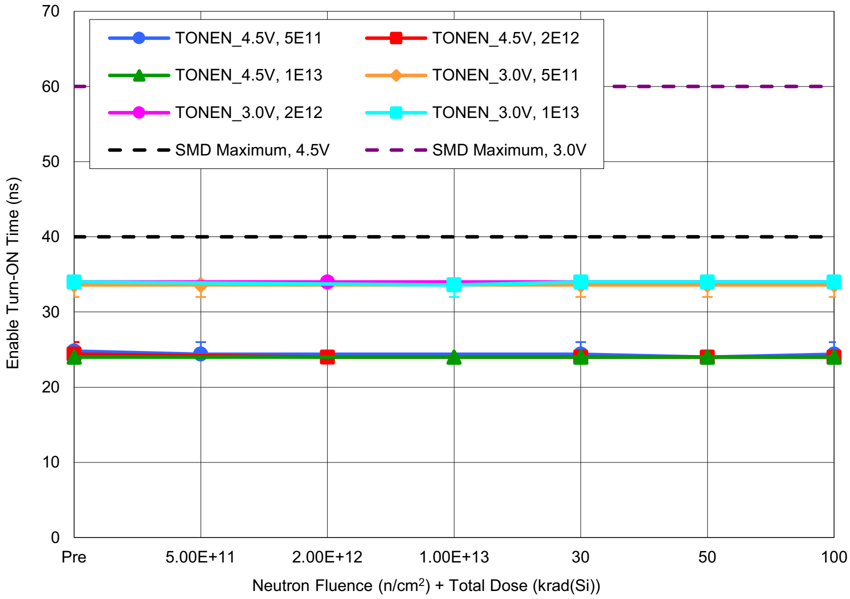


Figure 23. ISL71831SEH enable turn - ON time ($t_{EN(ON)}$) with V+ = 4.5V and 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are maximums of 40ns for a supply voltage of 4.5V, and 60ns for a supply voltages of 3.0V.

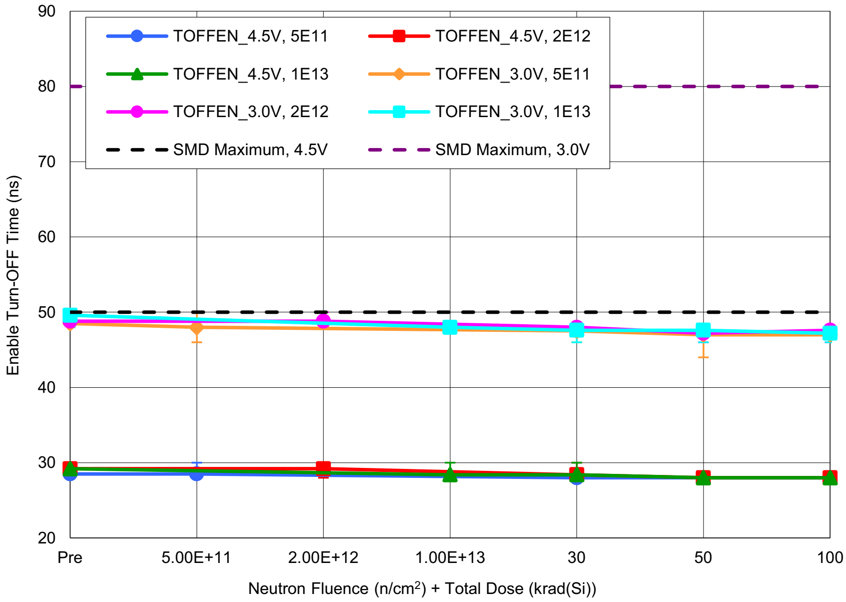


Figure 24. ISL71831SEH enable turn – OFF time ($t_{EN(OFF)}$) with V+ = 4.5V and 3.0V following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are maximums of 50ns for a supply voltage of 4.5V, and 80ns for a supply voltage of 3.0V

3. Discussion and Conclusion

This report summarizes results of combined 1MeV equivalent neutron testing and High Dose Rate (HDR) Total Ionizing Dose (TID) testing of the ISL71831SEH radiation tolerant 32-channel analog multiplexer. Parts were tested at actual fluences of 5.4×10^{11}n/cm^2, 2.1×10^{12}n/cm^2 and 1.1×10^{13}n/cm^2. Following neutron irradiation and testing, each set of samples underwent HDR TID testing. Each set of samples was irradiated under bias to 100krad(Si) with downpoints at 30krad(Si), 50krad(Si), and 100krad(Si). The results of key parameters before and after irradiation to each level are plotted in Figure 3 through Figure 24. The plots show the mean of each parameter as a function of neutron and total dose irradiation, with error bars that represent the minimum and maximum measured values. The figures also show the applicable electrical limits taken from the SMD, but it should be noted that these limits are provided for guidance only as the ISL71831SEH is not specified for the neutron environment.

All samples passed the post-irradiation SMD limits after all three neutron exposures up to and including 1.14×10^{13}n/cm^2 and after HDR irradiation through 100krad(Si). One sample, which was exposed to 5.38×10^{11}n/cm^2, experienced data corruption of three parameter measurements either during test datalogging or transferring the data to a spreadsheet as evidenced by the sample’s apparent return to normal functionality during the subsequent TID testing; those data were removed from switch ON-resistance match (Figure 4), Break-Before-Make delay (Figure 22), and enable turn-off time (Figure 24) measurements.

4. Revision History

Revision	Date	Description
1.00	Sep 7, 2022	Initial release.

Appendix

Table 3. Reported Parameters

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
3	Channel On-Resistance	$r_{DS(ON)}$	$V^+ = 3V$, $V_{IN} = 0V$ to V^+, $I_{OUT} = 1mA$	25	200	Ω
			$V^+ = 4.5V$, $V_{IN} = 0V$ to V^+, $I_{OUT} = 1mA$	15	120	
4	$r_{DS(ON)}$ Match between Channels	$\Delta r_{DS(ON)}$	$V^+ = 3V$ or $4.5V$, $V_{IN} = 0.5$, $I_{OUT} = 1mA$	-	5	Ω
5	On-Resistance Flatness	$r_{FLAT(ON)}$	$V^+ = 3.0V$, $V_{IN} = 0V$ to V^+	-	50	Ω
			$V^+ = 4.5V$, $V_{IN} = 0V$ to V^+		40	
6	Switch Input Off Leakage	$I_{IN(OFF)}$	$V^+ = 3.6V$, $V_{IN} = 3.1V$ or $0.5V$, Unused inputs and $V_{OUT} = 0.5V$ or $3.1V$	-30	30	nA
			$V^+ = 5.5V$, $V_{IN} = 5V$ or $0.5V$, Unused inputs and $V_{OUT} = 0.5V$ or $5V$			
7	Switch Input Off Overvoltage Leakage	$I_{IN(OFF-0V)}$	$V^+ = 3.6V$ or $5.5V$, $V_{IN} = 7V$, Unused inputs and $V_{OUT} = 0V$	-30	30	nA
8	Switch Input Off Leakage with Supply Voltage Grounded	$I_{IN(POWER-OFF)}$	$V_{IN} = 7V$, $V_{OUT} = 0V$, $V^+ = V_{EN} = V_{REF} = 0V$	-20	20	nA
9	Switch Input Off Leakage with Supply Voltage Open	$I_{IN(POWER-OFF)}$	$V_{IN} = 7V$, $V_{OUT} = 0V$, $V^+ = V_{EN} = V_{REF} =$ Open	-20	20	nA
10	Switch Input On Leakage with Overvoltage Applied to the Input	$I_{IN(ON-0V)}$	$V^+ = 5.5V$, $V_{IN} = 7V$, $V_{OUT} =$ Open	2.75	5.5	µA
11			$V^+ = 3.6V$, $V_{IN} = 7V$, $V_{OUT} =$ Open	1.8	3.6	
12	Switch Output Off Leakage	$I_{OUT(OFF)}$	$V^+ = 3.6V$, $V_{OUT} = 3.1V$ or $0.5V$, All inputs at 0.5V or 3.1V	-30	30	nA
			$V^+ = 5.5V$, $V_{OUT} = 5V$ or $0.5V$, All inputs at 0.5V or 5V			
13	Switch Output On Leakage with Switch Enabled	$I_{OUT(ON)}$	$V^+ = 3.6$, $V_{IN} = V_{OUT} = 3.1V$ or $0.5V$, All unused inputs at 0.5V or 3.1	-30	30	nA
			$V^+ = 5.5V$, $V_{IN} = V_{OUT} = 5V$ or 0.5, All unused inputs at 0.5V or 5V			
14	Logic Input Voltage Low	V_{IL}	$V^+ = 5.5V$, $V_{REF} = 3.3V$	1.3	1.6	V
15	Logic Input Voltage High	V_{IH}	$V^+ = 5.5V$, $V_{REF} = 3.3V$	1.3	1.6	V
16	Logic Input Current Low	I_{AL}, I_{ENL}	$V^+ = 5.5V$, $V_{REF} = 3.3V$	-100	100	nA
17	Logic Input Current High	I_{AH}, I_{ENH}	$V^+ = 5.5V$, $V_{EN} = V_A = V_{REF}$	-100	100	nA
18	Quiescent Supply Current	I_{SUPPLY}	$V^+ = V_{REF} = V_{EN} = 3.6V$ or $5.5V$	-	.3	µA
19	V_{REF} Supply Current	I_{REF}	$V^+ = V_{REF} = V_{EN} = 3.6V$ or $5.5V$, $V_A = 0V$	-	.2	µA
20	Addressing Transition Time (Low to High)	t_{ALH}	$V^+ = 3V$	10	100	ns
			$V^+ = 4.5V$		70	
21	Addressing Transition Time (High to Low)	t_{AHL}	$V^+ = 3V$	10	100	ns
			$V^+ = 4.5V$		70	

Table 3. Reported Parameters (Cont.)

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
22	Break-Before-Make Delay	t_{BBM}	$V^+ = 3V$	5	50	ns
			$V^+ = 4.5V$		40	
23	Enable Turn-On Time	$t_{EN(ON)}$	$V^+ = 3V$	-	60	ns
			$V^+ = 4.5V$		40	
24	Enable Turn-Off Time	$t_{EN(OFF)}$	$V^+ = 3V$	-	80	ns
			$V^+ = 4.5V$		50	

Related Information

For a list of related documents, visit our website:

- ISL71831SEH device page
- MIL-STD-883 test method 1017
- MIL-STD-883 test method 1019

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