ISL71710SLHM

LDR Testing Results of the ISL71710SLHM, Radiation Hardened Active-Input High Speed Digital Isolator

Introduction

This report documents the results of Low Dose Rate (LDR) total dose testing of the ISL71710SLHM, an active input digital signal isolator with CMOS output, that uses Giant Magnetoresistive (GMR) technology. The tests were conducted to provide an assessment of the total dose hardness of the part when exposed at a LDR and to provide an estimate of bias sensitivity. Parts were irradiated biased and unbiased at LDR (0.01rad(Si)/s) to 75krad(Si) level, which is the only TID rating for this part-type.

Related Information

- MIL-STD-883 Test Method 1019
- ISL71710SLHM Datasheet

Contents

1. Product Description

The Radiation Hardened ISL71710SLHM is an active input digital signal isolator with CMOS output, using Giant Magnetoresistive (GMR) technology for small size, high speed, and low power. The ISL71710SLHM is the fastest isolator of its type, with a 150Mbps typical data rate. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10ns and a pulse-width distortion as low as 0.3ns.

The ISL71710SLHM has unsurpassed common-mode transient immunity of 50kV/µs. It is ideal for isolating applications such as PROFIBUS, RS-485, and RS-422.

The ISL71710SLHM is offered in an 8 Ld 5mm x 4mm SOIC package and is fully specified across the military ambient temperature range of -55°C to +125°C. The functional block diagram is shown in Figure 1.

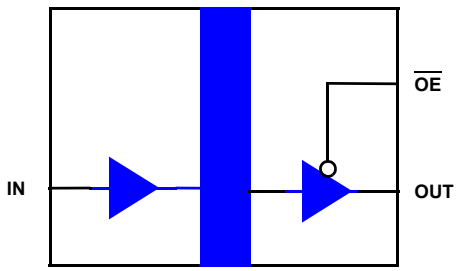

Figure 1. ISL71710SLHM Functional Block Diagram

The package outline and pin configuration for the ISL71710SLHM are shown in Figure 2 with the pin descriptions given in Table 1.

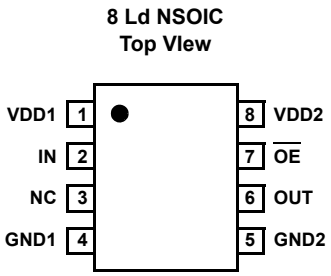

Figure 2. ISL71710SLHM Package and Pin Configuration

Table 1. ISL71710SLHM Pin Descriptions

Pin Number	Pin Name	Description
1	VDD1	Supply voltage
2	IN	Data in
3	NC	No internal connection. Leave this pin floating or connect it to VDD1 or GND1
4	GND1	Ground return for VDD1
5	GND2	Ground return for VDD2
6	OUT	Data output
7	$\overline{OE}$	Output enable, active low. Internally pulled low with 100kΩ to enable the output when this pin is not connected.
8	VDD2	Supply voltage

2. Test Description

2.1 Irradiation Facilities

The irradiation was performed at 0.01rad(Si)/s using the Renesas Palm Bay Hopewell Designs N40 panoramic commercial irradiator. This irradiator uses PbAl spectrum hardening filters to shield the test board and devices under test against low energy secondary gamma radiation.

2.2 Test Fixturing

Figure 3 shows the configuration used for biased irradiation.

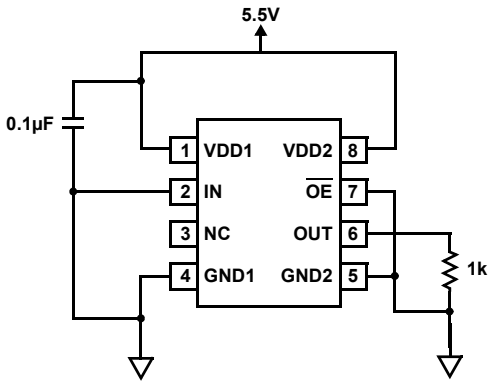

Figure 3. ISL71710SLHM TID Bias Schematic

2.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator, using production automated test equipment (ATE) with datalogging at each downpoint.

2.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 10 samples irradiated under bias and 12 samples irradiated with all pins grounded. Two units were removed from the biased samples because of socket issues resulting in non-valid data.

The twenty-four ISL71710SLHM samples were drawn equally from wafer lots 171618-04, 171618-05, and 171618-06. All samples were packaged in the standard 8 Ld NSOIC package. Samples were processed through the standard burn-in cycle before irradiation.

2.5 Downpoints

Downpoints for the tests were 0krad(Si), 10krad(Si), 30krad(Si), 50krad(Si), and 75krad(Si).

3. Test Results

3.1 Attributes Data

Total dose testing of the ISL71710SLHM was completed. All tested parameters passed the datasheet limits. Table 2 summarizes the results.

Table 2. ISL71710SLHM Total Dose Test Attributes Data

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass[1]	Fail
0.01	Biased (Figure 3)	10[2]	Pre-irradiation	10	
			10krad(Si)	10	0
			30krad(Si)	10	0
			50krad(Si)	10	0
			75krad(Si)	10	0
0.01	GND	12	Pre-irradiation	12	
			10krad(Si)	12	0
			30krad(Si)	12	0
			50krad(Si)	12	0
			75krad(Si)	12	0

1. A pass indicates a sample that passes all post-irradiation datasheet limits.
2. Two biased samples were removed because of socket issues and non-valid data.

3.2 Key Parameter Variables Data

The plots in Figure 4 through Figure 18 illustrate the TID response of selected parameters as shown in Table 3. The plots show the average tested values of the key parameters as a function of total dose for both conditions, biased and grounded. The plots also include error bars at each downpoint, representing the minimum and maximum measured values of the samples, although in some plots the error bars are not visible because of their values compared to the scale of the graph.

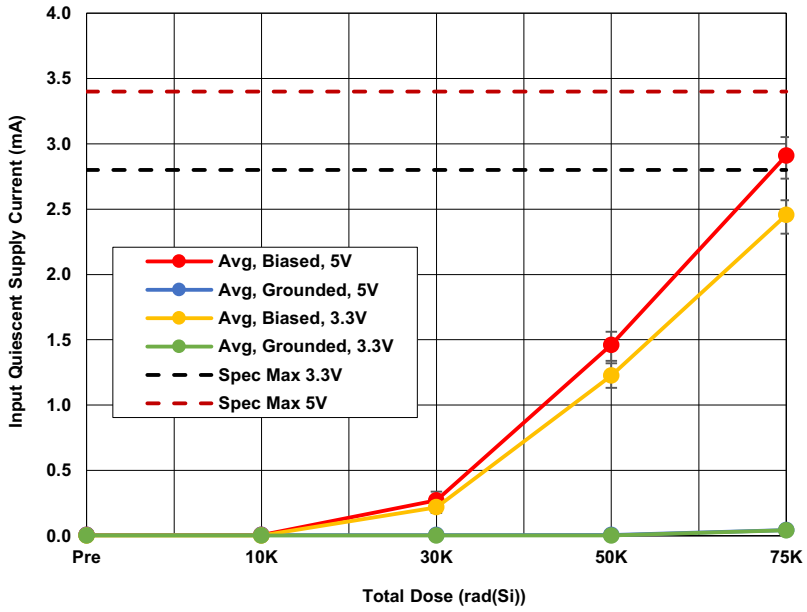

Figure 4. ISL71710SLHM input quiescent supply current (I_{DD1}) with V_{DD1} = V_{DD2} = 3.3V and 5V as a function of LDR irradiation. The error bars represent the minimum and maximum measured values. The datasheet limits are 2.8mA maximum at 3.3V and 3.4mA maximum at 5V.

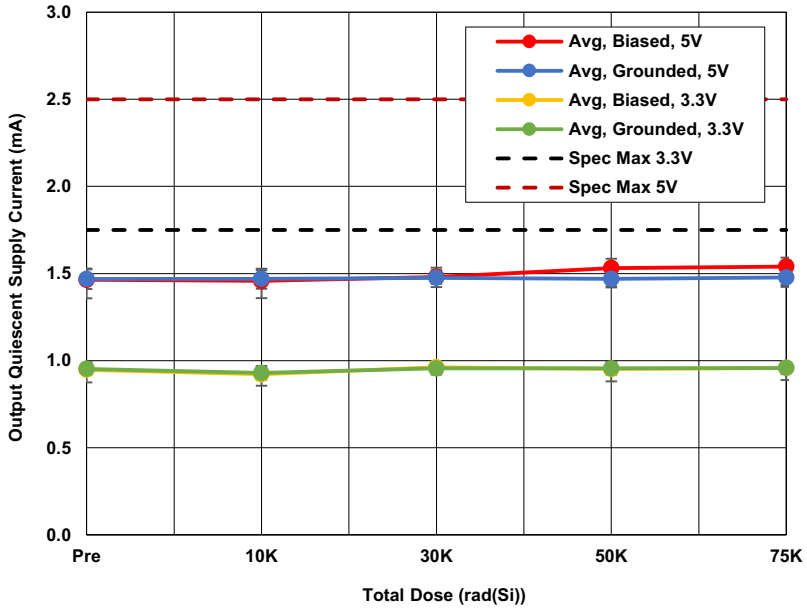

Figure 5. ISL71710SLHM average output quiescent supply current (I_{DD2}) with V_{DD1} = V_{DD2} = 3.3V and 5V as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 1.75mA maximum at 3.3V and 2.5mA maximum at 5V.

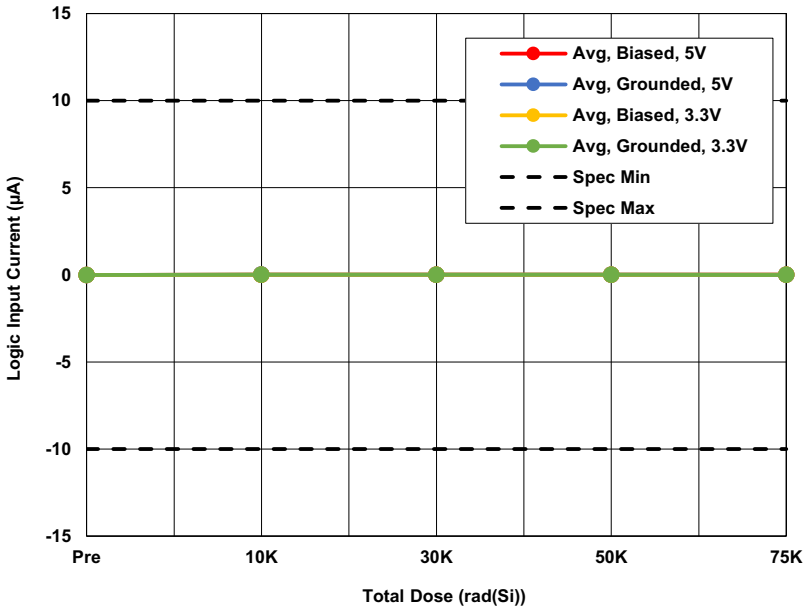

Figure 6. ISL71710SLHM logic input current (I_I) with V_{DD1} = V_{DD2} = 3.3V and 5V as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are -10µA minimum and 10µA maximum.

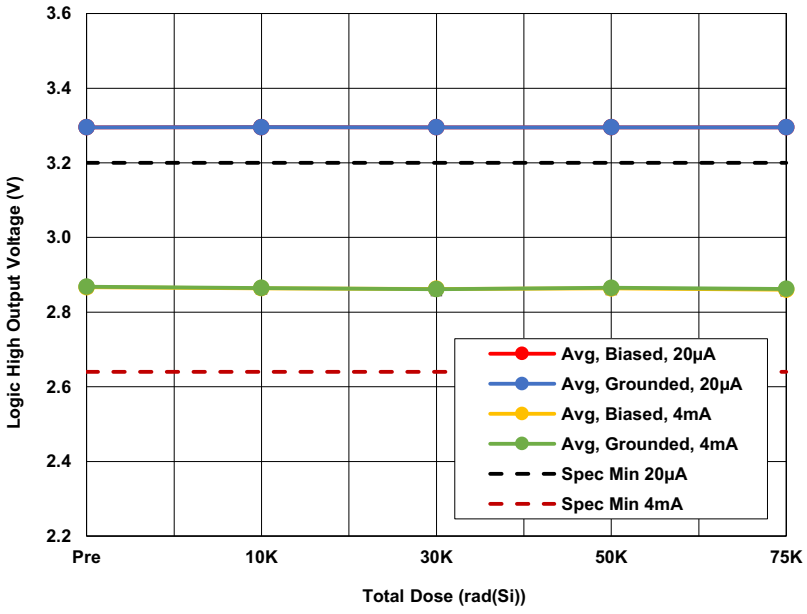

Figure 7. ISL71710SLHM average logic high output voltage (V_{OH}) with V_{DD1} = V_{DD2} = 3.3V and I_O = -20µA and -4mA as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 3.2V minimum for -20µA and 2.64V minimum for -4mA.

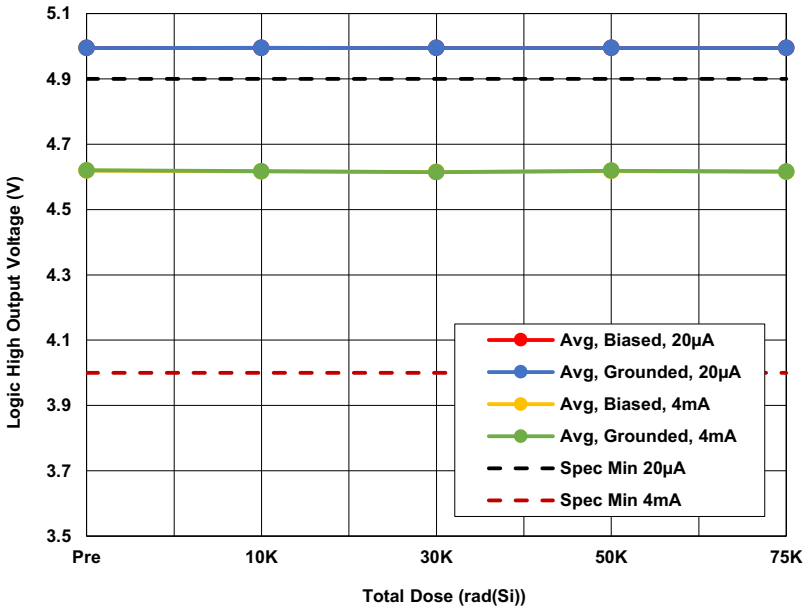

Figure 8. ISL71710SLHM average logic high output voltage (V_{OH}) with V_{DD1} = V_{DD2} = 5V and I_O = -20µA and -4mA as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 4.9V minimum for -20µA and 4V minimum for -4mA.

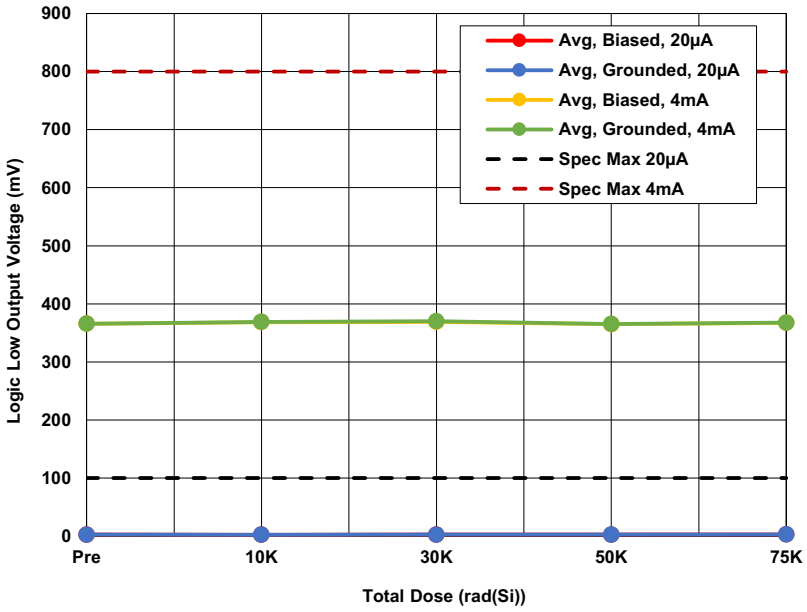

Figure 9. ISL71710SLHM average logic low output voltage (V_{OL}) with V_{DD1} = V_{DD2} = 3.3V and I_O = 20µA and 4mA as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 800mV maximum for 20µA and 100mV maximum for 4mA.

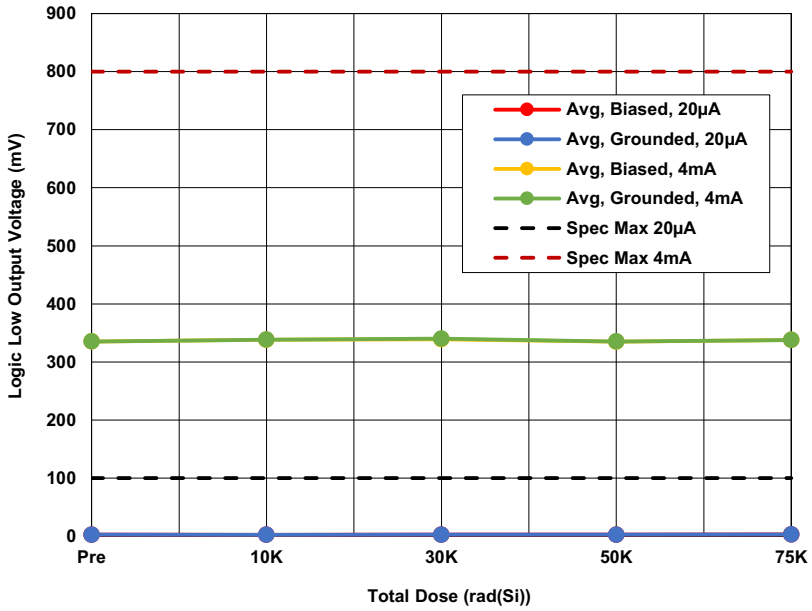

Figure 10. ISL71710SLHM average logic low output voltage (V_{OL}) with V_{DD1} = V_{DD2} = 5V and I_O = 20µA and 4mA as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 800mV maximum for 20µA and 100mV maximum for 4mA.

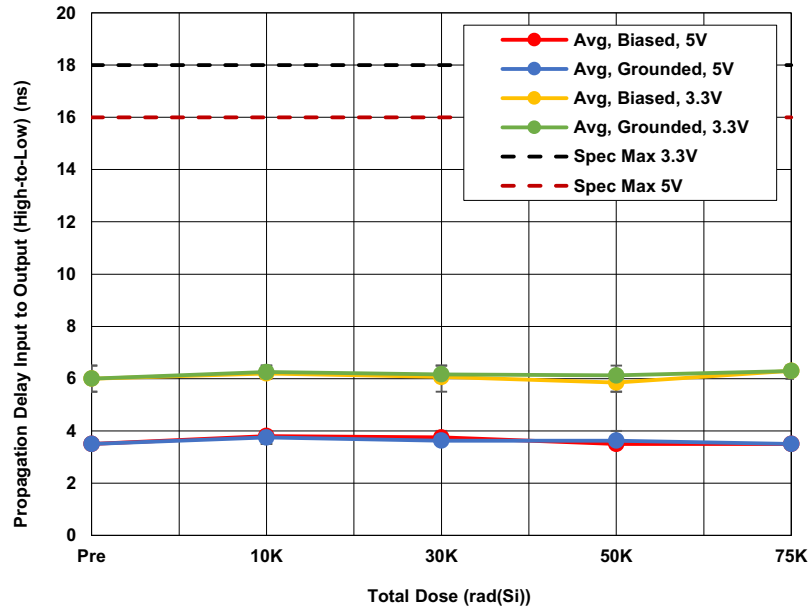

Figure 11. ISL71710SLHM average propagation delay, input to output, high to low (t_{PHL}) with V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 18ns maximum for 3.3V and 16ns maximum for 5V.

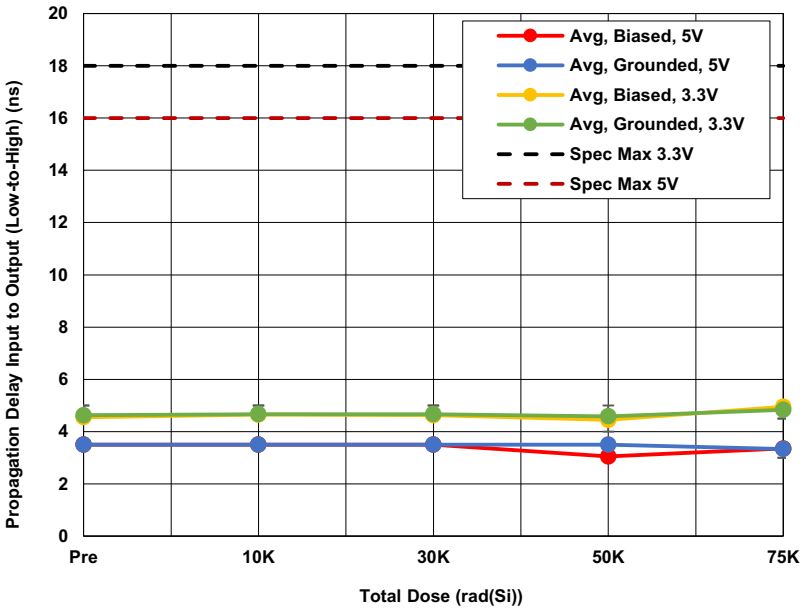

Figure 12. ISL71710SLHM average propagation delay, input to output, low to high (t_{PLH}) with V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 18ns maximum for 3.3V and 16ns maximum for 5V.

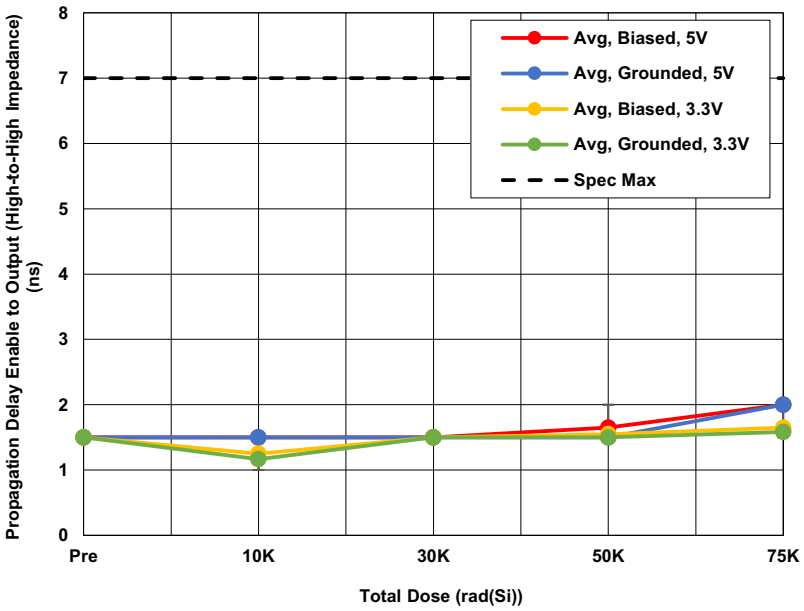

Figure 13. ISL71710SLHM average propagation delay, enable to output, high-to-high impedance (t_{PHZ}) with V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limit is 7ns maximum.

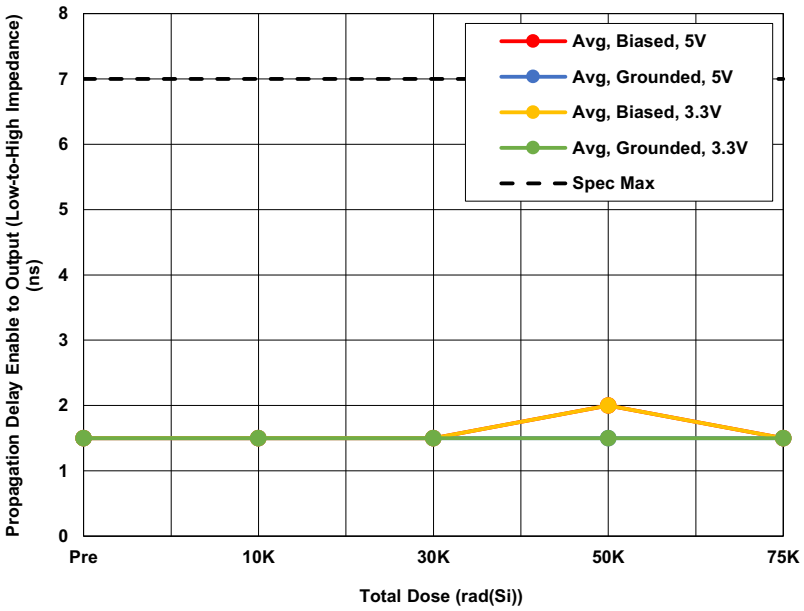

Figure 14. ISL71710SLHM average propagation delay, enable to output, low-to-high impedance (t_{PLZ}) with $V_{DD1} = V_{DD2} = 3.3V$ and 5V, $C_L = 15pF$ as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limit is 7ns maximum.

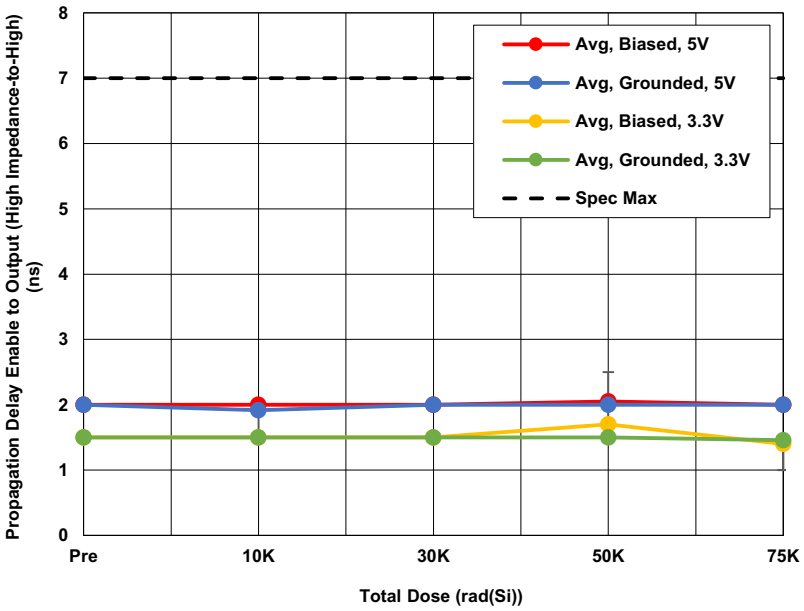

Figure 15. ISL71710SLHM average propagation delay, enable to output, high impedance-to-high (t_{PZH}) with $V_{DD1} = V_{DD2} = 3.3V$ and 5V, $C_L = 15pF$ as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limit is 7ns maximum.

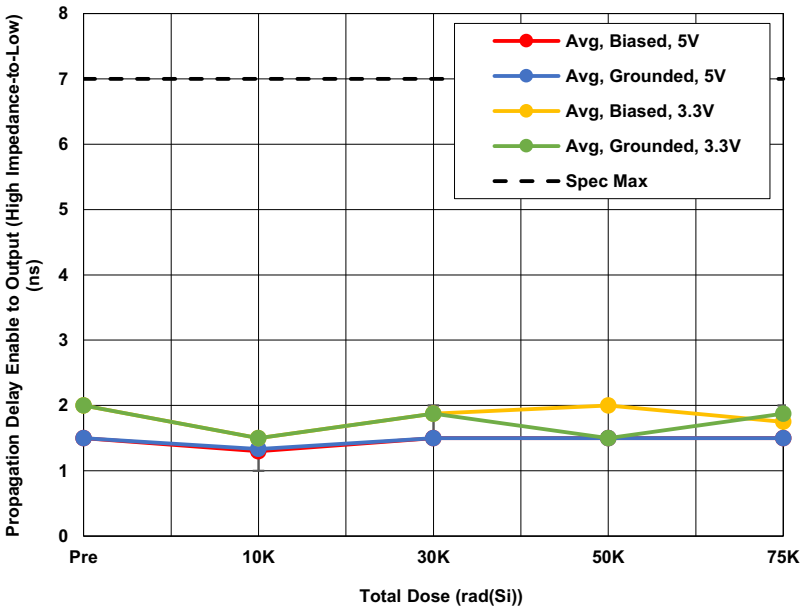

Figure 16. ISL71710SLHM average propagation delay, enable to output, high impedance-to-low (t_{PZL}) with V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limit is 7ns maximum.

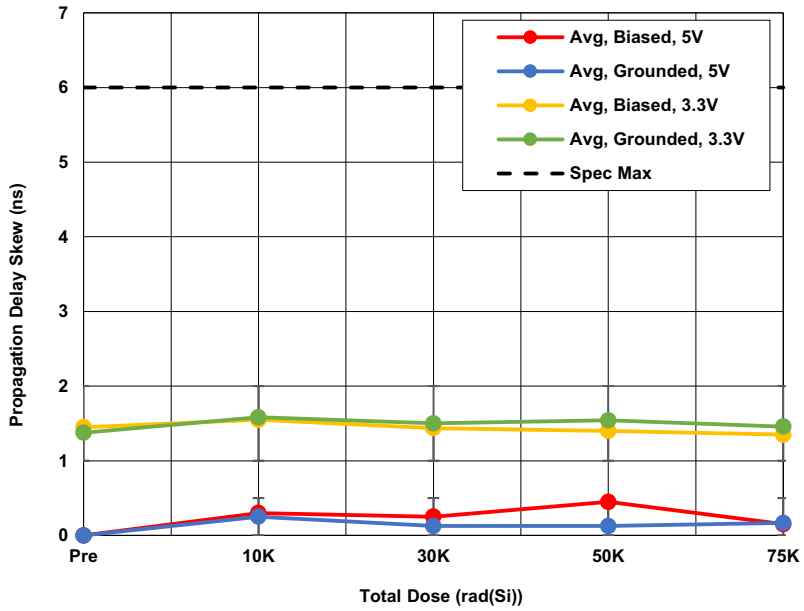

Figure 17. ISL71710SLHM average propagation delay skew (t_{PSK}) with V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limit is 6ns maximum.

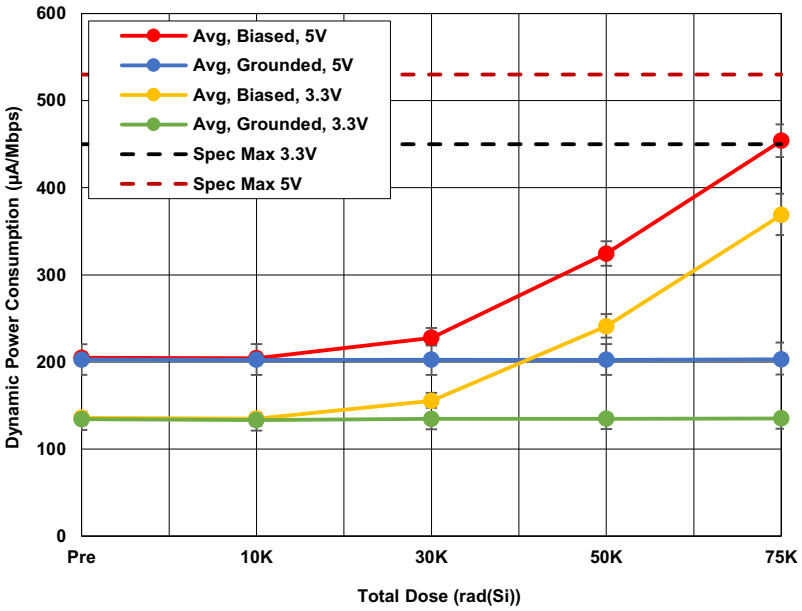

Figure 18. ISL71710SLHM average dynamic power consumption with V_{DD1} = V_{DD2} = 3.3V and 5V as a function of LDR irradiation. The error bars, if visible, represent the minimum and maximum measured values. The datasheet limits are 450 µA/Mbps maximum for 3.3V and 530µA/Mbps maximum for 5V.

4. Discussion and Conclusion

We reported the results of LDR total dose testing of the ISL71710SLHM radiation hardened active-input high speed digital isolator. The irradiation consisted of 10 biased and 12 grounded samples to 75krad(Si). All datasheet parameters passed at all downpoints. The only evidence of bias dependence was observed in the input quiescent supply current, as shown in Figure 4, and the dynamic power consumption, illustrated in Figure 18. The biased conditions for both parameters showed a significant increase after 10krad(Si) and they were continuing to increase at 75krad(Si). The increase of both parameters under bias is understandable, as both are dependent on the radiation-induced leakage of the CMOS input circuitry of the part. Although the current increases, neither functionality or any other parameters are not affected.

5. Revision History

Revision	Date	Description
1.0	Jun 24, 2021	Initial release

Appendix: Reported Parameters

Table 3 lists the key parameters that are considered indicative of part performance. These parameters are plotted in Figure 4 through Figure 18. All limits are taken from the ISL71710SLHM datasheet.

Table 3. ISL71710SLHM Key Total Dose Parameters (T_A = 25°C)

Figure	Parameter	Symbol	Conditions	Low Limit	High Limit	Unit
4	Input Quiescent Supply Current	I_{DD1}	V_{DD1} = V_{DD2} = 3.3V		2.8	mA
			V_{DD1} = V_{DD2} = 5V		3.4	mA
5	Output Quiescent Supply Current	I_{DD2}	V_{DD1} = V_{DD2} = 3.3V		1.75	mA
			V_{DD1} = V_{DD2} = 5V		2.5	mA
6	Logic Input Current	I_I	V_{DD1} = V_{DD2} = 3.3V and 5V	-10	10	µA
7	Logic High Output Voltage (V_{DD1} = V_{DD2} = 3.3V)	V_{OH}	I_O = -20µA	3.2		V
			I_O = -4mA	2.64		V
8	Logic High Output Voltage (V_{DD1} = V_{DD2} = 5V)		I_O = -20µA	4.9		V
			I_O = -4mA	4		V
9	Logic Low Output Voltage (V_{DD1} = V_{DD2} = 3.3V)	V_{OL}	I_O = 20µA		100	mV
			I_O = 4mA		800	mV
10	Logic Low Output Voltage (V_{DD1} = V_{DD2} = 5V)		I_O = 20µA		100	mV
			I_O = 4mA		800	mV
11	Propagation Delay Input to Output (High-to-Low)	t_{PHL}	V_{DD1} = V_{DD2} = 3.3V, C_L = 15pF		18	ns
			V_{DD1} = V_{DD2} = 5V, C_L = 15pF		16	ns
12	Propagation Delay Input to Output (Low-to-High)	t_{PLH}	V_{DD1} = V_{DD2} = 3.3V, C_L = 15pF		18	ns
			V_{DD1} = V_{DD2} = 5V, C_L = 15pF		16	ns
13	Propagation Delay Enable to Output (High-to-High Impedance)	t_{PHZ}	V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF		7	ns
14	Propagation Delay Enable to Output (Low-to-High Impedance)	t_{PLZ}	V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF		7	ns
15	Propagation Delay Enable to Output (High Impedance-to-High)	t_{PZH}	V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF		7	ns
16	Propagation Delay Enable to Output (High Impedance-to-Low)	t_{PZL}	V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF		7	ns
17	Propagation Delay Skew	t_{PSK}	V_{DD1} = V_{DD2} = 3.3V and 5V, C_L = 15pF		6	ns
18	Dynamic Power Consumption		V_{DD1} = V_{DD2} = 3.3V		450	µA/Mbps
			V_{DD1} = V_{DD2} = 5V		530	µA/Mbps

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(Rev.1.0 Mar 2020)

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