ISL70100SEH, ISL73100SEH

Total Dose Test Report

Introduction

This document reports the results of the Low Dose Rate (LDR) and High Dose Rate (HDR) total dose testing and subsequent high temperature biased annealing of the ISL70100SEH and ISL73100SEH (ISL7x100SEH) current sense amplifiers. The tests were conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of dose rate, bias or anneal sensitivity. Parts were irradiated biased and unbiased at LDR and HDR. The ISL70100SEH is rated at 100krad(Si) at HDR (50 – 300rad(Si)/s) and at 75krad(Si) at LDR (0.01rad(Si)/s). The ISL73100SEH is rated at 75krad(Si) at LDR (0.01rad(Si)/s). Both part types are acceptance tested on a lot-by-lot basis to these limits.

Related Literature

For a full list of related documents, visit our website:

- ISL70100SEH, ISL73100SEH device pages
- MIL-STD-883 Test Method 1019

Product Description

The ISL7x100SEH are radiation hardened 40V current sense amplifiers built on the proprietary PR40 SOI process and have a wide power supply range that starts at 2.7V and goes up to 40V. The common-mode input range is independent of the supply voltage and extends from -0.3V to 40.0V, making them ideal to use in both high-side and low-side applications.

The ISL7x100SEH are transconductance amplifiers that monitor current through an external sense resistor and output a current proportional to the sensed voltage. The overall gain is adjustable with a single resistor from output to ground.

These amplifiers have an extremely low offset voltage and input bias currents making them ideal for precision applications. They have a bandwidth of 500kHz with a slew rate of 500μ A/µs, making them useful for current feedback in telemetry applications. When the parts are powered down (V+ = V- = 0V), the sense pins (RS+, RS-) are high impedance to avoid loading the monitored circuit.

The parts are available in a hermetically sealed 10 Ld ceramic flat-pack package or die form and operate across the full-range military temperature of -55°C to +125°C.

The pinout for the ISL7x100SEH is shown in Figure 1 with the pin descriptions shown in Table 1.

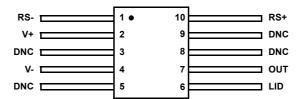


Figure 1. ISL7x100SEH Package and Pin Configuration

 Table 1.
 ISL7x100SEH Pin Descriptions

Pin Number	Pin Name	Description
1	RS-	Negative sense input of current sense amplifier
2	V+	Positive power supply
3	DNC	Do not connect, leave floating. This pin leaks to V-
4	V-	Negative power supply

Pin Number	Pin Name	Description	
5	DNC	Do not connect, leave floating. This pin leaks to V-	
6	LID	Electrically connected to the lid, connect this pin to V- to avoid floating metal	
7	OUT	aled output of the input differential (current out for ADJ version and voltage out for fixed)	
8	DNC	Do not connect, leave floating. This pin leaks to V-	
9	DNC	o not connect, leave floating. This pin leaks to V-	
10	RS+	Positive sense input of current sense amplifier	

Table 1. ISL7x100SEH Pin Descriptions (Continued)

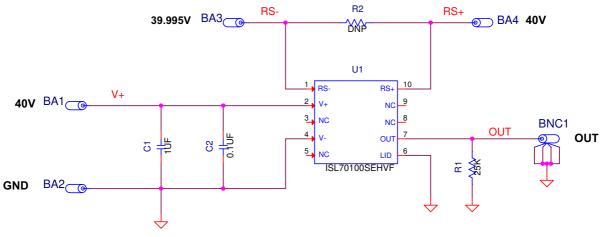
1. Test Description

1.1 Irradiation Facilities

HDR testing was performed at 187.2rad(Si)/s using a Gammacell 220 commercial irradiator located in the Palm Bay, Florida Renesas facility. LDR testing was performed at 0.01rad(Si)/s using the Renesas Palm Bay Hopewell Designs N40 panoramic commercial irradiator. Both irradiators use PbAI spectrum hardening filters to shield the test board and devices under test against low energy secondary gamma radiation. Biased irradiation and annealing were performed on all samples following irradiation at 100°C for 168 hours in a small temperature chamber.

1.2 Test Fixturing

Figure 2 shows the configurations used for biased irradiation at both dose rates.





1.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator, using production Automated Test Equipment (ATE) with data logging at each downpoint.

1.4 Experimental Matrix

Irradiation was performed following the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 12 samples irradiated at LDR under bias, 12 samples irradiated at LDR with all pins grounded, bias, 6 samples irradiated at HDR under bias, and 6 samples irradiated at HDR with all pins grounded. At anneal all samples were biased. Two control units were used.

The ISL7x100SEH samples were drawn from wafer lot XHA0LB. All samples were packaged in a 10 Ld hermetic flatpack (package code K10.A). Samples were processed through the standard burn-in cycle before irradiation.

1.5 Downpoints

Downpoints for the LDR tests were 0, 10, 30, 50, 75, and 100krad(Si). Downpoints for the HDR tests were 0, 30, 50, 75, 100, and 150krad(Si). All irradiations were followed by a 168-hour high temperature anneal at 100°C under bias, as described in <u>Experimental Matrix</u>.

2. Test Results

2.1 Attributes Data

Total dose testing of the ISL7x100SEH is complete. All tested parameters passed the post-irradiation SMD limits. <u>Table 2</u> summarizes the results.

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass (<u>Note 1</u>)	Fail
0.01	Biased	12	Pre-irradiation	12	
	(<u>Figure 2</u>)		10krad(Si)	12	0
			30krad(Si)	12	0
			50krad(Si)	12	0
			75krad(Si)	12	0
			100krad(Si)	12	0
			Anneal	12	0
0.01	GND	12	Pre-irradiation	12	
			10krad(Si)	12	0
			30krad(Si)	12	0
			50krad(Si)	12	0
			75krad(Si)	12	0
			100krad(Si)	12	0
			Anneal	12	0
187.2	Biased 6		Pre-irradiation	6	
	(<u>Figure 2</u>)		30krad(Si)	6	0
			50krad(Si)	6	0
			75krad(Si)	6	0
			100krad(Si)	6	0
			150krad(Si)	6	0
			Anneal	6	0
187.2	GND	6	Pre-irradiation	6	
			30krad(Si)	6	0
			50krad(Si)	6	0
			75krad(Si)	6	0
			100krad(Si)	6	0
			150krad(Si)	6	0
			Anneal	6	0

Note:

1. Pass indicates a sample that passes all post-irradiation SMD limits.

2.2 Key Parameter Variables Data

The plots in Figures 3 through 45 show the TID response of selected SMD parameters listed in Table 3. The plots show the average tested values of the key parameters as a function of total dose for both conditions, biased and GND at HDR and LDR. For example, the legend that includes LDR_Bias indicates the average LDR response for biased samples. PA_L on the graphs stands for Post-Anneal Low Dose and PA_H represents the Post-Anneal High Dose results. The plots also include error bars at each downpoint, representing the minimum and maximum measured values of the samples; however, in some plots the error bars are not visible due to their values compared to the scale of the graph.

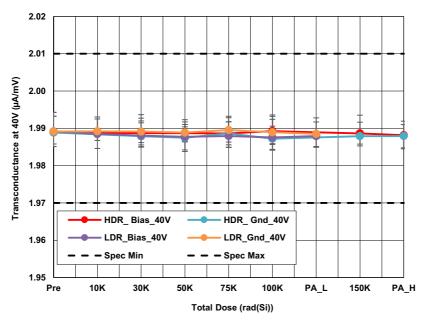


Figure 3. ISL7x100SEH transconductance (g_m) with V+ = 40V, V_{RS+} = 40V, and V_{SEN} = 25mV to 150mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 1.970µA/mV minimum and 2.010µA/mV maximum.

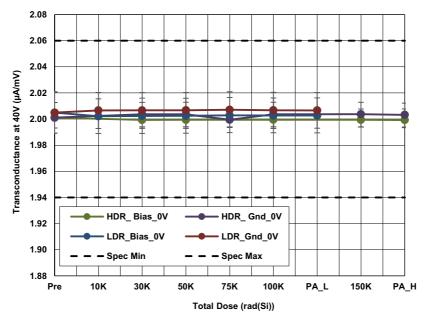


Figure 4. ISL7x100SEH transconductance (g_m) with V+ = 40V, V_{RS+} = 0V, and V_{SEN} = 25mV to 150mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 1.940µA/mV minimum and 2.060µA/mV maximum.

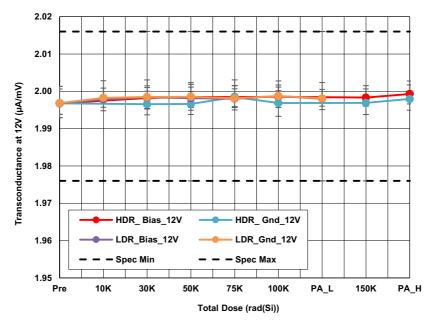


Figure 5. ISL7x100SEH transconductance (g_m) with V+ = 12V, V_{RS+} = 12V, and V_{SEN} = 25mV to 150mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 1.976µA/mV minimum and 2.016µA/mV maximum.

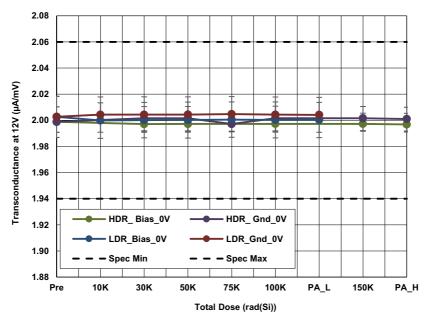


Figure 6. ISL7x100SEH transconductance (g_m) with V+ = 12V, V_{RS+} = 0V, and V_{SEN} = 25mV to 150mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 1.940µA/mV minimum and 2.060µA/mV maximum.

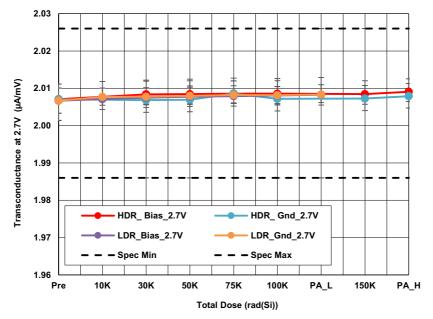


Figure 7. ISL7x100SEH transconductance (g_m) with V+ = 2.7V, V_{RS+} = 2.7V, and V_{SEN} = 25mV to 150mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 1.986µA/mV minimum and 2.026µA/mV maximum.

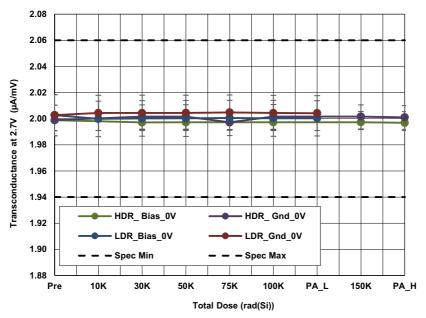


Figure 8. ISL7x100SEH transconductance (g_m) with V+ = 2.7V, V_{RS+} = 0V, and V_{SEN} = 25mV to 150mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 1.940µA/mV minimum and 2.060µA/mV maximum.

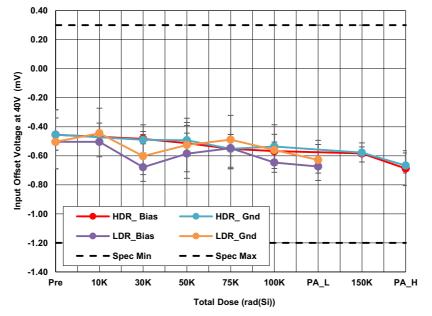


Figure 9. ISL7x100SEH input offset voltage (V_{OS}) with V+ = 40V, V_{RS+} = 40V and V_{SEN} = 5mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are -1200µV minimum and 300µV maximum.

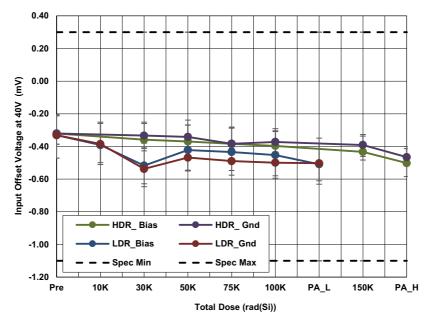


Figure 10. ISL7x100SEH input offset voltage (V_{OS}) with V+ = 40V, V_{RS+} = 0V and V_{SEN} = 5mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are -1100µV minimum and 300µV maximum.

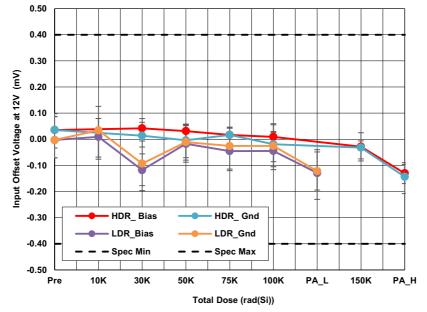


Figure 11. ISL7x100SEH input offset voltage (V_{OS}) with V+ = 12V, V_{RS+} = 12V and V_{SEN} = 5mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are -400µV minimum and 400µV maximum.

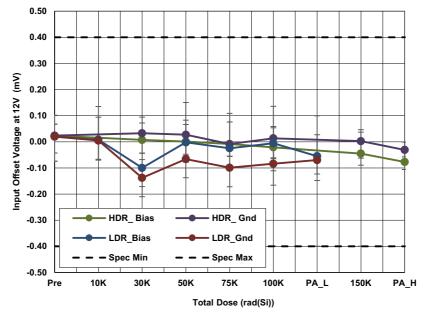


Figure 12. ISL7x100SEH input offset voltage (V_{OS}) with V+ = 12V, V_{RS+} = 0V and V_{SEN} = 5mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are -400µV minimum and 400µV maximum.

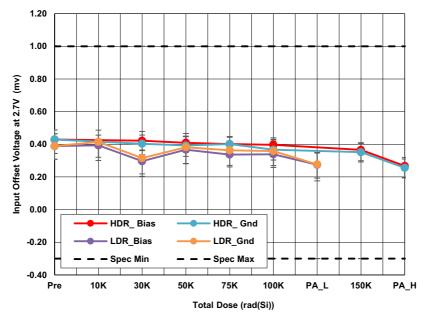


Figure 13. ISL7x100SEH input offset voltage (V_{OS}) with V+ = 2.7V, V_{RS+} = 2.7V and V_{SEN} = 5mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are -300µV minimum and 1000µV maximum.

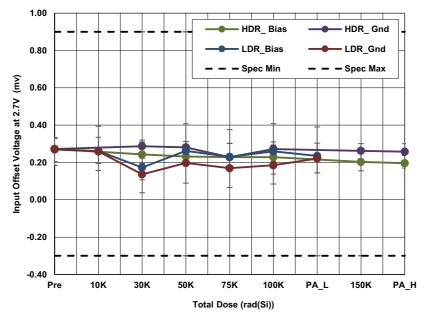


Figure 14. ISL7x100SEH input offset voltage (V_{OS}) with V+ = 2.7V, V_{RS+} = 0V and V_{SEN} = 5mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are -300µV minimum and 900µV maximum.

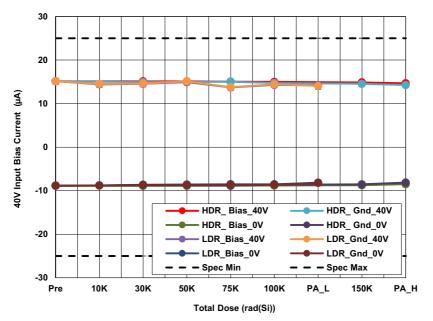


Figure 15. ISL7x100SEH positive input bias current (I_{BIAS+}) with V+ = 40V, V_{SEN} = 0mV and V_{RS+} = 40V and V_{RS+} = 0V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 25µA maximum for V_{RS+} = 40V and -25µA minimum for V_{RS+} = 0V.

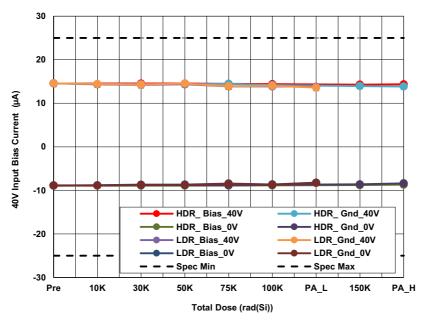


Figure 16. ISL7x100SEH negative input bias current (_{IBIAS-}) with V+ = 40V, V_{SEN} = 0mV and V_{RS+} = 40V and V_{RS+} = 0V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 25µA maximum for V_{RS+} = 40V and -25µA minimum for V_{RS+} = 0V.

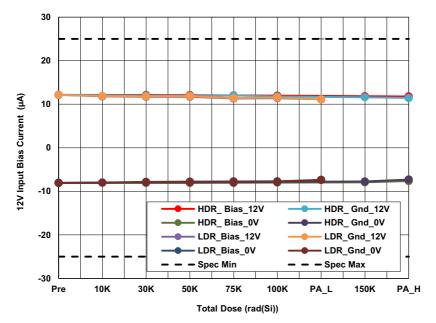


Figure 17. ISL7x100SEH positive input bias current (I_{BIAS+}) with V+ = 12V, V_{SEN} = 0mV and V_{RS+} = 12V and V_{RS+} = 0V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 25µA maximum for V_{RS+} = 12V and -25µA minimum for V_{RS+} = 0V.

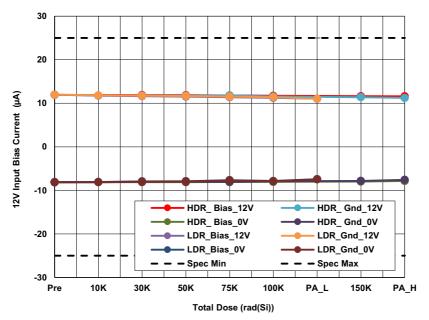


Figure 18. ISL7x100SEH negative input bias current (I_{BIAS}) with V+ = 12V, V_{SEN} = 0mV and V_{RS+} = 12V and V_{RS+} = 0V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 25µA maximum for V_{RS+} = 12V and -25µA minimum for V_{RS+} = 0V.

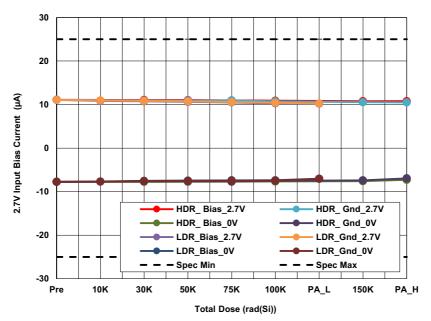


Figure 19. ISL7x100SEH positive input bias current (I_{BIAS+}) with V+ = 2.7V, V_{SEN} = 0mV and V_{RS+} = 2.7V and V_{RS+} = 0V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 25µA maximum for V_{RS+} = 2.7V and -25µA minimum for V_{RS+} = 0V.

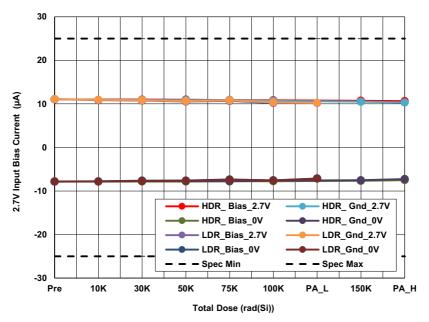


Figure 20. ISL7x100SEH negative input bias current (I_{BIAS}.) with V+ = 2.7V, V_{SEN} = 0mV and V_{RS+} = 2.7V and V_{RS+} = 0V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 25µA maximum for V_{RS+} = 2.7V and -25µA minimum for V_{RS+} = 0V.

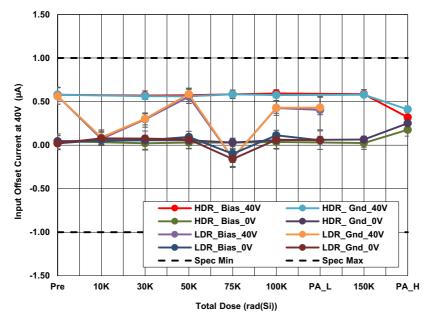


Figure 21. ISL7x100SEH input offset current (I_{OS}) with V+ = 40V, V_{SEN} = 0mV and V_{RS+} = 40V and V_{RS+} = 0V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are -1µA minimum and 1µA maximum.

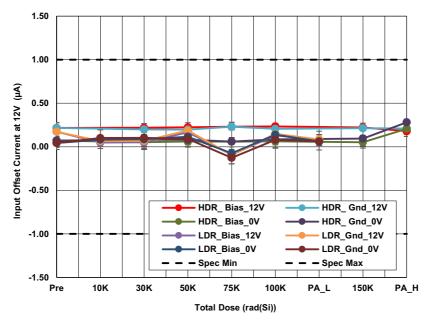


Figure 22. ISL7x100SEH input offset current (I_{OS}) with V+ = 12V, V_{SEN} = 0mV and V_{RS+} = 12V and V_{RS+} = 0V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are -1µA minimum and 1µA maximum.

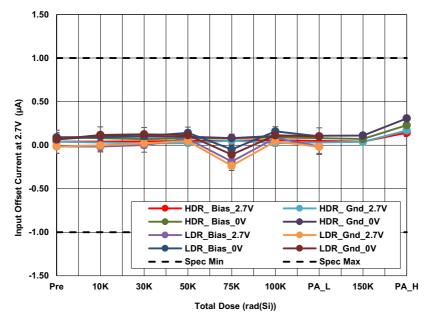


Figure 23. ISL7x100SEH input offset current (I_{OS}) with V+ =2.7V, V_{SEN} = 0mV and V_{RS+} = 2.7V and $_{VRS+}$ = 0V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are -1µA minimum and 1µA maximum.

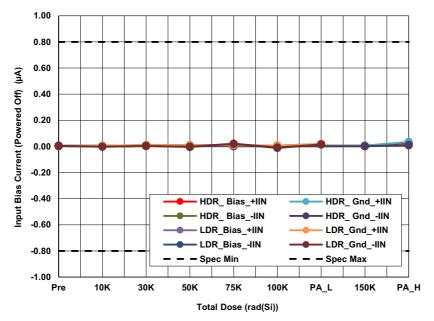


Figure 24. ISL7x100SEH input bias current (powered off) (I_{OFF}) with V+ = V_{SEN} = 0V, and V_{RS+} = 40V, 12.7V and 2.7V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are -0.8µA minimum and 0.8µA maximum.

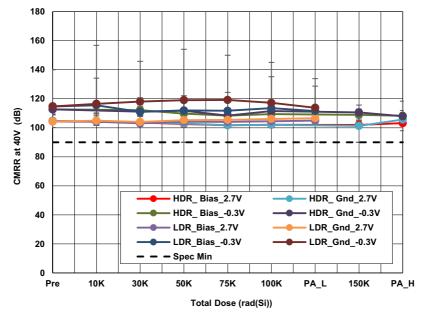


Figure 25. ISL7x100SEH Common-Mode Rejection Ratio (CMRR) with V+ = 40V, V_{SEN} = 5mV, V_{RS+} = 2.7V to 40V and -0.3V to 40V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limit is 90dB minimum.

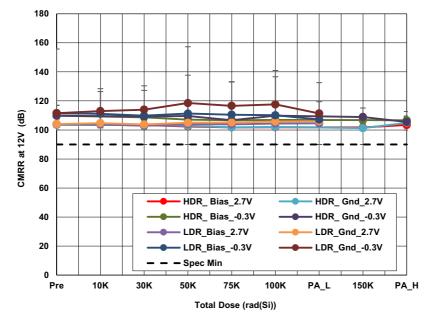


Figure 26. ISL7x100SEH Common-Mode Rejection Ratio (CMRR) with V+ = 12V, V_{SEN} = 5mV, V_{RS+} = 2.7V to 40V and -0.3V to 40V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limit is 90dB minimum.

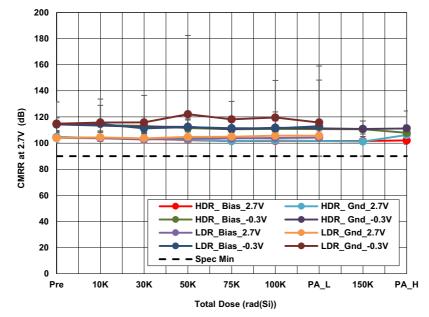


Figure 27. ISL7x100SEH Common-Mode Rejection Ratio (CMRR) with V+ = 2.7V, V_{SEN} = 5mV, V_{RS+} = 2.7V to 40V and -0.3V to 40V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limit is 90dB minimum.

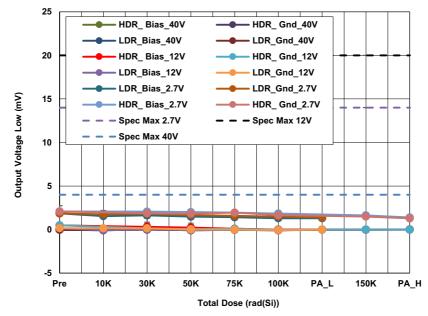


Figure 28. ISL7x100SEH minimum output voltage (V_{OL}) with V+ = 40V, 12V, and 2.7V and V_{SEN} = 0V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 4mV maximum for V+ = 40V, 14mV maximum for V+ = 2.7V and 20mV maximum for V+ = 12V.

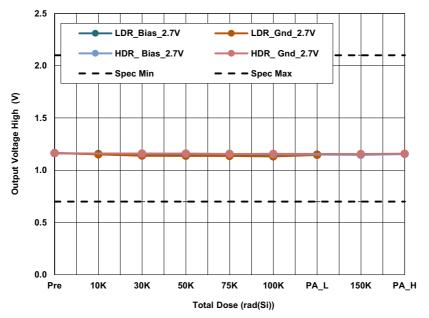


Figure 29. ISL7x100SEH maximum output voltage (V_{OH}) with V+ = 2.7V (V_{SEN} = 27mV), A_V = 100, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 0.7V minimum and 2.1V maximum.

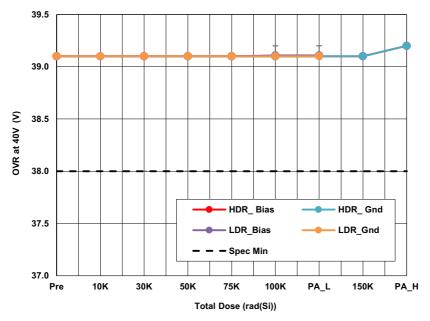


Figure 30. ISL7x100SEH maximum linear output voltage range (OVR) with V+ = 40V, V_{SEN} = 150mV, and R_L = OPEN, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limit is 38.0V minimum.

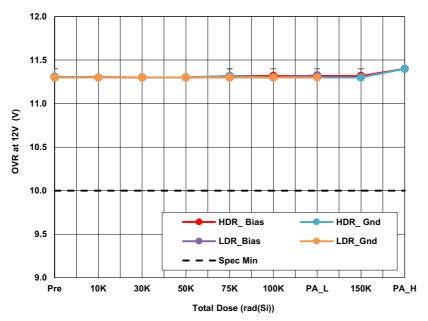


Figure 31. ISL7x100SEH maximum linear output voltage range (OVR) with V+ = 12V, V_{SEN} = 150mV, and R_L = OPEN, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limit is 10.0V minimum.

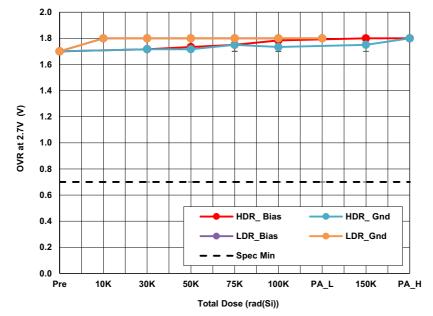


Figure 32. ISL7x100SEH maximum linear output voltage range (OVR) with V+ = 2.7V, V_{SEN} = 150mV, and R_L = OPEN, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limit is 0.7V minimum.

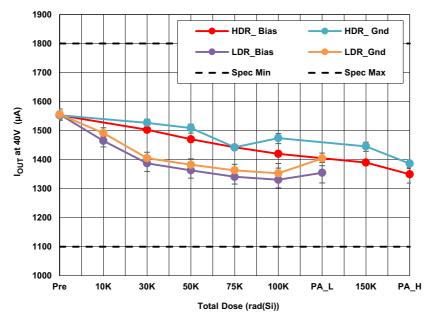


Figure 33. ISL7x100SEH maximum linear output current range (I_{OUT}) with V+ = 40V and R_{OUT} = 0 Ω , as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 1100 μ A minimum and 1800 μ A maximum.

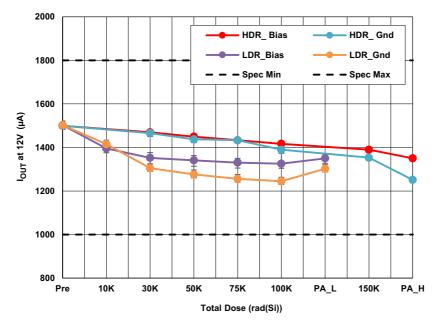


Figure 34. ISL7x100SEH maximum linear output current range (I_{OUT}) with V+ = 12V and R_{OUT} = 0 Ω , as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 1000 μ A minimum and 1800 μ A maximum.

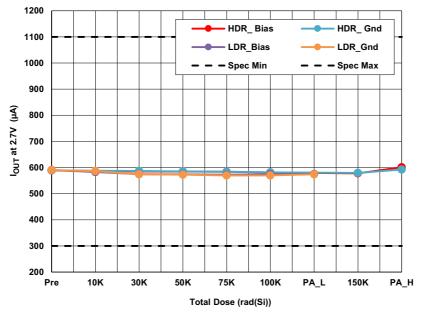


Figure 35. ISL7x100SEH maximum linear output current range (I_{OUT}) with V+ = 2.7V and R_{OUT} = 0 Ω , as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 300µA minimum and 1100µA maximum.

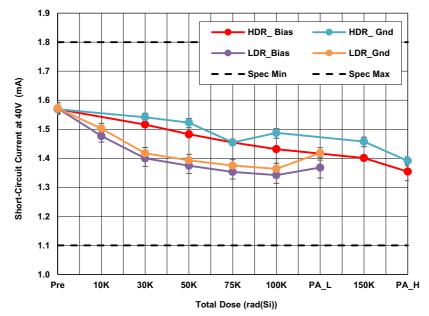


Figure 36. ISL7x100SEH short-circuit current (I_{SC}) with V+ = 40V, V_{RS+} = 40V, V_{RS-} = 0V and R_{OUT} = 0 Ω , as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 1100µA minimum and 1800µA maximum.

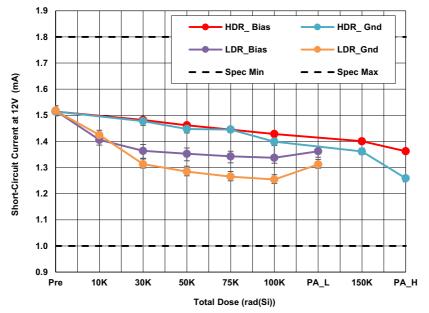


Figure 37. ISL7x100SEH short-circuit current (I_{SC}) with V+ = 12V, V_{RS+} = 40V, V_{RS-} = 0V and R_{OUT} = 0 Ω , as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 1000µA minimum and 1800µA maximum.

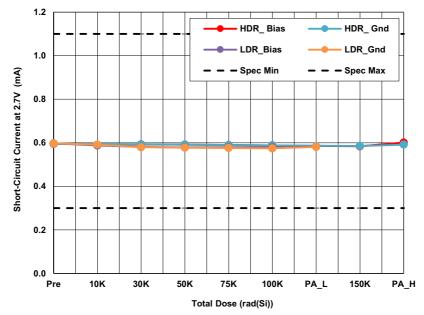


Figure 38. ISL7x100SEH short-circuit current (I_{SC}) with V+ = 2.7V, V_{RS+} = 40V, V_{RS-} = 0V and R_{OUT} = 0 Ω , as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 300 μ A minimum and 1100 μ A maximum.

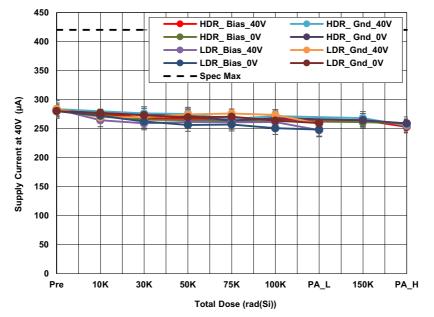


Figure 39. ISL7x100SEH supply current (I₊) with V+ = 40V, V_{SEN} = 0V, V_{RS+} = 40V and 0V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limit is 420µA maximum.

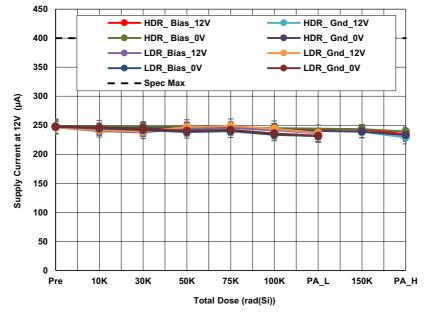


Figure 40. ISL7x100SEH supply current (I₊) with V+ = 12V, V_{SEN} = 0V, V_{RS+} = 12V and 0V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limit is 400µA maximum.

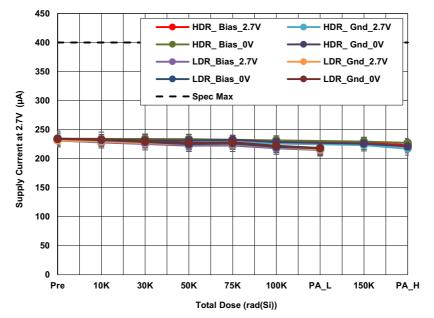


Figure 41. ISL7x100SEH supply current (I₊) with V+ = 2.7V, V_{SEN} = 0V, V_{RS+} = 2.7V and 0V, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limit is 400µA maximum.

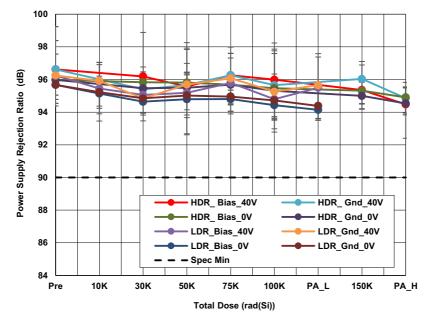


Figure 42. ISL7x100SEH power supply rejection ration (PSRR) with V+ = 40V, V_{RS+} = 0V, 40V and V_{SEN} = 5mV to 150mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limit is 90dB minimum.

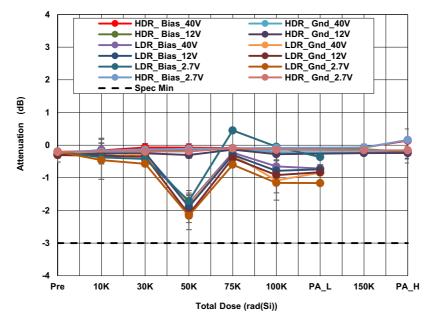


Figure 43. ISL7x100SEH 500kHz Attenuation (Att_{500kHz}) with V+ = 40V, 12V, and 2.7V, V_{SEN} = 5mV to 150mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limit is -3dB minimum.

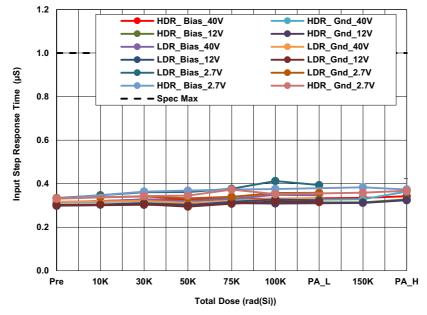


Figure 44. ISL7x100SEH input step response time (t_{RES}) with V+ = 40V, 12V, and 2.7V, V_{SEN} = 5mV to 150mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limit is 1µs maximum.

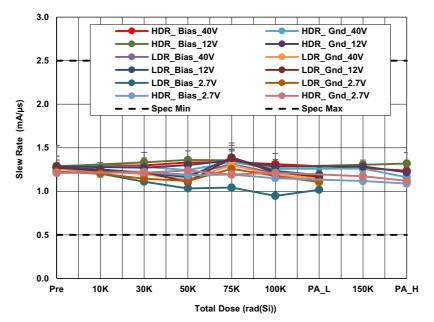


Figure 45. ISL7x100SEH slew rate (SR) with V+ = 40V, 12V, and 2.7V, VSEN = 5mV to 150mV, as a function of total dose irradiation at LDR and HDR. The post-irradiation SMD limits are 0.5mA/µs minimum and 2.5ma/µs maximum.

3. Discussion and Conclusion

The results of the LDR and HDR total dose test of the ISL7x100SEH radiation hardened 40V current sense amplifier are reported. Both irradiations were followed by a 168-hour anneal at 100°C under bias. All SMD parameters passed at all downpoints, but some showed some degradation. **Note**: Although the 12V and 40V V_{OH} results were well within the limits, only the 2.7V V_{OH} results were plotted.

The maximum linear output current range (I_{OUT}), shown in <u>Figures 33</u> and <u>34</u>, degrades significantly over irradiation at both dose rates, as does the short-circuit current (I_{SC}), shown in <u>Figures 36</u> and <u>37</u>. From these results, it is seen that those parameters in the PNP output driver degrade more at higher biases because the same degree of degradation is not seen at 2.7V but the current requirements are not as stringent either. Some minor anneal sensitivity is seen in some of those same graphs but have less than a 10% delta.

4. Appendices

4.1 Reported parameters

<u>Table 3</u> lists the key parameters that are considered indicative of part performance. These parameters are plotted in <u>Figures 3</u> through <u>45</u>. All limits are taken from the ISL7x100SEH SMD.

Table 3.	ISL7x100SEH Key Total Dose SMD Parameters (T _A = 25°C)
----------	---

Figure	Parameter	Symbol	Conditions	Low Limit	High Limit	Units
<u>3</u>	Transconductance (V_{SEN} = 25mV to 150mV)	9 _m	V+ = 40V, V _{RS+} = 40V	1.970	2.010	µA/mV
<u>4</u>			V+ = 40V, V _{RS+} = 0V	1.940	2.060	µA/mV
<u>5</u>			V+ = 12V, V _{RS+} = 12V	1.976	2.016	µA/mV
<u>6</u>			V+ = 12V, V _{RS+} = 0V	1.940	2.060	µA/mV
<u>Z</u>			V+ = 2.7V, V _{RS+} = 2.7V	1.986	2.026	µA/mV
<u>8</u>			V+ = 2.7V, V _{RS+} = 0V	1.940	2.060	µA/mV
<u>9</u>	Input Offset Voltage (V _{SEN} = 5mV)	V _{OS}	V+ = 40V, V _{RS+} = 40V	-1200	300	μV
<u>10</u>			V+ = 40V, V _{RS+} = 0V	-1100	300	μV
<u>11</u>			V+ = 12V, V _{RS+} = 12V	-400	400	μV
<u>12</u>			V+ = 12V, V _{RS+} = 0V	-400	400	μV
<u>13</u>			V+ = 2.7V, V _{RS+} = 2.7V	-300	1000	μV
<u>14</u>			V+ = 2.7V, V _{RS+} = 0V	-300	900	μV
<u>15</u>	Input Bias Current (V _{SEN} = 0mV)	I _{BIAS+}	V+ = 40V, V _{RS+} = 40V, 0V	-25	25	μA
<u>16</u>		I _{BIAS-}				
<u>17</u>		I _{BIAS+}	V+ = 12V, V _{RS+} = 12V, 0V	-25	25	μA
<u>18</u>		I _{BIAS-}				
<u>19</u>		I _{BIAS+}	V+ = 2.7V, V _{RS+} = 2.7V, 0V	-25	25	μA
<u>20</u>		I _{BIAS-}				
<u>21</u>	Input Offset Current (V _{SEN} = 0mV)	I _{OS}	V+ = 40V, V _{RS+} = 40V, 0V	-1	1	μA
<u>22</u>			V+ = 12V, V _{RS+} = 12V, 0V	-1	1	μA
<u>23</u>			V+ = 2.7V, V _{RS+} = 2.7V, 0V	-1	1	μA
<u>24</u>	Input Bias Current (powered off) (V+ = V _{SEN} = 0mV)	I _{OFF}	V _{RS+} = 40V, 12V, 2.7V	-0.8	0.8	μA
<u>25</u>	Common-Mode Rejection Ratio (V _{SEN} = 5mV,	CMRR	V+ = 40V	90	-	dB
<u>26</u>	V _{RS+} = 2.7V to V+ and -0.3V to V+)		V+ = 12V	90	-	dB
<u>27</u>			V+ = 2.7V	90	-	dB
<u>28</u>	Minimum Output Voltage (V _{SEN} = 0mV)	V _{OL}	V+ = 40V	-	4	mV
			V+ = 12V	-	20	mV
			V+ = 2.7V	-	14	mV
<u>29</u>	Maximum Output Voltage (Note: Only V+ = 2.7V is plotted)	V _{OH}	V+ =40V (V _{SEN} = 100mV, A _V = 400)	38	39.4	V
			V+ = 12V (V _{SEN} = 120mV, A _V = 100)	10	11.4	V
			V+ = 2.7V (V _{SEN} = 120mV, A _V = 100)	0.7	2.1	V
<u>30</u>	Maximum Linear Output Voltage Range	OVR	V+ = 40V	38	-	V
<u>31</u>	(V _{SEN} = 150mV, R _L = OPEN)		V+ = 12V	10	-	V
<u>32</u>			V+ = 2.7V	0.7	-	V

Figure	Parameter	Symbol	Conditions	Low Limit	High Limit	Units
<u>33</u>	Maximum Linear Output Current Range ($R_{OUT} = 0\Omega$)	I _{OUT}	V+ = 40V	1200	1800	μA
<u>34</u>			V+ = 12V	1000	1800	μA
<u>35</u>			V+ = 2.7V	300	1100	μA
<u>36</u>	Short-Circuit Current ($R_{OUT} = 0\Omega$)	I _{SC}	V+ = 40V, V _{RS+} = 40V, 0V	1200	1800	μA
<u>37</u>			V+ = 12V, V _{RS+} = 12V, 0V	1000	1800	μA
<u>38</u>			V+ = 2.7V, V _{RS+} = 2.7V, 0V	300	1100	μA
<u>39</u>	Supply Current (V _{SEN} = 0mV)	I+	V+ = 40V, V _{RS+} = 40V, 0V	-	420	μA
<u>40</u>			V+ = 12V, V _{RS+} = 12V, 0V	-	400	μA
<u>41</u>			V+ = 2.7V, V _{RS+} = 2.7V, 0V	-	400	μA
<u>42</u>	Power supply rejection ratio (V _{SEN} = 5mV to 150mV)	PSRR	V+ = 40V, V _{RS+} = 0V, 40V	90	-	dB
<u>43</u>	500kHz Attenuation	Att _{500kHz}	V+ = 40V, 12V, 2.7V	-3	-	dB
<u>44</u>	Input Step Response Time (V _{SEN} = 5mV to 150mV)	t _{RES}	V+ = 40V, 12V, 2.7V	-	1	μs
<u>45</u>	Slew Rate (V _{SEN} = 5mV to 150mV)	SR	V+ = 40V, 12V, 2.7V	0.5	2.5	mA/µs

Table 3. ISL7x100SEH Key Total Dose SMD Parameters (T_A = 25°C) (Continued)

5. Revision History

Rev.	Date	Description
1.00	Jun.29.20	Initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/