ISL70005SEH

Total Dose Test Report

Introduction

This report provides interim results of a Low Dose Rate (LDR) and High Dose Rate (HDR) Total Ionizing Dose (TID) test of the ISL70005SEH and ISL73005SEH dual output point-of-load converters, which combine a synchronous buck regulator and a low dropout voltage linear regulator. The two parts have identical electrical performance and differ only in their total dose specifications, and the ISL70005SEH results reported in this document apply equally to the ISL73005SEH. The test was conducted to determine the sensitivity of the parts to the total dose environment and to determine if the parts display dose rate or bias sensitivity. The test also included biased high temperature anneals after the completion of irradiation to evaluate time-dependent effects. The LDR used was 0.01rad(Si)/s and the HDR was 70rad(Si)/s.

HDR testing is complete through 150krad(Si) and subsequent high temperature biased anneal. The LDR tests have completed 75krad(Si) and are being continued to 100krad(Si) and through anneal.

Product Description

The ISL70005SEH and ISL73005SEH are radiation hardened dual output Point-of-Load (POL) regulators combining the high efficiency of a synchronous buck regulator with the low noise of a Low Dropout (LDO) linear regulator. The parts are suited for 3.3V or 5V power buses and can support a continuous output load current of 3A for the buck regulator and ±1A for the LDO. Figure 1 shows a block diagram.

The buck regulator uses voltage mode control architecture and switches at an adjustable frequency of 100kHz to 1MHz set by an external resistor. Externally adjustable loop compensation allows for an optimum balance between stability and output dynamic performance. The integrated synchronous power switches are optimized for high efficiency and excellent thermal performance.

The LDO is completely configurable independently of the switching regulator. It uses NMOS pass devices and the chip bias voltage (L_VCC) is used to drive the pass device gate. This enables the LDO to function with less than 1V on the L_VIN NMOS input. The LDO can sink and source up to 1A continuously making it a suitable choice for powering DDR memory.

The ISL70005SEH is radiation hardened to a TID rating of 100krad(Si) at HDR (50 - 300rad(Si)/s) and to 75krad(Si) at LDR (< 0.01rad(Si)/s). The ISL73005SEH is radiation hardened to a TID rating of 75krad(Si) at LDR (< 0.01rad(Si)/s). This document reports TID response data for 75krad(Si) at LDR and 150krad(Si) at HDR for the biased and unbiased cases. The LDR tests are being continued to 100krad(Si) and anneal. The ISL70005SEH is acceptance tested on a wafer-by-wafer basis to 75krad(Si) at LDR and 100krad(Si) at HDR, while the ISL73005SEH is acceptance tested on a wafer-by-wafer basis to 75krad(Si) at LDR only.

The ISL70005SEH and ISL73005SEH are also rated for Single-Event Effects (SEE). The parts are free of permanent damage up to a LET of 86MeV•cm^2/mg at a maximum supply voltage of 6.0V and a case temperature of +125°C ±10°C. Single-Event Transient (SET) performance is specified as a change in an output voltage of less than 3% at a LET of 86.4MeV•cm^2/mg. Single-Event Functional Interrupt (SEFI) free operation is specified up to a LET of 43MeV•cm^2/mg.

Both parts are implemented in a submicron BiCMOS process optimized for power management applications. The process is in volume production under MIL-PRF-38535 certification and is used for a wide range of commercial and radiation-hardened power management devices. The parts are available in a 28 Ld ceramic flatpack or die form and are specified across the military temperature range of -55°C to +125°C.

Related Literature

For a full list of related documents, visit our website:

- ISL70005SEH, ISL73005SEH device pages
- MIL-STD-883 test method 1019

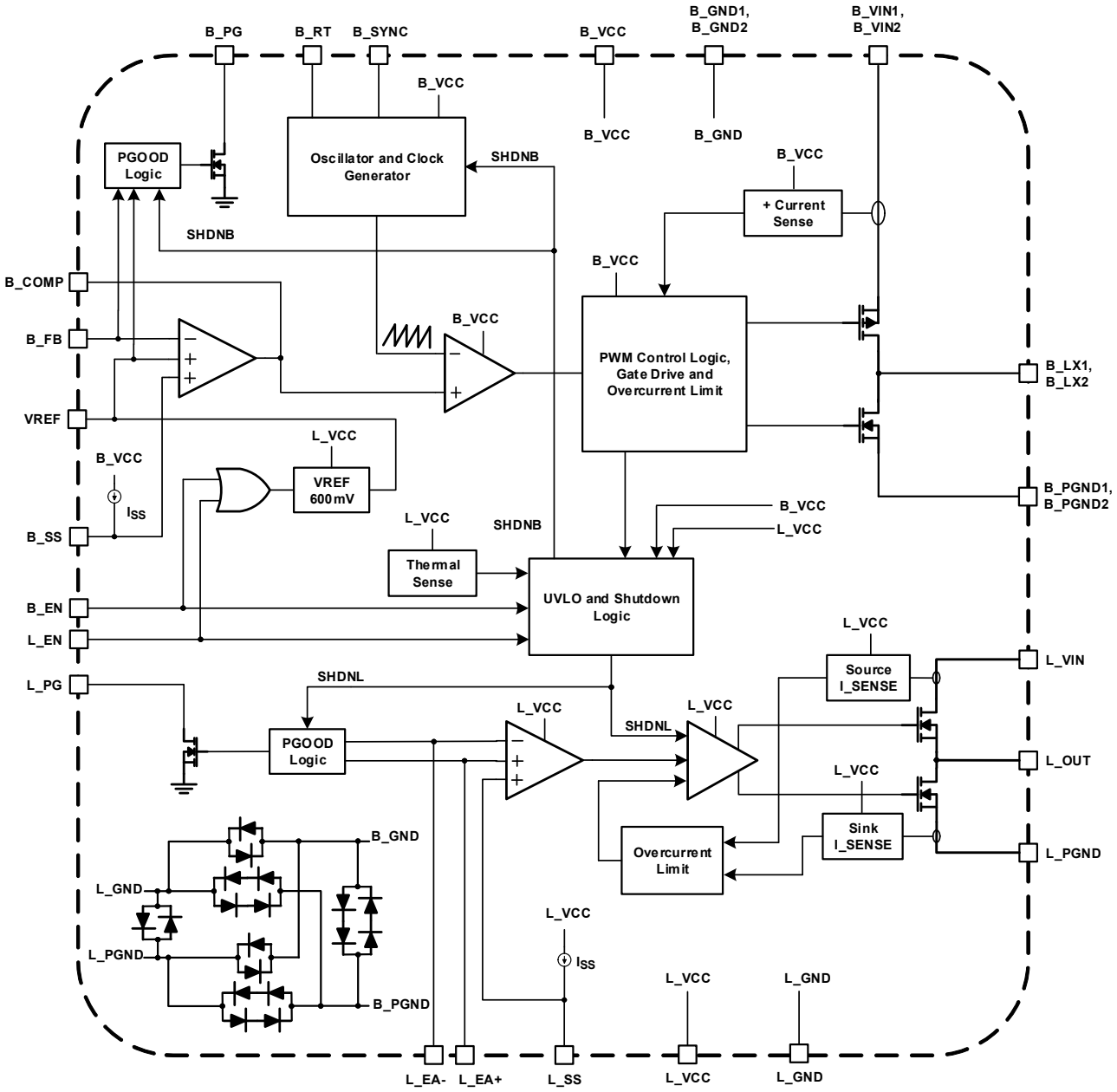

Figure 1. ISL70005SEH Block Diagram

1. Test Description

1.1 Irradiation Facilities

HDR testing was performed using a Gammacell 220 gamma-ray irradiator located in the Renesas Palm Bay, Florida facility. LDR testing used a Hopewell Designs (Alpharetta, GA) N40 vault-type LDR irradiator located in the same facility. The HDR irradiations were performed at 70rad(Si)/s and the LDR work was performed at 0.010rad(Si)/s, both per MIL-STD-883 Method 1019. The post-irradiation biased anneals used the same bias configuration (Figure 2) as the biased irradiation and were performed at 100°C using a small temperature chamber.

1.2 Test Fixturing

Figure 2 shows the configuration used for biased LDR and HDR irradiation and anneal.

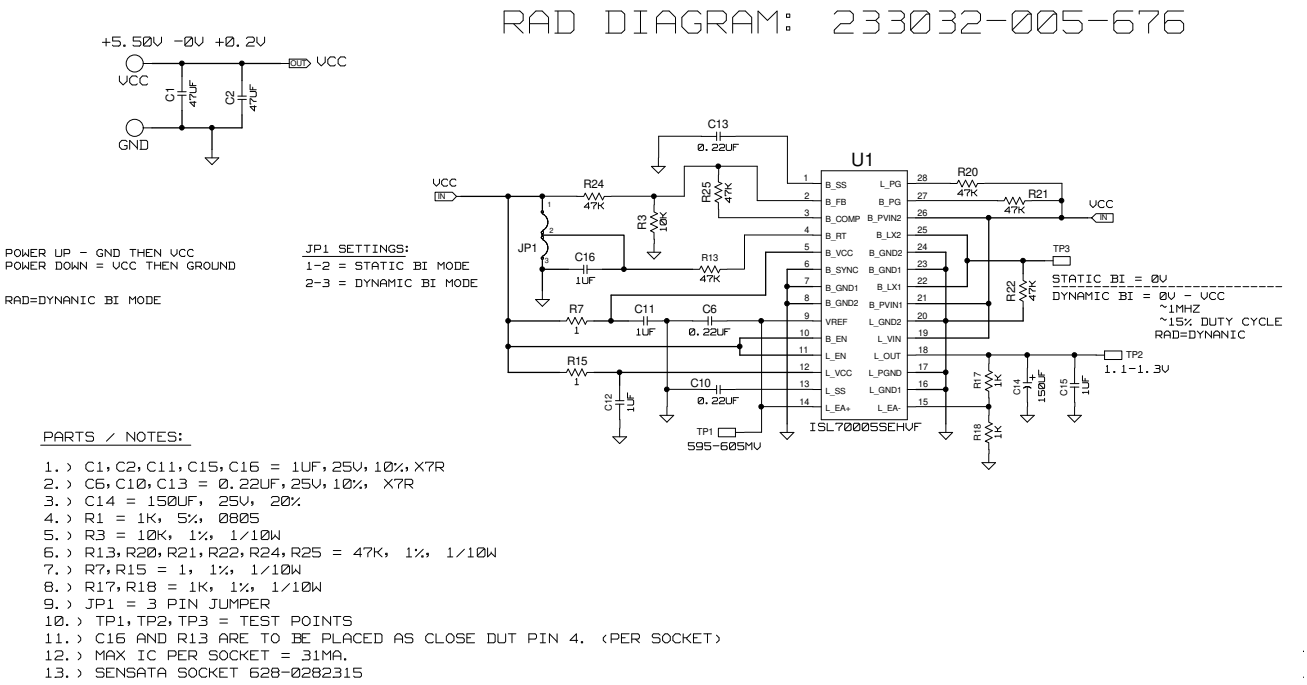

Figure 2. Irradiation and Anneal Bias Configuration

1.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with data logging at each down point. Down point electrical testing was performed at room temperature. Three control units were used to ensure repeatable data.

1.4 Experimental Matrix

Testing proceeded in accordance with the LDR sensitivity diagnostic protocol outlined in MIL-STD-883 Test Method 1019. The experimental matrix consisted of 12 samples irradiated at HDR with all pins grounded, 12 samples irradiated at HDR under bias, 21 samples irradiated at LDR with all pins grounded and 21 samples irradiated at LDR under bias. A biased anneal at 100°C for 168 hours was performed on the HDR samples following the final irradiation to evaluate the Time-Dependent Effect (TDE) characteristics of the part.

Samples of the ISL70005SEH were drawn from lot 1KJWB00000, wafer A3IBVUW and were packaged in production package code KDA 28 Ld ceramic flatpacks. Samples were processed through the standard QML-V burn-in screens of 180 hours dynamic burn-in and 72 hours static burn-in before irradiation, as required by

MIL-STD-883, and were screened to the SMD 5962-19209 limits at room, low, and high temperature before the start of total dose testing.

1.5 Down Points

The HDR down points were 0, 10, 30, 50, 100, and 150krad(Si) and the LDR down points to date were 0, 10, 30, 50, and 75krad(Si). The biased anneals were performed at 100°C for 168 hours.

2. Results

Total dose testing of the ISL70005SEH showed no reject devices at any down point after biased or grounded irradiation at either dose rate, noting that the LDR tests continued through 100krad(Si) and subsequent anneal. All samples were classified as Bin 1 at all down points including annealing, indicating full compliance with datasheet and SMD limits. It should be noted that all SMD pre-irradiation and post-irradiation limits are identical.

2.1 Attributes Data

Table 1. Attributes Data

Part	Dose Rate (rad(Si)/s)	Bias	Sample Size	Down Point	Pass (Note 1)	Fail
ISL70005SEH	70	Biased	12	Pre-irradiation	12	0
				10krad(Si)	12	0
				30krad(Si)	12	0
				50krad(Si)	12	0
				100krad(Si)	12	0
				150krad(Si)	12	0
				Anneal	12	0
ISL70005SEH	70	Grounded	12	Pre-irradiation	12	0
				10krad(Si)	12	0
				30krad(Si)	12	0
				50krad(Si)	12	0
				100krad(Si)	12	0
				150krad(Si)	12	0
				Anneal	12	0
ISL70005SEH	0.01	Biased	21	Pre-irradiation	21	0
				10krad(Si)	21	0
				30krad(Si)	21	0
				50krad(Si)	21	0
				75krad(Si)	21	0
ISL70005SEH	0.01	Grounded	21	Pre-irradiation	21	0
				10krad(Si)	21	0
				30krad(Si)	21	0
				50krad(Si)	21	0
				75krad(Si)	21	0

Note:
1. A pass indicates a sample that passes all SMD limits.

2.2 Variables Data

Figure 3 through Figure 21 show the total dose response of selected critical parameters at all down points to date. The plots show the average as a function of the total dose for each of the irradiation conditions. All parts showed good stability over irradiation and anneal, with no observed dose rate or bias sensitivity.

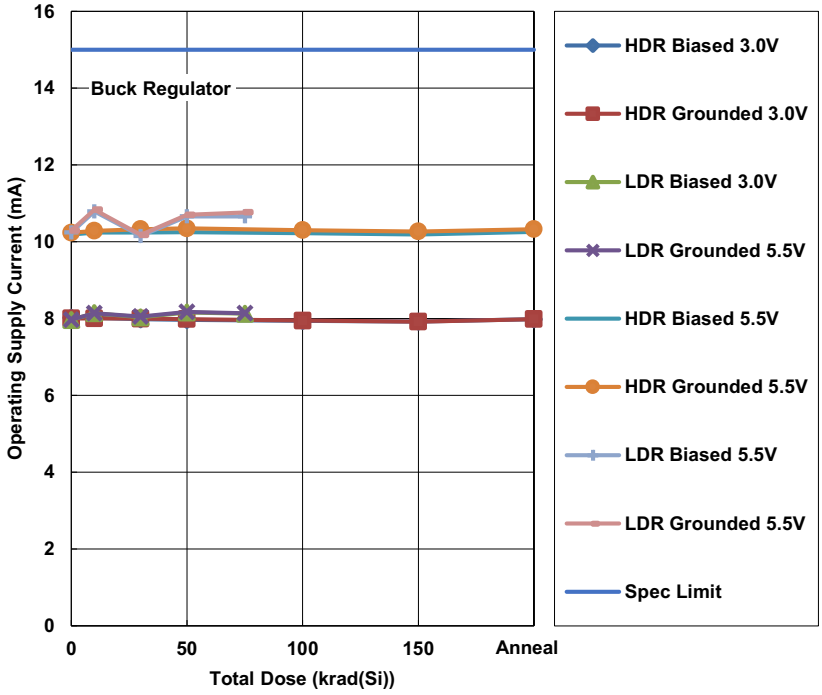

Figure 3. ISL70005SEH buck regulator operating power supply current at 100kHz, 3.0V and 5.5V supply cases, as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limit is 15mA maximum for both supply voltage cases.

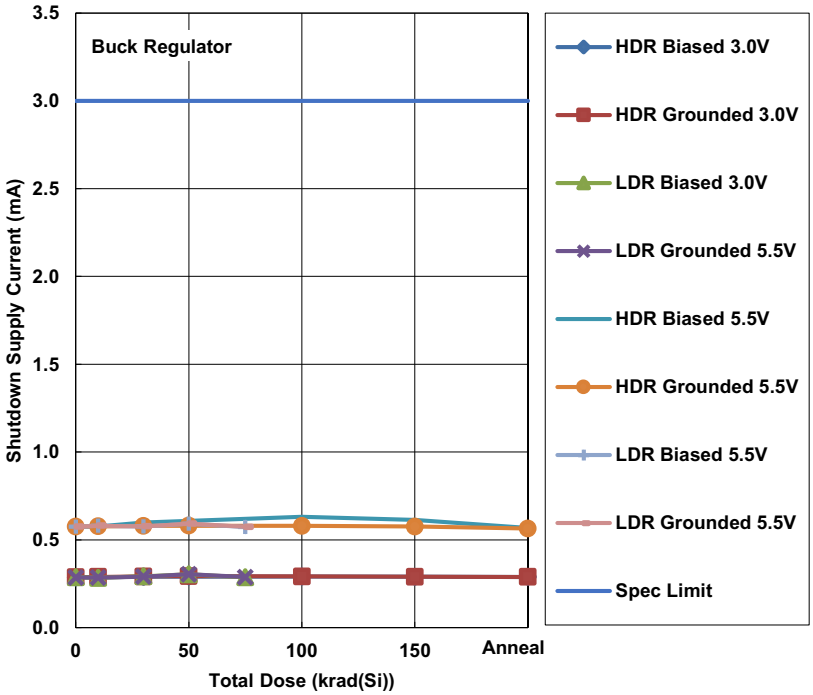

Figure 4. ISL70005SEH buck regulator shutdown power supply current, 3.0V and 5.5V supply cases, as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limit is 3.0mA maximum for both supply voltage cases.

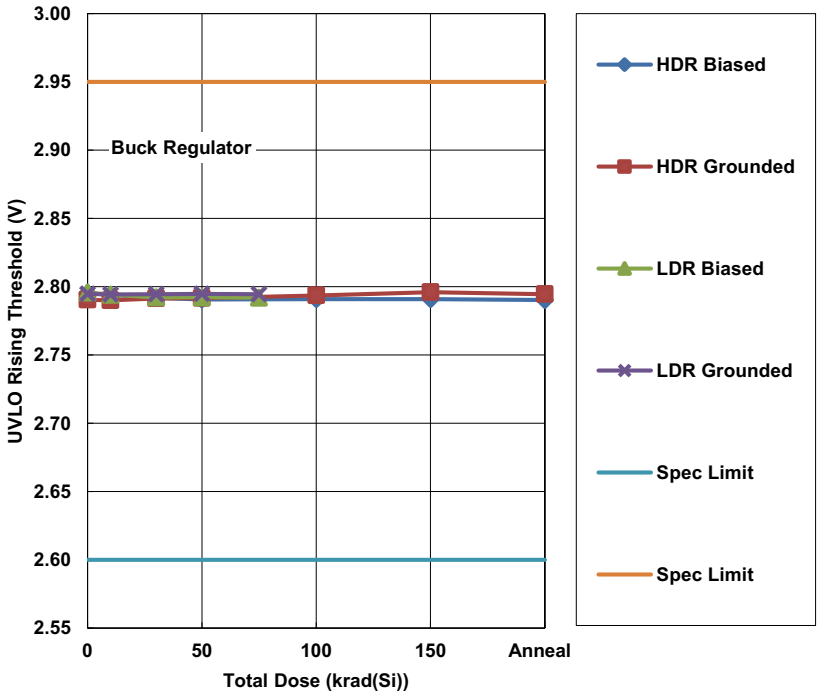

Figure 5. ISL70005SEH buck regulator Undervoltage Lockout (UVLO) rising threshold as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are 2.60V to 2.95V.

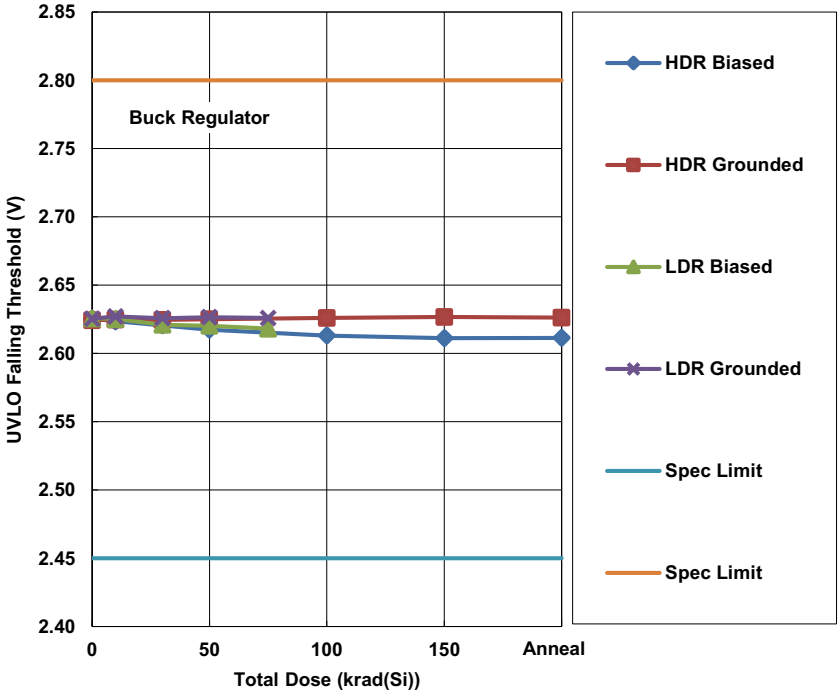

Figure 6. ISL70005SEH buck regulator Undervoltage Lockout (UVLO) falling threshold as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are 2.45V to 2.80V.

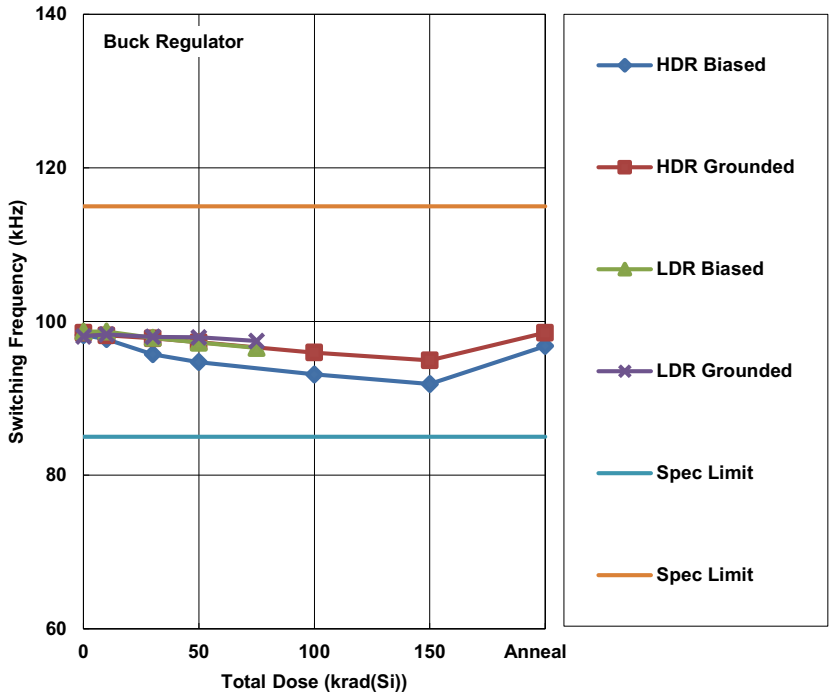

Figure 7. ISL70005SEH buck regulator switching frequency as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are 85kHz to 115kHz.

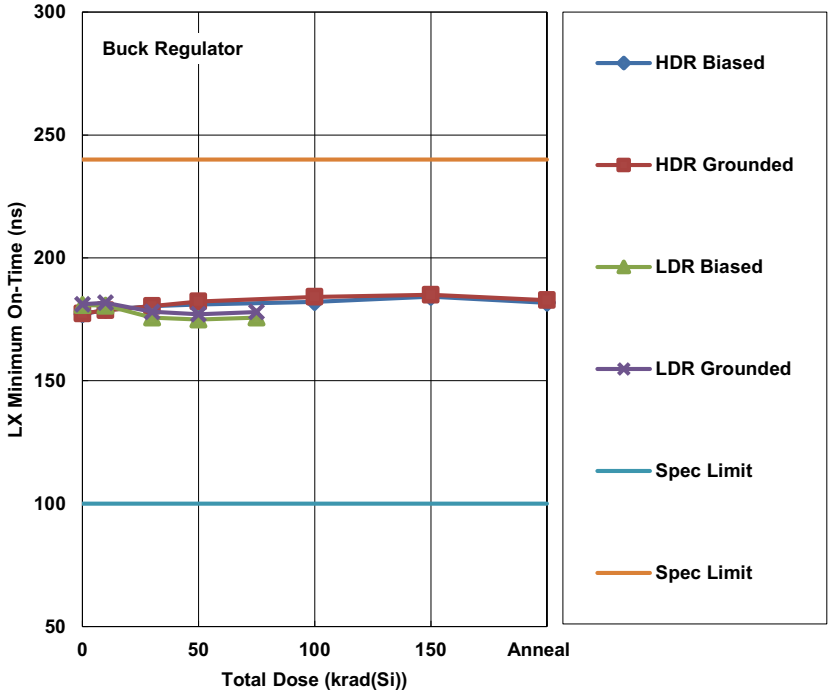

Figure 8. ISL70005SEH buck regulator LX output minimum on-time, 5.5V supply, as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are 100ns to 240ns.

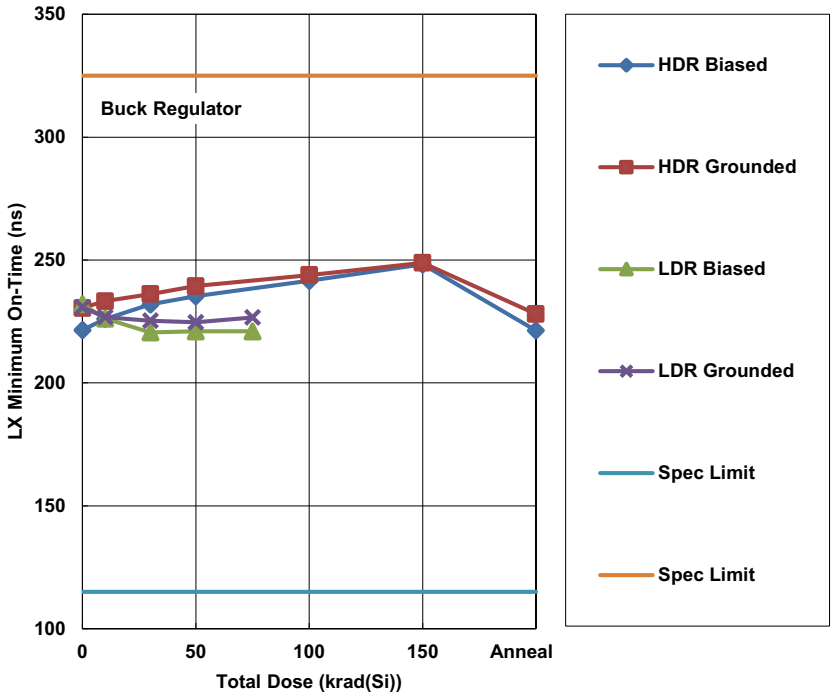

Figure 9. ISL70005SEH buck regulator LX minimum on-time, 3.0V supply, as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are 115ns to 325ns.

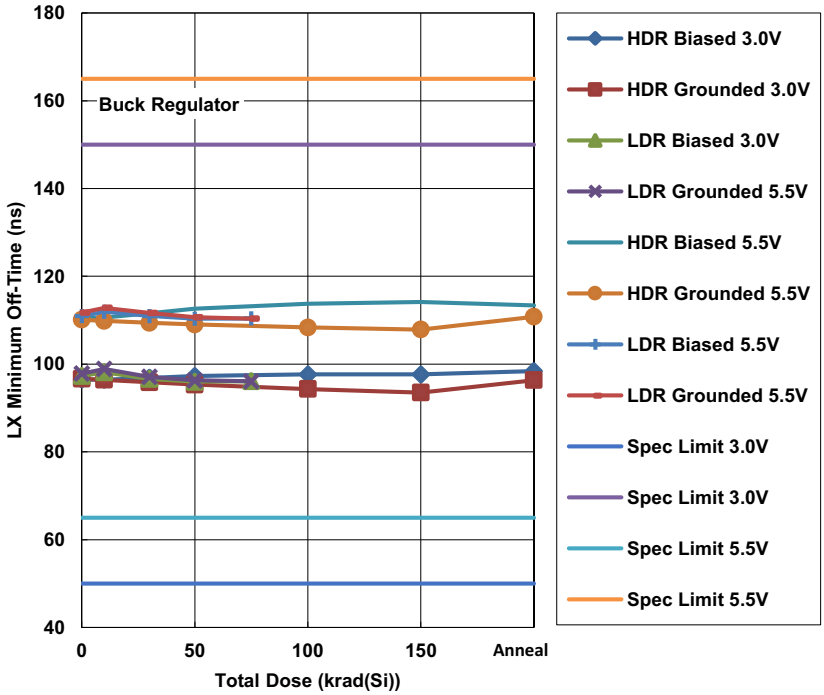

Figure 10. ISL70005SEH buck regulator LX minimum off-time, 3.0V and 5.5V supply, as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are 50ns to 150ns (3.0V) and 65ns to 165ns (5.5V).

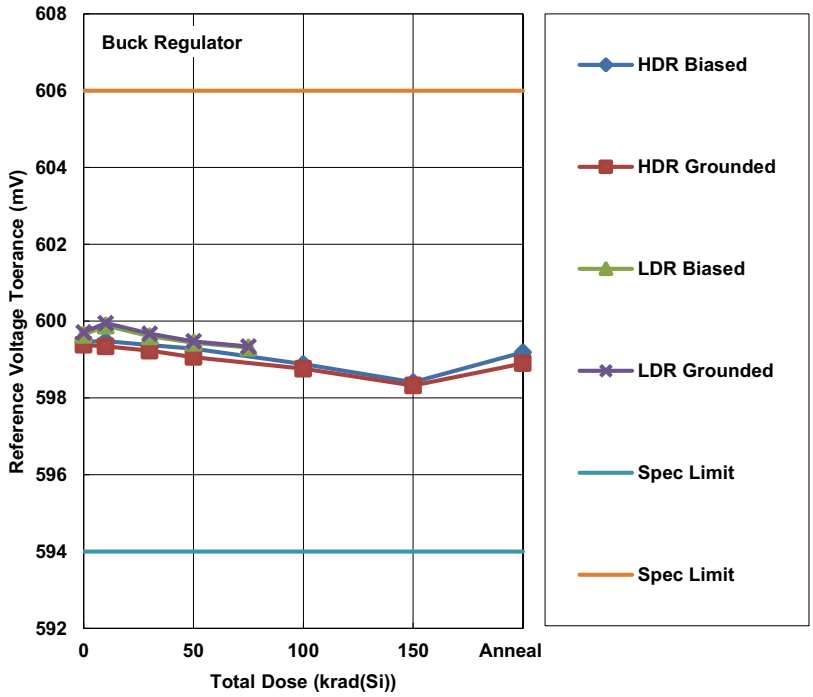

Figure 11. ISL70005SEH buck regulator reference voltage tolerance (defined as the sum of V_{REF} and error amplifier V_{IO}) as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are 594mV to 606mV.

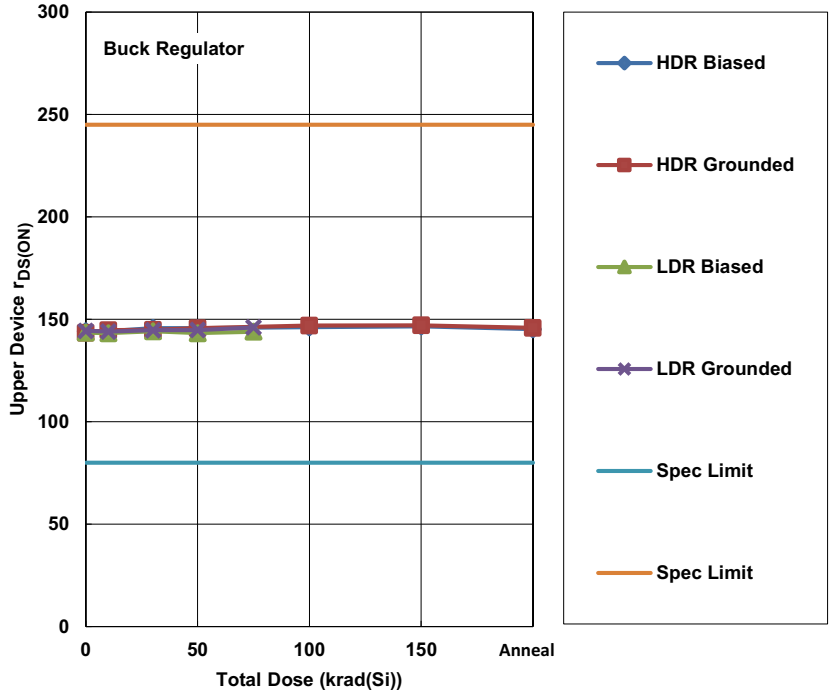

Figure 12. ISL70005SEH buck regulator upper device ON-resistance, 3.0V supply, as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are 80mΩ to 245mΩ.

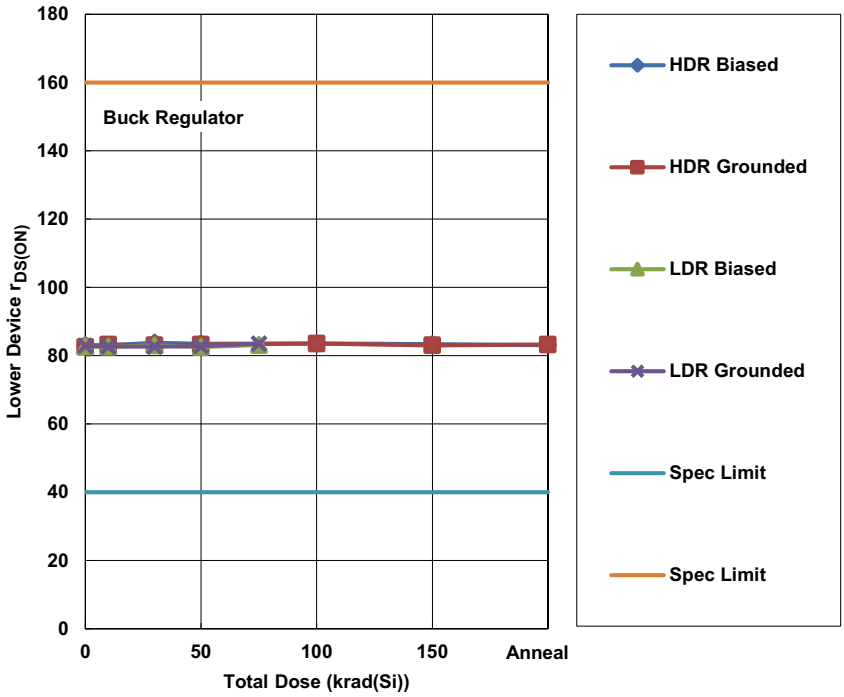

Figure 13. ISL70005SEH buck regulator lower device ON-resistance, 3.0V supply, as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are 40mΩ to 160mΩ.

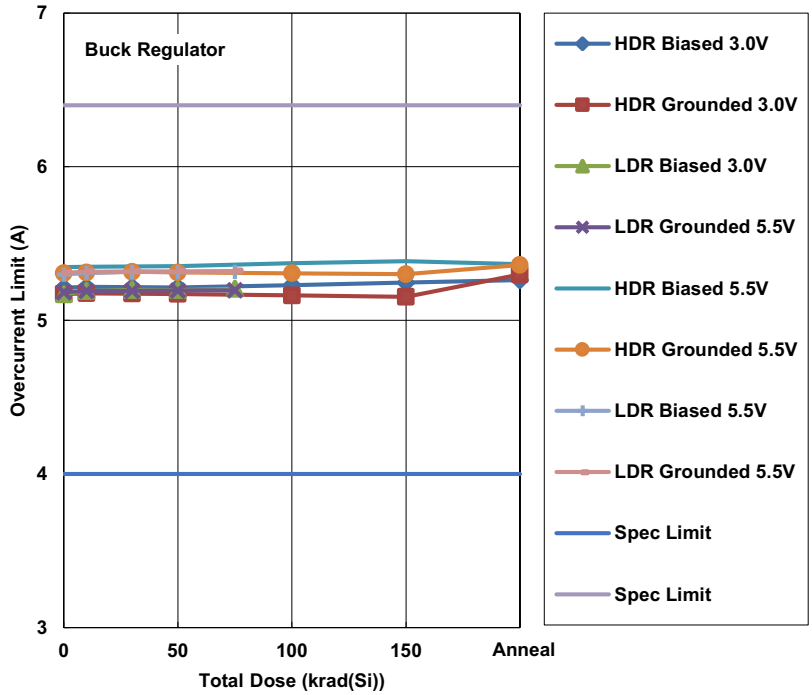

Figure 14. ISL70005SEH buck regulator overcurrent limit, 3.0V and 5.5V supply cases, as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are 4.0A to 6.4A for both cases.

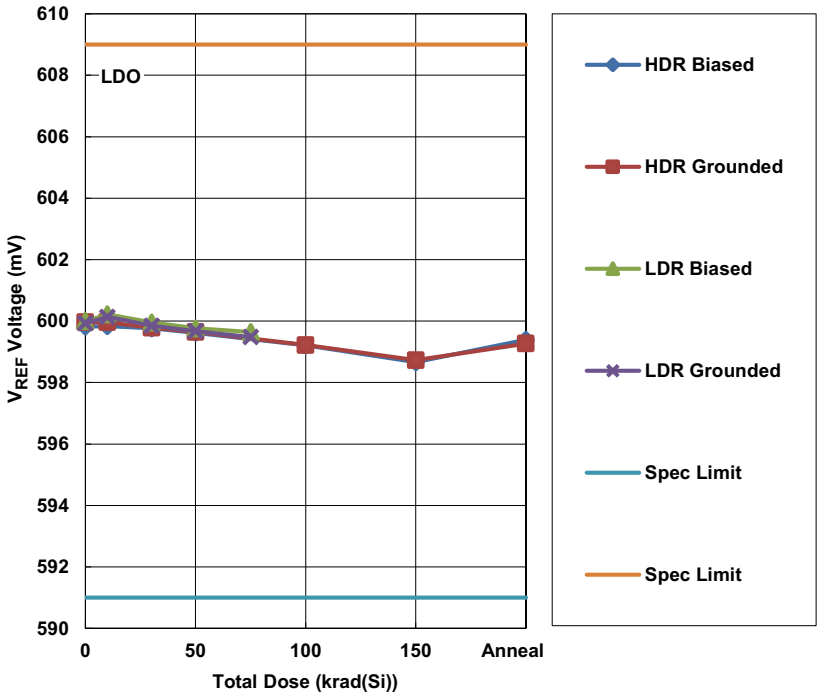

Figure 15. ISL70005SEH LDO reference voltage as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are 591mV to 609mV.

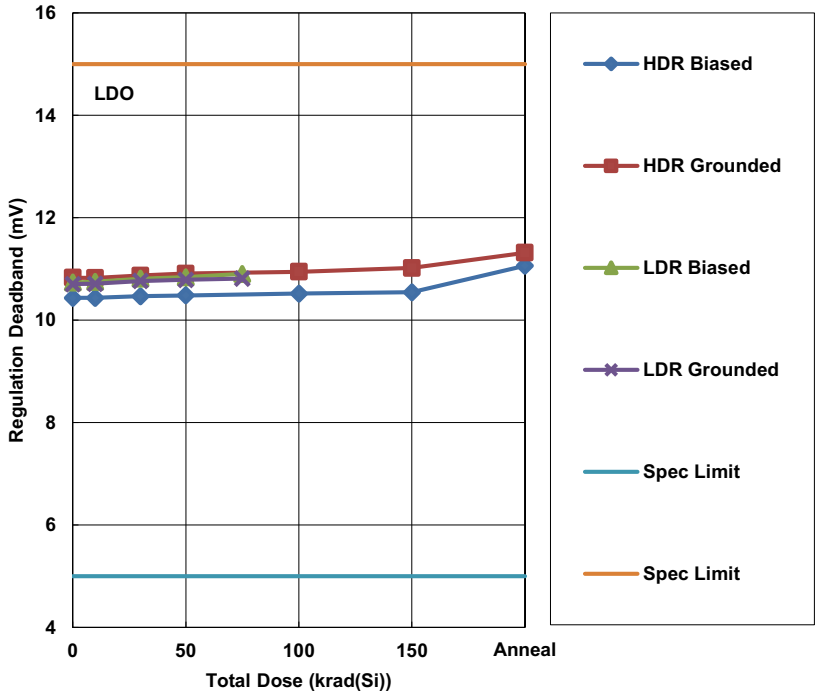

Figure 16. ISL70005SEH LDO regulation deadband, 5.5V supply, as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are 5mV to 15mV.

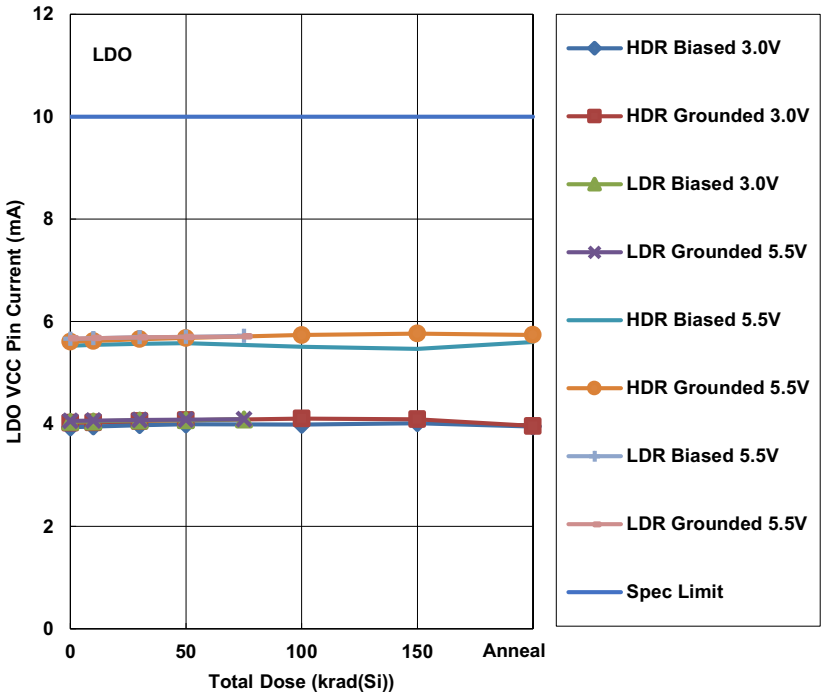

Figure 17. ISL70005SEH LDO VCC pin current as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limit is 10mA maximum.

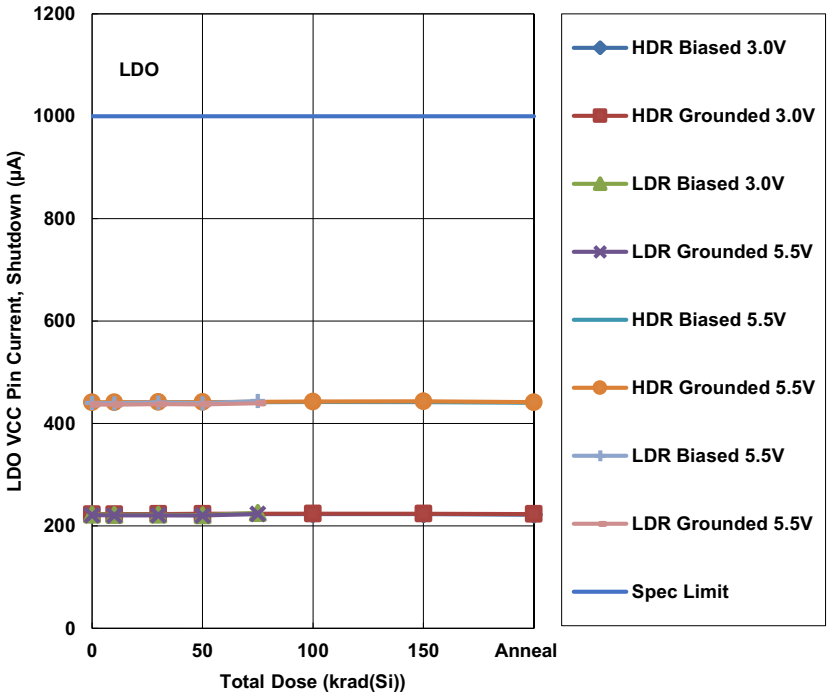

Figure 18. ISL70005SEH LDO VCC pin current in shutdown mode as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limit is 1000µA maximum.

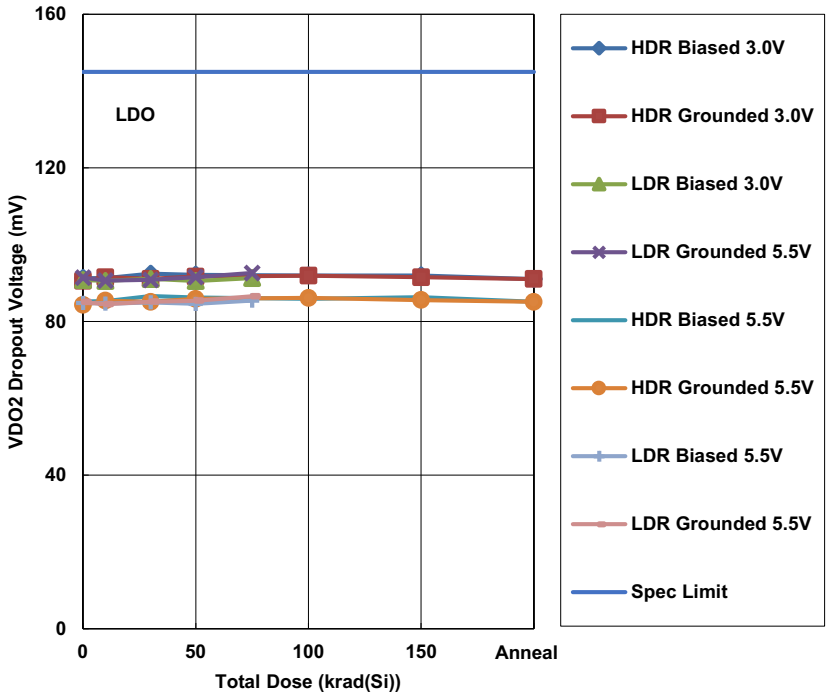

Figure 19. ISL70005SEH LDO VDO2 dropout voltage as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limit is 145mV maximum.

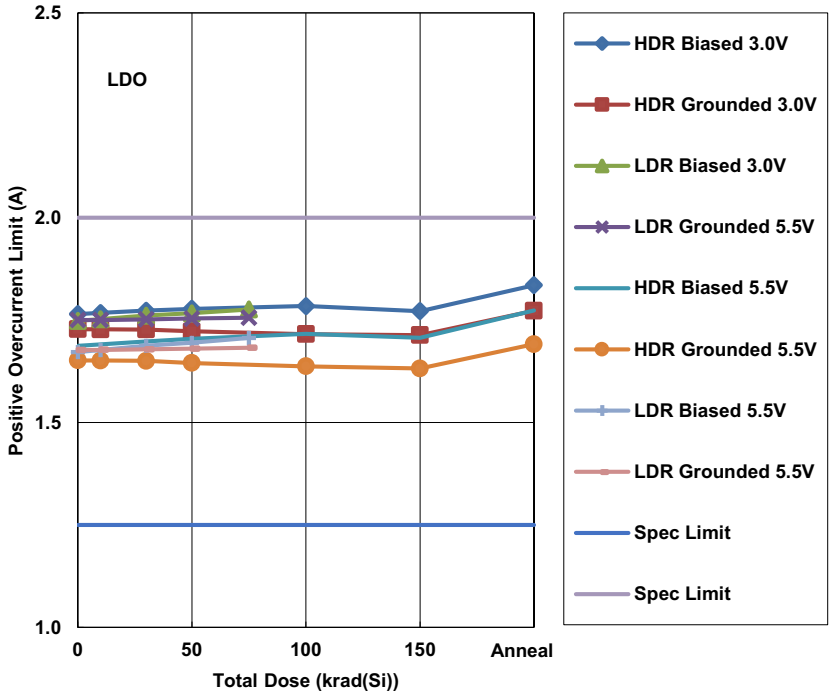

Figure 20. ISL70005SEH LDO positive overcurrent limit as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are 1.25A to 2.0A.

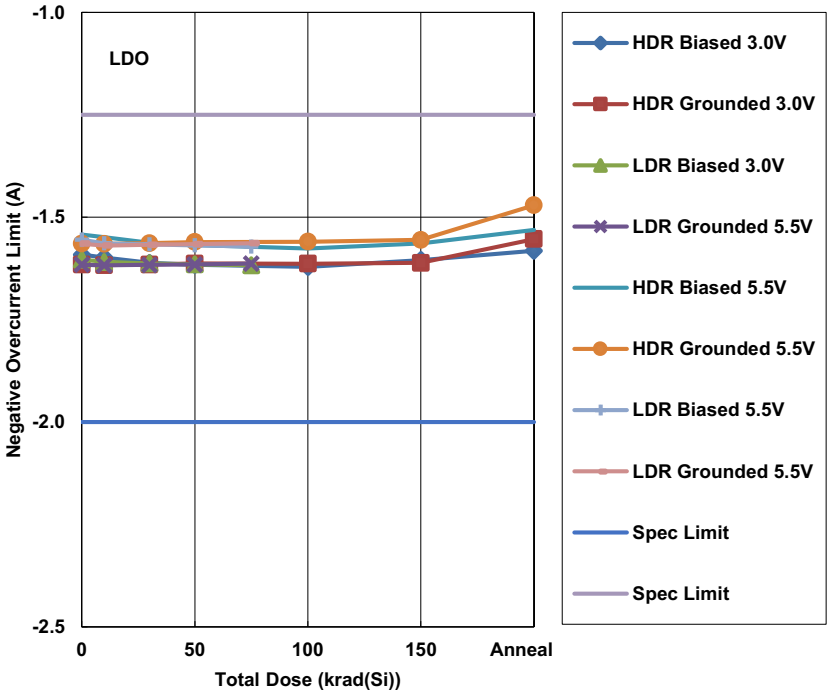

Figure 21. ISL70005SEH LDO negative overcurrent limit as a function of total dose irradiation at LDR and HDR for the unbiased and biased cases. The HDR irradiations were followed by a high temperature anneal at 100°C for 168 hours. The LDR tests were taken to 75krad(Si) and are being continued to 100krad(Si) and through anneal. The LDR was 0.01rad(Si)/s and the HDR was 70rad(Si)/s. Sample sizes are given in Table 1. The SMD limits are -2.0A to -1.25A.

3. Discussion and Conclusion

This interim document reports the results to date of TID testing of the ISL70005SEH radiation hardened dual point-of-load regulator. Parts were tested at LDR and HDR under biased and unbiased conditions, as outlined in MIL-STD-883 TM1019. HDR testing is complete through 150krad(Si) and subsequent high temperature biased anneal. The LDR tests have completed 75krad(Si) and are being continued to 100krad(Si) and through anneal. All samples showed excellent stability over irradiation and anneal, with no observed LDR sensitivity (or HDR sensitivity, for that matter). It should be noted that the SMD pre-irradiation and post-irradiation limits are identical. No differences between biased and unbiased irradiation were noted, and the part is not considered bias sensitive or dose rate sensitive. A detailed discussion of the response of the critical parameters is omitted as a look at the figures show that there was very little change.

4. Appendix

Table 2. Reported Parameters and Figures

Figure	Parameter	SMD Symbol	Low Limit	High Limit	Units
Buck Regulator Section					
3	Operating Supply Current	IOP	-	15	mA
4	Shutdown Supply Current	ISDN	-	3	mA
5	B_VCC Internal UVLO Rising Threshold	PORRT	2.60	2.95	V
6	B_VCC Internal UVLO Falling Threshold	PORFT	2.45	2.80	V
7	Switching Frequency	t_{SF}	85	115	kHz
8	B_LXx Minimum On-Time	t_{ON}	100	240	ns
9	B_LXx Minimum On-Time	t_{ON1}	115	325	ns
10	B_LXx Minimum Off-Time (3V)	t_{OFF}	50	150	ns
	B_LXx Minimum Off-Time (5V)		65	165	ns
11	Reference Voltage Tolerance	$V_{REF} + V_{IO}$	594	606	mV
12	Packaged Upper Device $r_{DS(ON)}$	PURON	80	245	mΩ
13	Packaged Lower Device $r_{DS(ON)}$	PLRON	40	160	mΩ
14	Overcurrent Limit	OCL	4.0	6.4	A
Low Dropout Regulator Section					
15	VREF Voltage	V_{REF}	591	609	mV
16	Regulation Deadband	RegDB	5	15	mV
17	L_VCC Pin Current	I_Q	-	10	mA
18	L_VCC Pin Current in Shutdown	I_{SHDN}	-	1000	µA
19	Dropout Voltage, VDO	VDO2	-	145	mV
20	Positive Overcurrent Limit	LOCLP	1.25	2.0	A
21	Negative Overcurrent Limit	LOCLN	-2.0	-1.25	A

5. Revision History

Rev.	Date	Description
1.00	Jan.15.20	Initial release

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