HS-26C32EH

Total Dose Test

TR058
Rev.0.00
Jan 5, 2018

Introduction

This report describes the results of Low Dose Rate (LDR) total dose testing of the HS-26C32EH quad differential line receiver. The data originated from routine production wafer-by-wafer acceptance testing of the part.

Two versions of the HS-26C32 are available. The base HS-26C32RH is acceptance tested on a wafer-by-wafer basis to 300krad(Si) at High Dose Rate (HDR), as defined in MIL-STD-883 test method 1019 (50–300rad(Si)/s). The HS-26C32EH is acceptance tested on a wafer-by-wafer basis to 300krad(Si) at HDR and to 50krad(Si) at LDR, also as defined in MIL-STD-883 test method 1019 (0.01rad(Si)/s maximum). The HS-26C32RH and HS-26C32EH are identical parts and differ only in radiation lot acceptance testing (RLAT) procedures.

Product Description

The HS-26C32RH and HS-26C32EH are differential line receivers designed for digital data transmission over balanced lines and meet the requirements of EIA Standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments. The HS-26C32RH and HS-26C32EH have a typical input sensitivity of 200mV over the common-mode input voltage range of ±7V. The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to logic “1” when the inputs are open. Enable and Disable functions are common to all four receivers.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency, Land and Maritime (DLA). The SMD number listed in this report must be used when ordering. Detailed electrical specifications for these devices are contained in SMD 5962-95689.

Related Literature

- MIL-STD-883G test method 1019.7
- For a full list of related documents, visit our website
  - HS-26C32EH product page

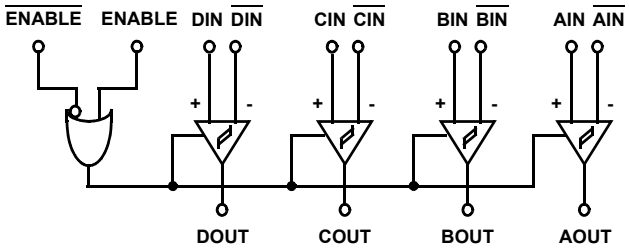

Figure 1. HS-26C32EH Block Diagram

1. Test Description

1.1 Irradiation Facilities

All data was derived from wafer acceptance testing results. LDR irradiation was performed at 0.010rad(Si)/s per MIL-STD-883 Method 1019.7, using the Intersil N40 panoramic irradiator.

1.2 Test Fixturing

Figure 2 shows the configuration used for biased irradiation in conformance with Standard Microcircuit Drawing (SMD) 5962-95689.

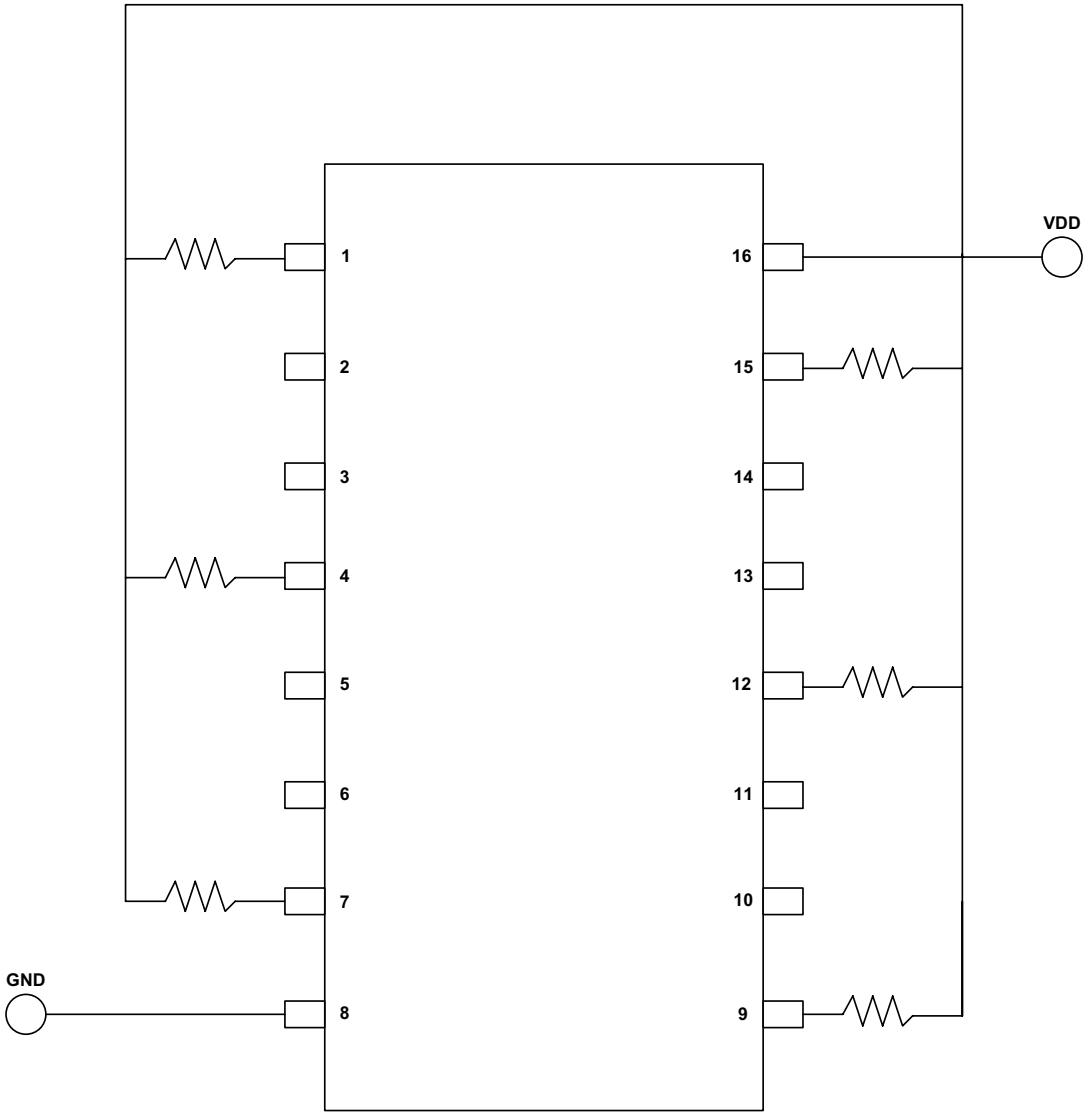

Figure 2. Irradiation Bias Configuration

Notes:

1. VDD = +5V ±5%
2. GND = ground
3. All resistors are 47kΩ ± 5%
4. Use generic 16-pin universal board
5. Use patch labeled HS26C32

1.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature using the production Automated Test Equipment (ATE), with datalogging at each downpoint.

1.4 Experimental Matrix

The experimental matrix consisted of 16 samples irradiated at LDR with all pins grounded and 16 samples irradiated at LDR under bias. All samples were part of the wafer-by-wafer acceptance testing procedure. Samples of the HS-26C32EH die were drawn from production lot G2A0PEH and were packaged in the standard hermetic 16-Ld flatpack (CDFP4-F16) production package. Samples were processed through the standard burn-in cycle before irradiation and were screened to the SMD limits at room, low, and high temperatures before the test.

2. Results

2.1 Attributes Data

Testing of the HS-26C32EH at LDR showed no rejected devices after irradiation, screening to the SMD limits. The SMD specifies that the part will meet all pre-irradiation limits post-irradiation because the pre-irradiation limits and post-irradiation limits are the same. No bias sensitivity was noted.

Table 1. HS-26C32EH Total Dose Test Attributes Data

Dose Rate	Bias	Sample Size	Downpoint	Bin 1 (Note 6)	Rejects
0.01rad(Si)/s	Figure 2	16	Pre-irradiation	16	
			50krad(Si)	16	0
			100krad(Si)	16	0
0.01rad(Si)/s	Grounded	16	Pre-irradiation	16	
			50krad(Si)	16	0
			100krad(Si)	16	0

Note:

6. Bin 1 indicates a device that passes all pre-irradiation specification limits.

2.2 Variables Data

The plots in Figures 3 through 21 show data at all downpoints. Most of the plots show the individual total dose response of each of the four channels. Note that error bars are not supplied for this data because the distributions were tight enough to render this unnecessary.

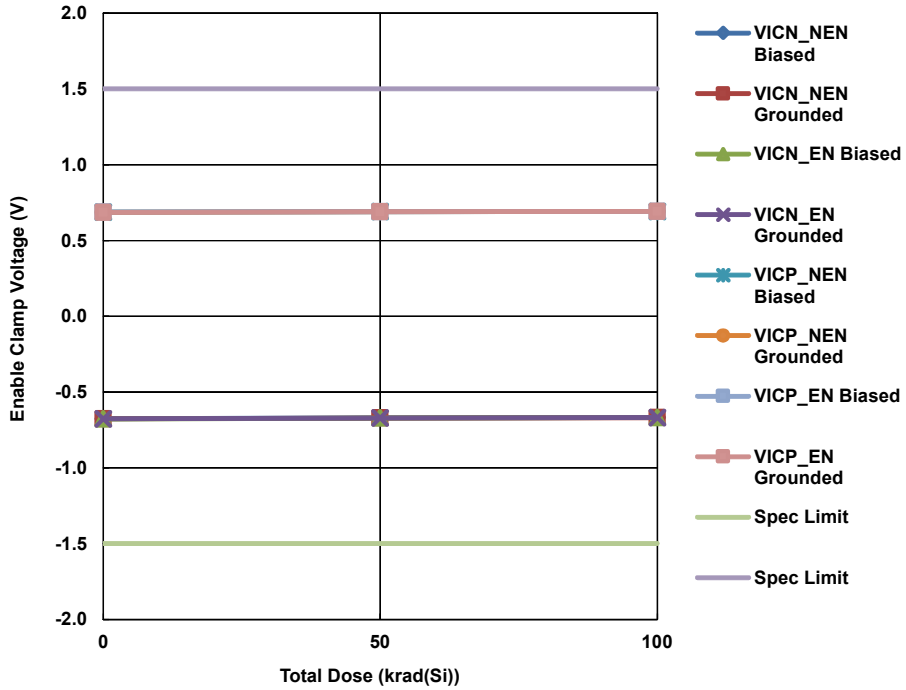

Figure 3. HS-26C32EH enable input clamp voltage as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limits are -1.5V to 1.5V.

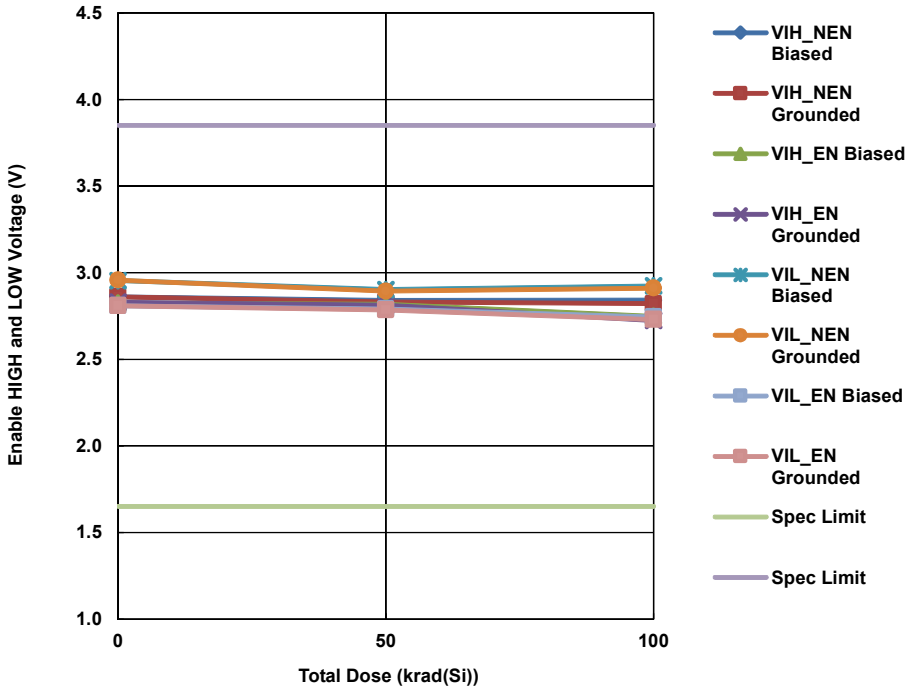

Figure 4. HS-26C32EH enable HIGH and LOW input voltage as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limit is 3.85V maximum (enable HIGH voltage) and 1.65V minimum (enable LOW input voltage).

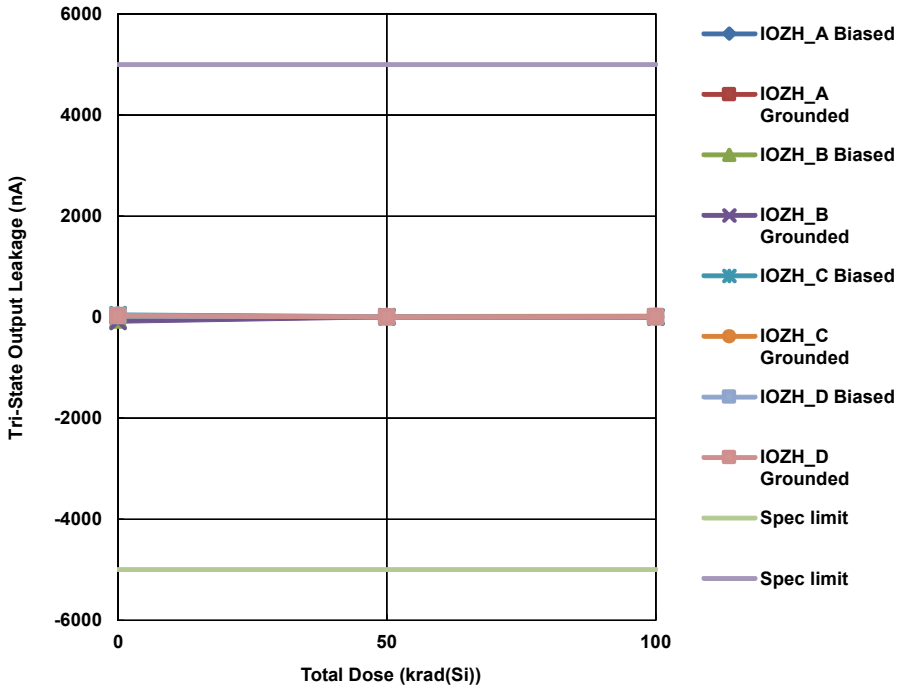

Figure 5. HS-26C32EH tristate output leakage, output at VDD, each channel, as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limits are -5000nA (-5µA) to +5000nA (+5µA).

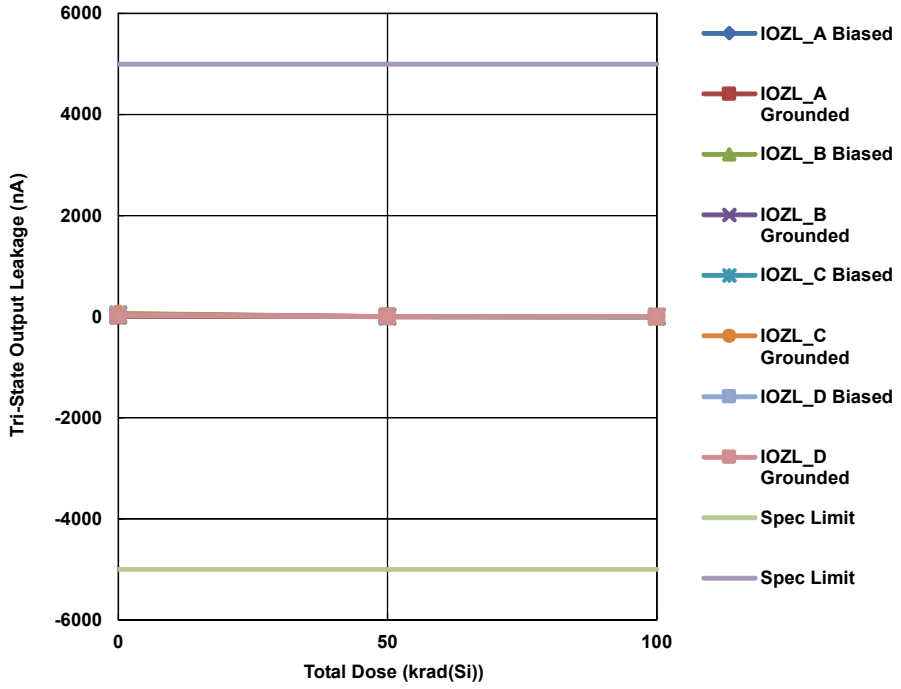

Figure 6. HS-26C32EH tristate output leakage, output at ground, each channel, as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limits are -5000nA (-5µA) to +5000nA (+5µA).

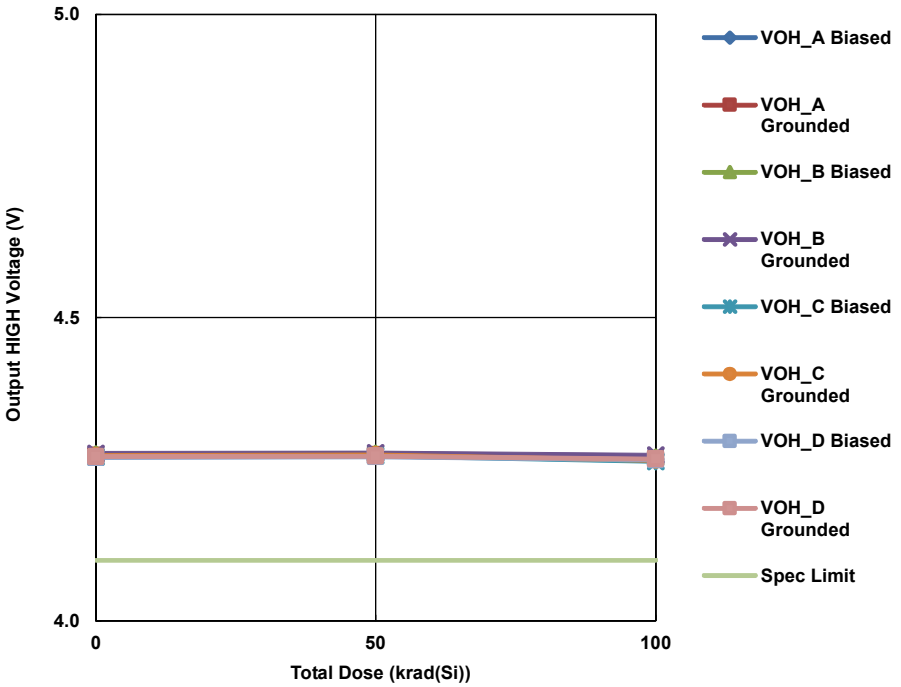

Figure 7. HS-26C32EH output HIGH voltage, each channel, as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limit is 4.1V minimum.

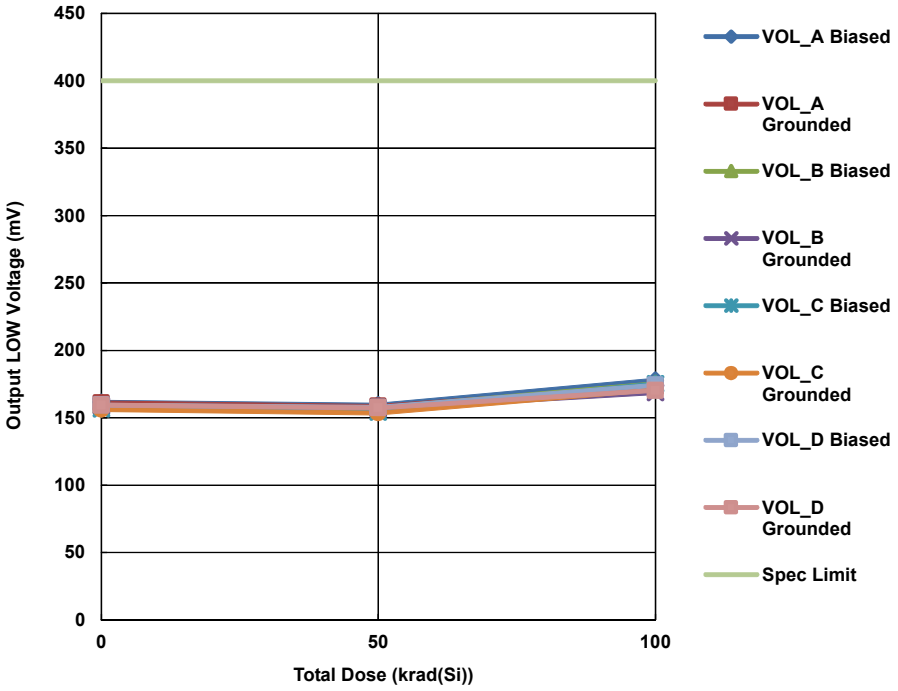

Figure 8. HS-26C32EH output LOW voltage, each channel, as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limit is 400mV maximum.

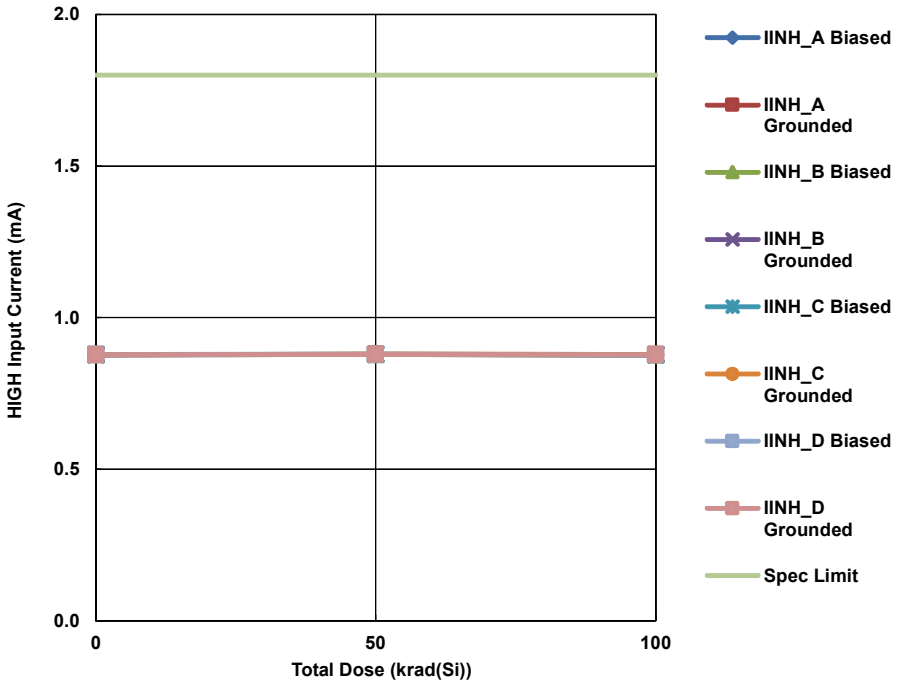

Figure 9. HS-26C32EH input HIGH current, each channel, as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limit is 1.8mA maximum.

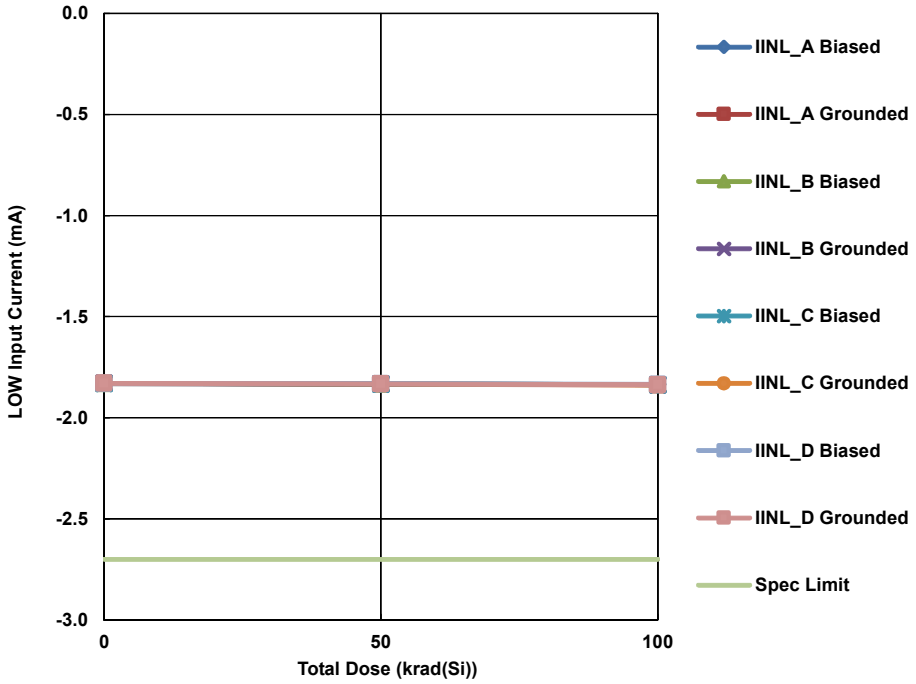

Figure 10. HS-26C32EH input LOW current, each channel, as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limit is -2.7mA minimum.

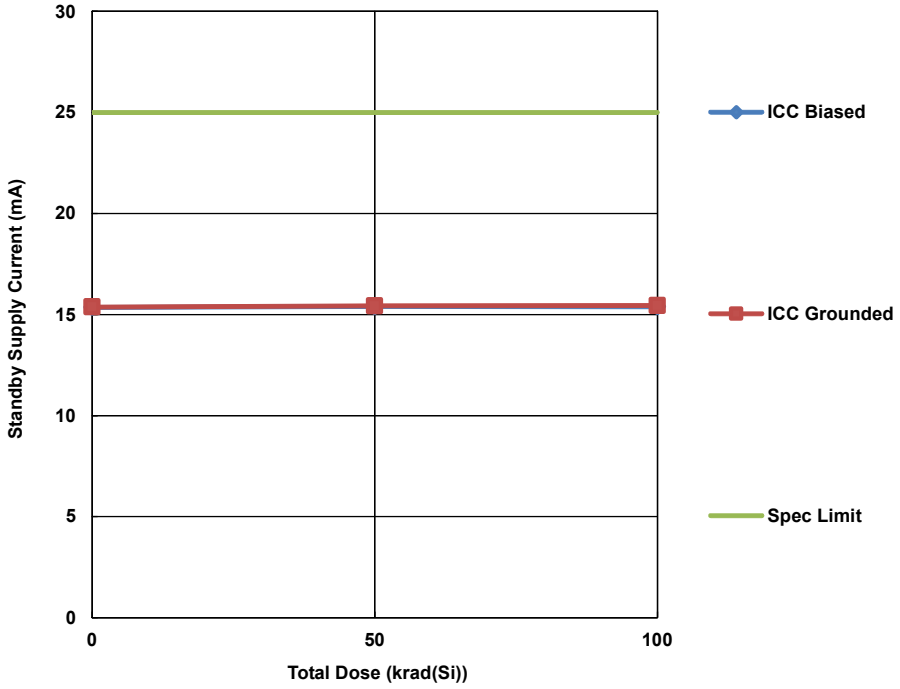

Figure 11. HS-26C32EH standby supply current as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limit is 25mA maximum.

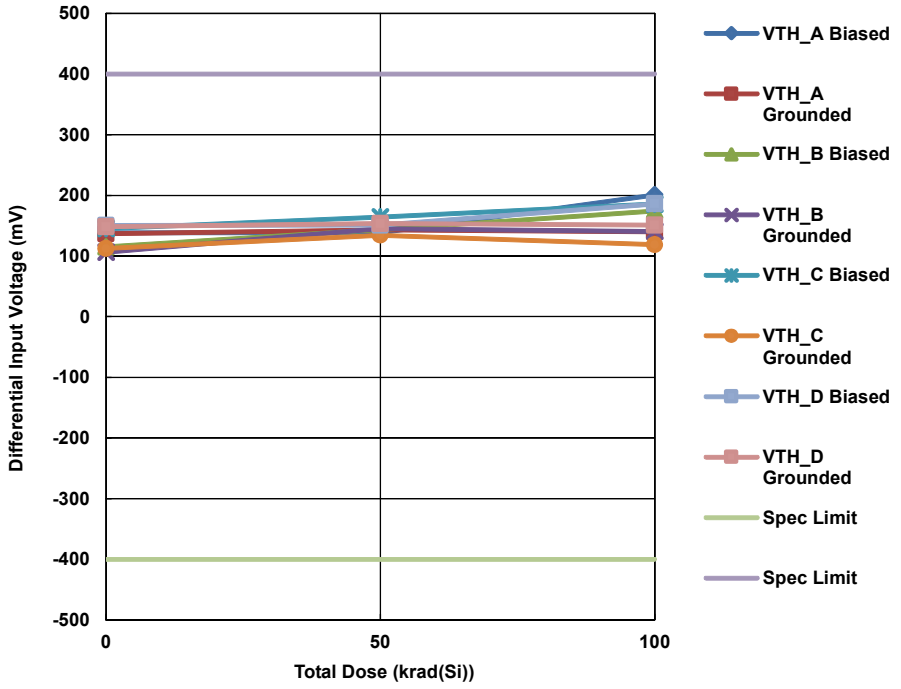

Figure 12. HS-26C32EH differential input voltage, each channel, as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limits are -400mV to 400mV.

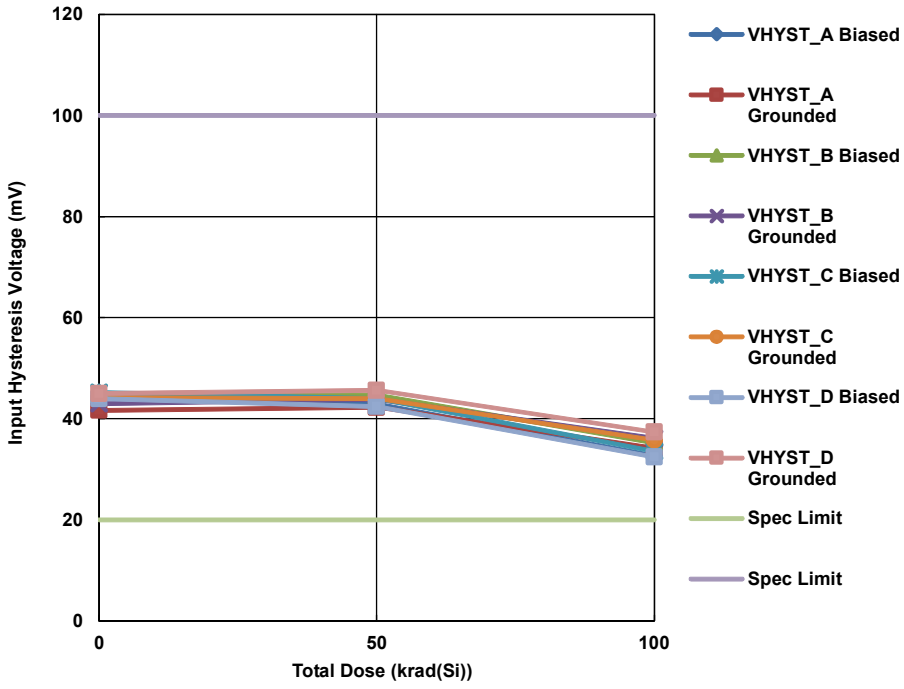

Figure 13. HS-26C32EH input hysteresis voltage, each channel, as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limits are 20mV to 100mV.

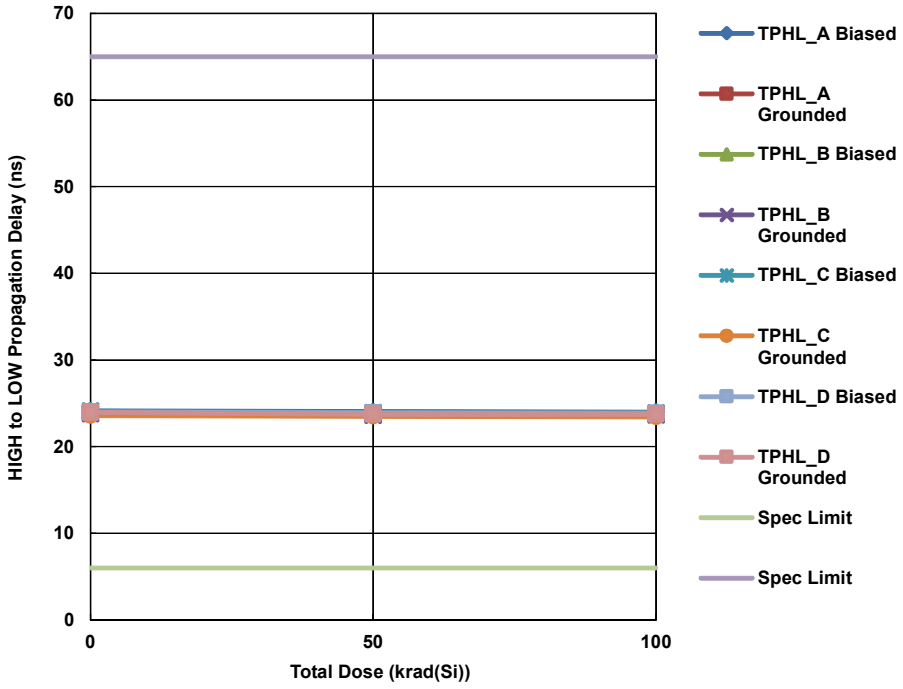

Figure 14. HS-26C32EH HIGH to LOW propagation delay as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limits are 6ns to 65ns.

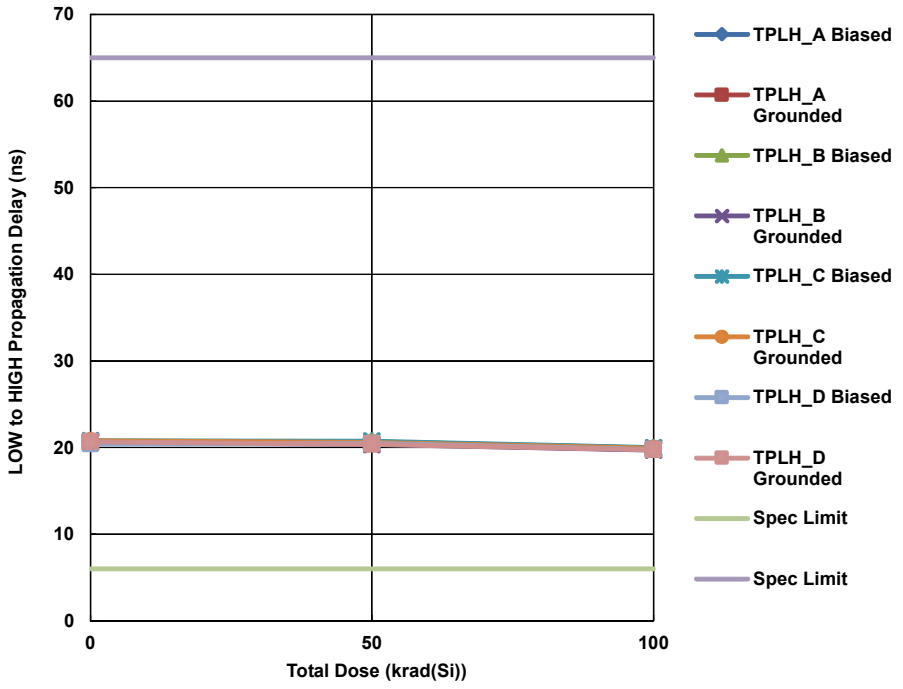

Figure 15. HS-26C32EH LOW to HIGH propagation delay as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limits are 6ns to 65ns.

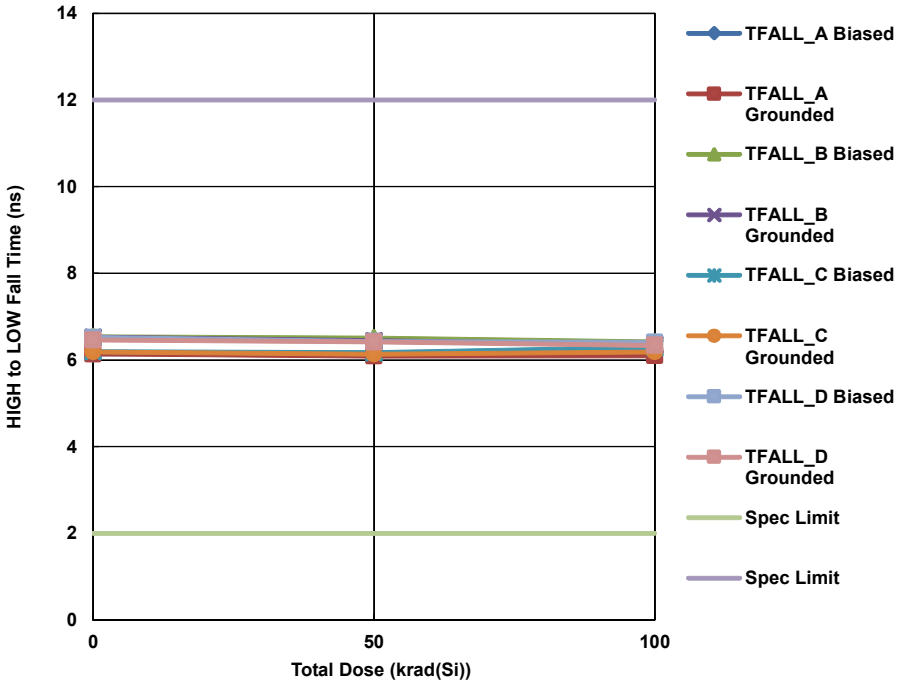

Figure 16. HS-26C32EH HIGH to LOW output fall time as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limits are 2ns to 12ns.

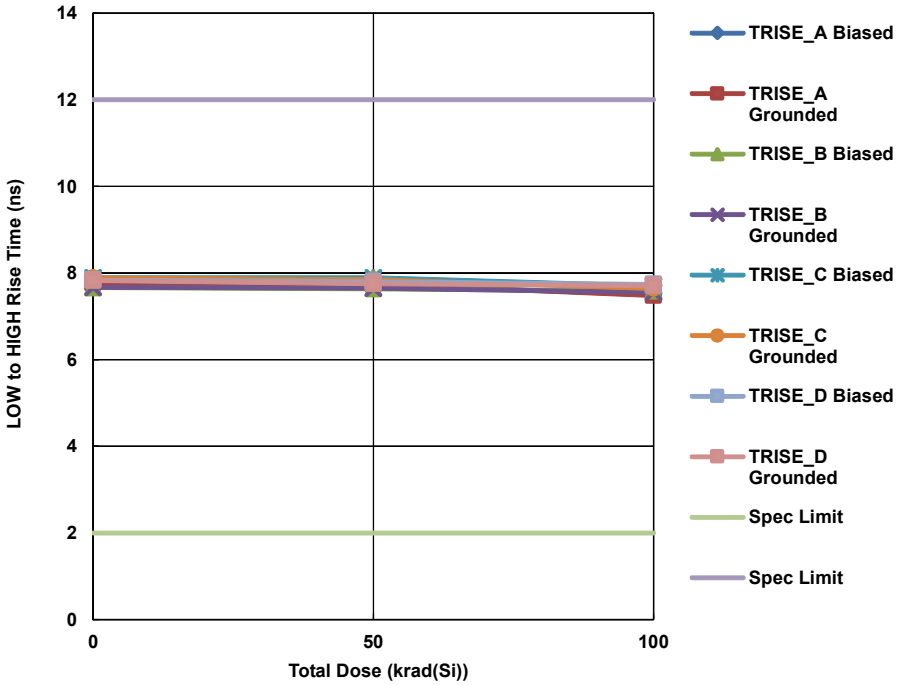

Figure 17. HS-26C32EH LOW to HIGH output rise time as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limits are 2ns to 12ns.

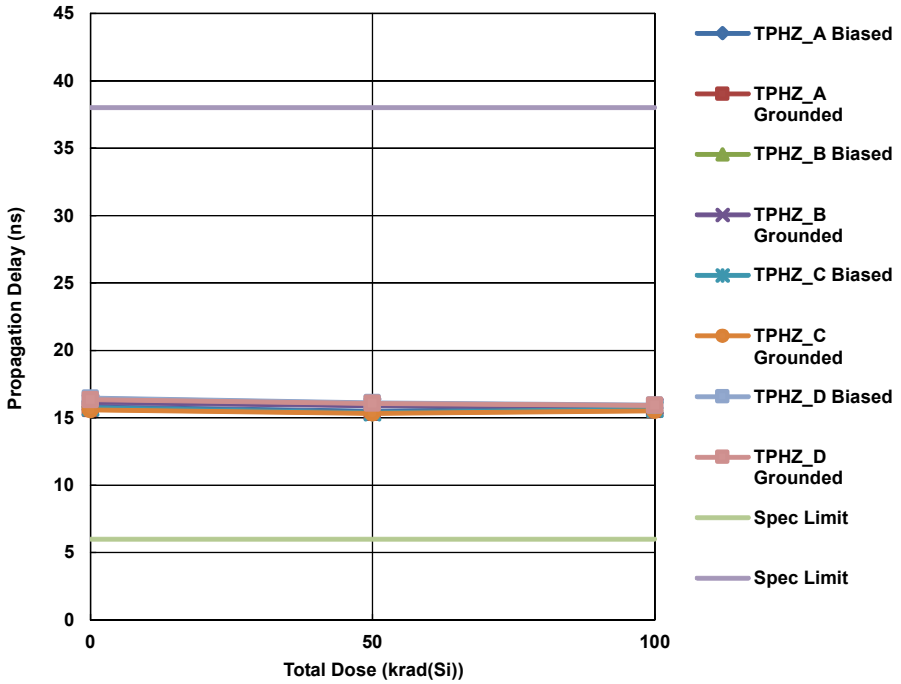

Figure 18. HS-26C32EH propagation delay, HIGH to tristate, as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limits are 6ns to 38ns.

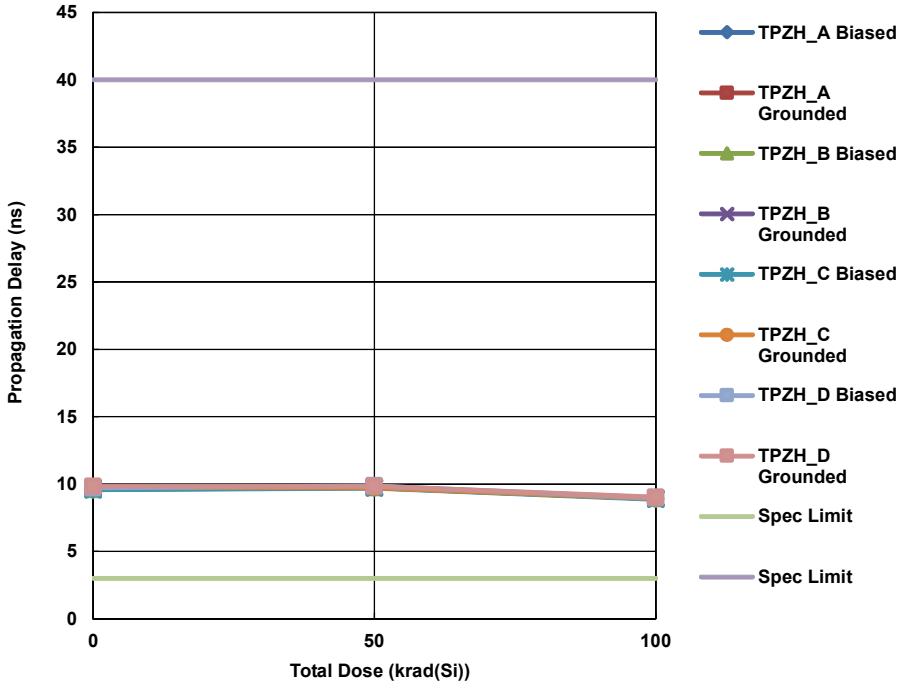

Figure 19. HS-26C32EH propagation delay, tristate to HIGH, as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limits are 3ns to 40ns.

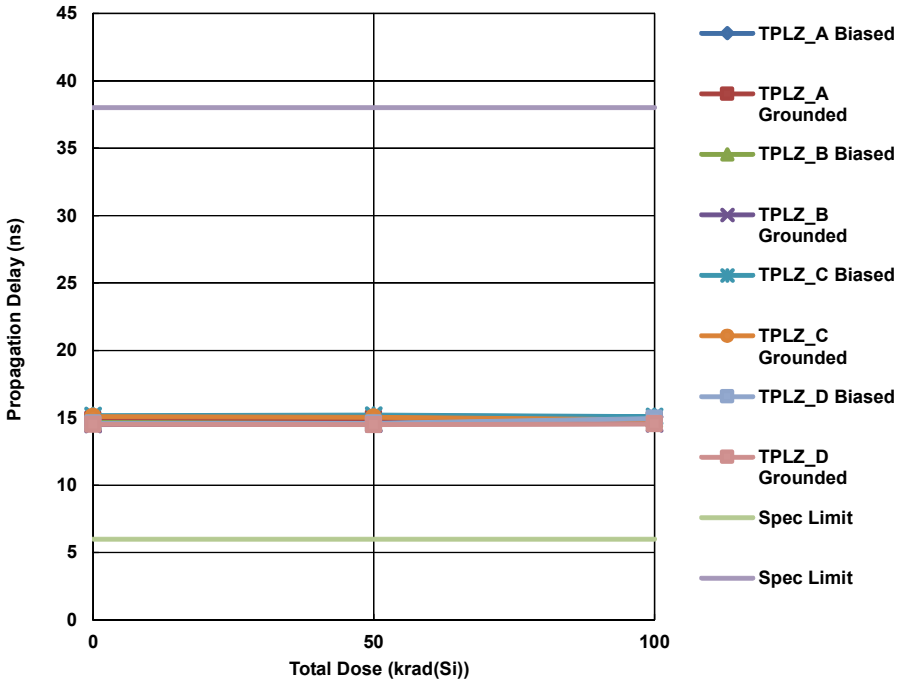

Figure 20. HS-26C32EH propagation delay, LOW to tristate, as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limits are 6ns to 38ns.

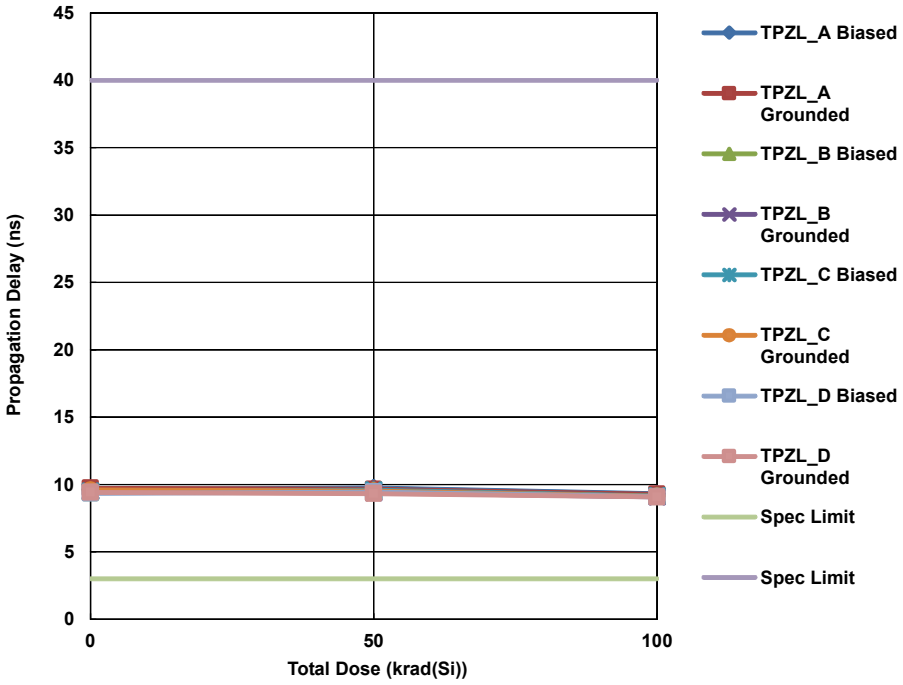

Figure 21. HS-26C32EH propagation delay, tristate to LOW, as a function of biased (Figure 2) and unbiased (grounded) LDR irradiation to 100krad(Si). The sample size for each of the LDR cells was 16. The SMD limits are 3ns to 40ns.

3. Conclusion

This report describes the results of a total dose test of the HS-26C32EH quad differential line receiver. Parts were irradiated at LDR under biased and unbiased conditions as part of routine production acceptance testing, to a total dose of 100krad(Si). Testing showed zero reject devices to the SMD pre-radiation limits, noting that the post-radiation limits are the same as the pre-radiation limits for this part. No bias sensitivity was noted.

4. Appendices

4.1 Reported Parameters

Figure	Parameter	Limit, Low (Note 7)	Limit, High (Note 7)	Units	Notes
3	Enable Input Clamp Voltage	-1.5	1.5	V	
4	Enable HIGH Input Voltage	-	3.85	V	
	Enable LOW Input Voltage	1.65	-	mV	
5	Tristate Output Leakage	-5000	5000	nA	Output at VDD
6	Tristate Output Leakage	-5000	5000	nA	Output at ground
7	Output HIGH Voltage	4.1	-	V	
8	Output LOW Voltage	-	400	mV	
9	Input HIGH Current	-	1.8	mA	
10	Input LOW Current	-2.7	-	mA	
11	Standby Supply Current	-	25	mA	
12	Differential Input Voltage	-400	400	mV	
13	Input Hysteresis	20	100	mV	
14	HIGH to LOW Propagation Delay	6	65	ns	
15	LOW to HIGH Propagation Delay	6	65	ns	
16	Output Fall Time	2	12	ns	
17	Output Rise Time	2	12	ns	
18	Propagation Delay	6	38	ns	HIGH to tri-state
19	Propagation Delay	3	40	ns	Tri-state to HIGH
20	Propagation Delay	6	38	ns	LOW to tri-state
21	Propagation Delay	3	40	ns	Tri-state to LOW

Note:

7. These limits are taken from Standard Microcircuit Drawing (SMD) 5962-95689, with additional guardbanding for some parameters.

5. Revision History

Rev.	Date	Description
0.00	Jan 5, 2018	Initial release

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

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80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
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Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
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Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
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