# HS-1825AEH

Total Dose Testing

AN1823
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## Introduction

This report summarizes the results of a low dose rate (LDR), total dose test of the HS-1825AEH current mode PWM controller. The test was specifically conducted in order to determine the total dose sensitivity under low dose rate conditions.

Both the HS-1825ARH and HS-1825AEH are acceptance tested on a wafer-by-wafer basis to 300krad(Si) at high dose rate (50 to 300 rad(Si)/s). Only the HS-1825AEH is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate (0.01 rad(Si)/s). The LDR performance characterization beyond the 50krad(Si) assurance level is included in this report as indicative, but no assurance testing beyond 50krad(Si) is performed at LDR in production.

## Reference Documents

- MIL-STD-883G test method 1019.7
- MIL-PRF-38535 (QML)
- HS-1825AEH data sheet
- DLA Standard Microcircuit Drawing (SMD) 5962-99558

## Part Description

The HS-1825ARH, HS-1825AEH pulse width modulator is designed to be used in high frequency switched-mode power supplies and can be used in either current-mode or voltage-mode. It is well suited for single-ended boost converter applications.

Device features include a precision voltage reference, low power start-up circuit, high frequency oscillator, wide-band error amplifier, and fast current-limit comparator. The use of proprietary process capabilities and unique design techniques results in fast propagation delay times and high output current over a wide range of output voltages.

Constructed with the Intersil Rad Hard Silicon Gate (RSG), Dielectric Isolation BiCMOS process, the HS-1825ARH, HS-1825AEH have been specifically designed to provide highly reliable performance when exposed to harsh radiation environments.

- Electrically screened to DLA SMD 5962-99558
- QML qualified per MIL-PRF-38535 requirements
- Maximum high dose rate total dose . . . . . . . . . . 300krad(Si)
- Vertical architecture provides low dose rate immunity
- Dielectric isolation process (RSG) provides latch-up immunity
- Low start-up current. . . . . . . . . . . . . . . . . . . . . . . . 100µA (Typ)
- Fast propagation delay . . . . . . . . . . . . . . . . . . . . . . 80ns (Typ)
- 12V to 30V operation
- 1A (peak-to-peak) dual output drive capability
- 5.1V reference
- Undervoltage lock-out (UVLO)
- Programmable soft-start
- Switching frequencies . . . . . . . . . . . . . . . . . . . . . . . . .500kHz
- Latched overcurrent comparator with full cycle restart

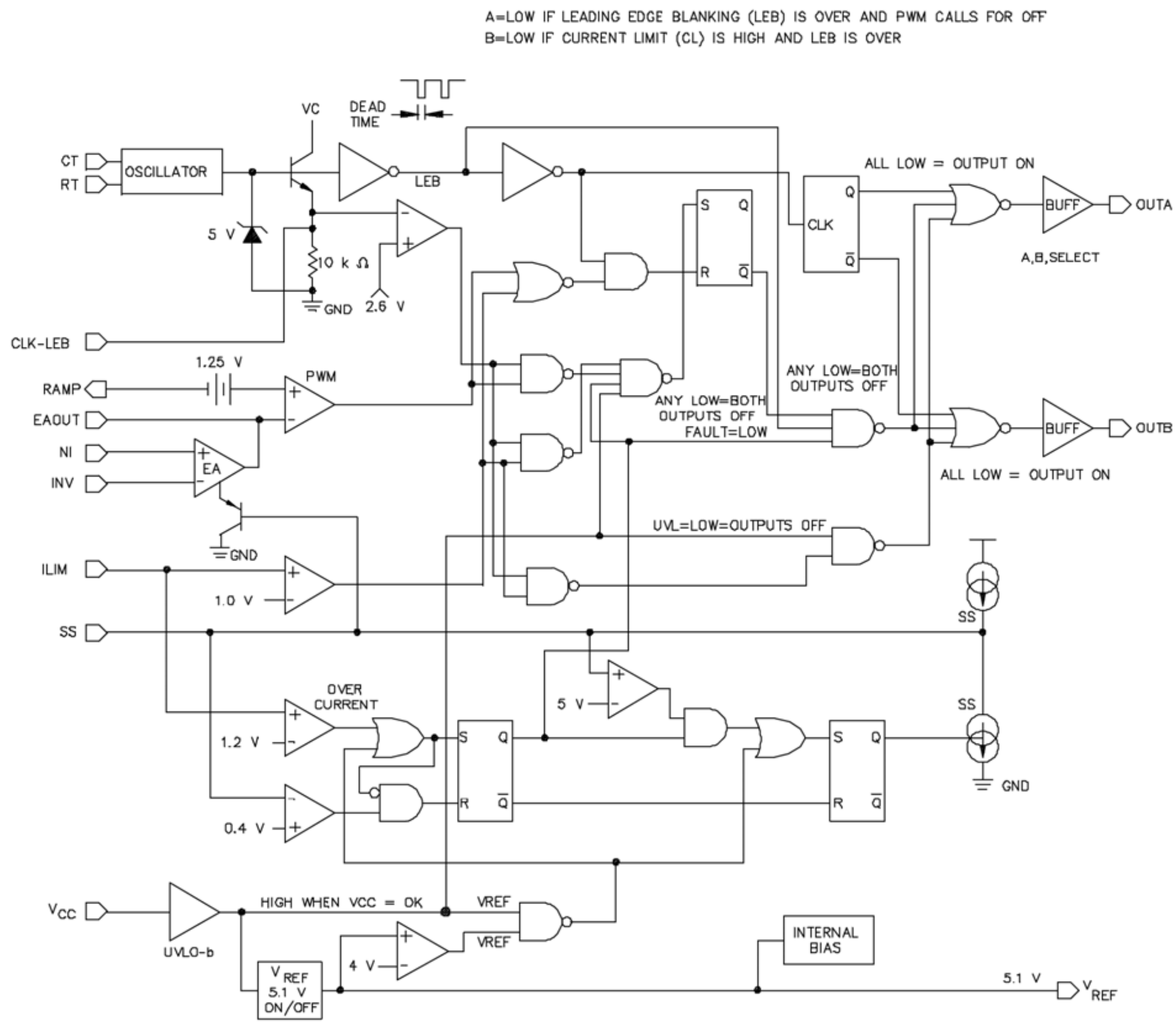



**FIGURE 1. HS-1825AEH CONCEPTUAL BLOCK DIAGRAM**

The HS-1825AEH is implemented in Intersil's dielectrically isolated radiation hardened silicon gate BiCMOS technology (RSG). Active devices include 30V CMOS and complementary bipolar transistors. The process in production is under MIL PRF 38535 certification and is used for a range of space qualified products.

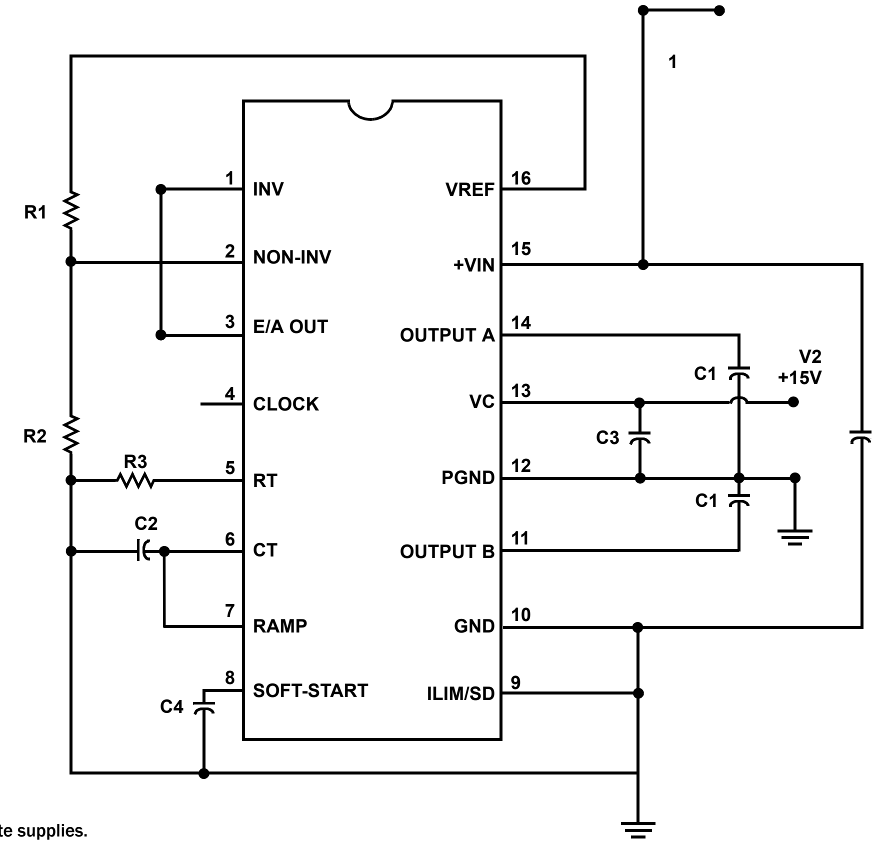
# Test Description

## Irradiation Facilities

Low dose rate testing was done at Intersil's low dose rate irradiation facility located in Palm Bay, FL. This facility was built expressly for supporting production (LDR assurance testing) of Intersil products. A description of the Intersil LDR facility can be found on the Intersil web site. The facility uses a $^{60}$Co source and maintains a 10mrad(Si)/s flux by device positioning relative to the source. Devices are packaged in PbAl boxes to shield them against low energy secondary gamma radiation, as required by MIL STD 883.

## Test Fixturing

Figure 2 on page 3 shows the configuration used for biased irradiation in conformance with Standard Microcircuit Drawing (SMD) 5962-99558. This configuration was used for the biased low dose rate irradiation. The unbiased low dose rate irradiation was carried out with all pins grounded.




NOTE: V1 and V2 are separate supplies.
V1, V2 = 15V, ±0.5V
R1 = 6kΩ, ±5%, R2 = 10kΩ, ±5%, R3 = 10kΩ, ±1%
C1 = 250pF, ±5%, C2 = 1000pF, ±5%, C3 = 1µF, ±10%
C4 = 0.1µF, ±10%

**FIGURE 2. IRRADIATION BIAS CONFIGURATION FOR THE HS-1825AEH PER STANDARD MICROCIRCUIT DRAWING (SMD) 5962-99558, AS USED FOR BOTH LOW DOSE RATE IRRADIATION REPORTED IN THIS DOCUMENT**

## Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production automated test equipment (ATE) with data-logging of all parameters at each downpoint. Electrical testing was performed at room temperature.

## Experimental Matrix

The experimental matrix consists of two irradiation groups; biased and unbiased, and a sequence of dose downpoints. Units were cumulatively dosed up to the maximum dose listed; Table 1 summarizes the test points and identifies the number of units tested for each condition. The number of samples in the unbiased condition changes from 18 to 10. This was due to electrical overstress damage incurred during testing the devices.

**TABLE 1. NUMBER OF UNITS TESTED AT EACH CONDITION**

| | 0 krad | 50 krad | 100 krad | 150 krad | 200 krad |
|---|---|---|---|---|---|
| Biased | 18 | 18 | 18 | 18 | – |
| Unbiased | 18 | 18 | 10 | 10 | 10 |

NOTE: The dose downpoints are sequential on the units left to right.

Samples of the HS-1825AEH were drawn from pre-production inventory for the HS-1825ARH and were packaged in the standard hermetic 16-pin ceramic flatpack (CFP) production package. Samples were processed through the standard burn-in cycle before irradiation, as required by MIL-STD-883 and were screened to the SMD 5962-99558 limits at room, low and high temperature before the radiation testing.

## SMD Electrical Parameter Results

Results for the key parameters are presented in Figures 3 through 37 for all downpoints. The plots show the median parameter values as connected points against total dose. The median values are augmented with markers at each of the extremes recorded. Table 2 lists the SMD parameters, limits, plus chart number and page. Some redundant test data and SMD parameters were omitted from the charts. These omitted charts added no information beyond those included.

TABLE 2. SMD PARAMETERS, LIMITS PLUS CHART NUMBER AND PAGE

| SMD ELECTRICAL PARAMETER | SYMBOL | PRE/POST RADIATION LIMITS +25°C | | | CHART NO. & PG. |
|---|---|---|---|---|---|
| | | MIN | MAX | UNIT | |
| Reference Output Voltage | $V_{REF}$ | 5.05/5.00 | 5.15/5.20 | V | 3, 5 |
| Reference Line Regulation | $V_{LINE}$ | -15/-20 | 15/20 | mV | 4, 5 |
| Reference Load Regulation | $V_{LOAD}$ | -25/-50 | 25/50 | mV | 5, 6 |
| Reference Total Output Variation | $V_{OM}$ | 5.00/4.95 | 5.20/5.25 | mV | |
| Reference Short Circuit Current | $I_{SC}$ | 30/20 | | mA | 6, 6 |
| Oscillatory Initial Accuracy | $F_O$ | 350/300 | 425 | kHz | 7, 6 |
| Oscillatory Voltage Stability | $dF_O/dV$ | -2/-3 | 2/3 | % | 8, 6 |
| Oscillatory Total Variation | $F_{OM}$ | 350/300 | 425 | kHz | |
| Clock Out High Voltage | $V_{CLKH}$ | 4.00/3.75 | | V | 9, 7 |
| Clock Out Low Voltage | $V_{CLKL}$ | | 0.2 | V | 10, 7 |
| E/A Input Offset Voltage | $V_{OS}$ | -10 | 10 | mV | 11, 7 |
| E/A Input Bias Current | $I_{IB}$ | -1 | 1 | µA | 12, 7 |
| E/A Amplifier Input Offset Current | $I_{OS}$ | -4 | 4 | µA | 13, 8 |
| E/A Open Loop Gain | $A_{VOL}$ | 60 | | dB | 14, 8 |
| E/A Common Mode Rejection Ratio | CMRR | 65 | | dB | 15, 8 |
| E/A Power Supply Rejection Ratio | PSRR | 80 | | dB | 16, 8 |
| E/A Output Sink Current | $I_{OSK}$ | 1 | | mA | 17, 9 |
| E/A Output Source Current | $I_{OSC}$ | -0.5 | | mA | 18, 9 |
| E/A Output High Voltage | $V_{OH1}$ | 4.0 | | V | 19, 9 |
| E/A Output Low Voltage | $V_{OL1}$ | | 1.0 | V | 20, 9 |
| PWM Ramp Bias Current | $I_{RAMP}$ | | -8 | µA | 21, 10 |
| PWM Duty Cycle Range | $D_{CRNG}$ | 40 | | % | 22, 10 |
| PWM E/A Out Zero DC Threshold | $V_{TH}$ | 0.89 | | V | 23, 10 |
| Soft-Start Charge Current | $I_{CHG}$ | 8 | 20/25 | µA | 24, 10 |
| Soft-Start Discharge Current | $I_{DCHG}$ | 0.1 | 0.5 | mA | 25, 11 |
| Overcurrent Restart Threshold | $V_{RS}$ | | 0.5 | V | 26, 11 |
| $I_{LIM}$ Bias Current | $I_{BLIM}$ | | 15 | µA | 27, 11 |
| Current Limit Threshold | $V_{LIMIT}$ | 0.95/0.88 | 1.10 | V | 28, 11 |
| Overcurrent Threshold | $V_{OVER}$ | 1.14/1.08 | 1.26 | V | 29, 12 |
| Output Low Saturation 1 | $V_{SATL1}$ | | 0.8 | V | |
| Output Low Saturation 2 | $V_{SATL2}$ | | 2.2 | V | 30, 12 |
| Output High Saturation 1 | $V_{SATH1}$ | 10 | | V | |
| Output High Saturation 2 | $V_{SATH2}$ | 9 | | V | 31, 12 |
| UVLO Output Low Saturation | $V_{OLS}$ | | 1.2 | V | 32, 12 |

TABLE 2. SMD PARAMETERS, LIMITS PLUS CHART NUMBER AND PAGE (Continued)

| SMD ELECTRICAL PARAMETER | SYMBOL | PRE/POST RADIATION LIMITS +25°C | | | CHART NO. & PG. |
|---|---|---|---|---|---|
| | | MIN | MAX | UNIT | |
| UVLO Start Threshold | $V_{START}$ | 8.4 | 9.6 | V | 33, 13 |
| UVLO Stop Threshold | $V_{STOP}$ | | 9.6 | V | 34, 13 |
| UVLO Hysteresis | $V_{HYS}$ | 0.3 | 1.2 | V | 35, 13 |
| Start-Up Current | $I_{SU}$ | | 300 | µA | 36, 13 |
| Supply Current | $I_{CC}$ | | 36 | mA | 37, 14 |

NOTE: Not all parameters have charts.

## Parameter Results

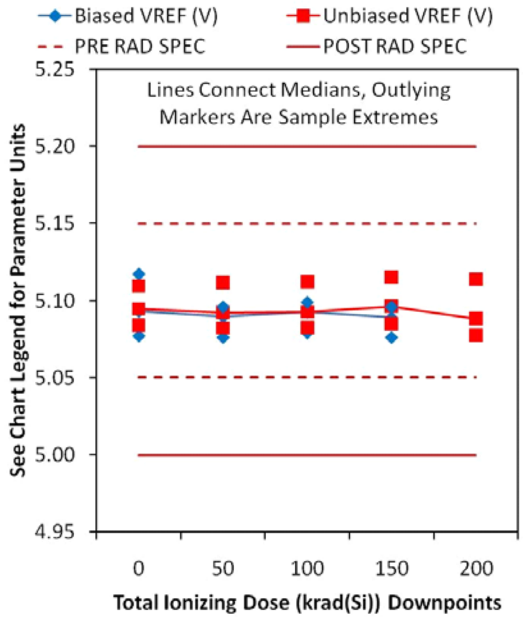



FIGURE 3. REFERENCE OUTPUT VOLTAGE, $V_{REF}$. THE REFERENCE TOTAL OUTPUT VARIATION, $V_{OM}$, CLOSELY MATCHES $V_{REF}$, SO IT IS NOT INCLUDED AS A SEPARATE CHART

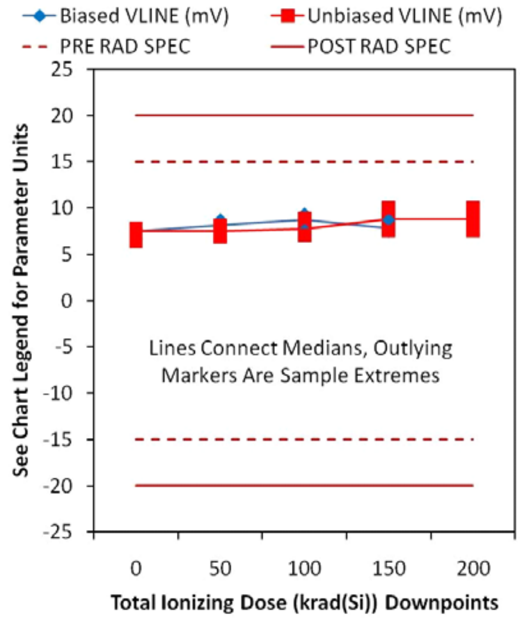



FIGURE 4. REFERENCE VOLTAGE LINE REGULATION, $V_{LINE}$

# Parameter Results (Continued)

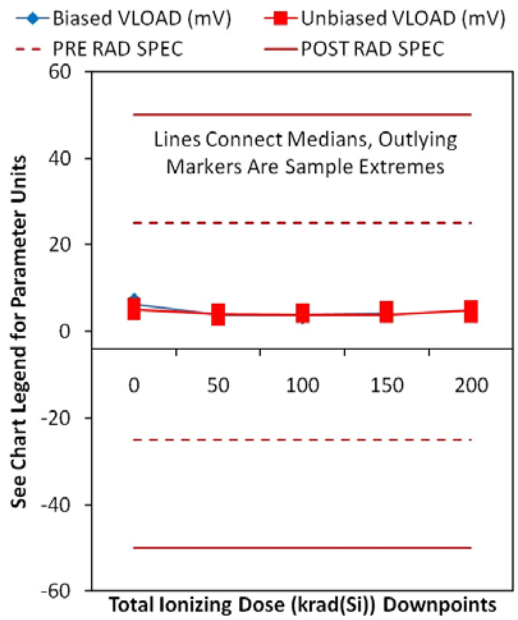



FIGURE 5. REFERENCE VOLTAGE LOAD REGULATION, $V_{LOAD}$

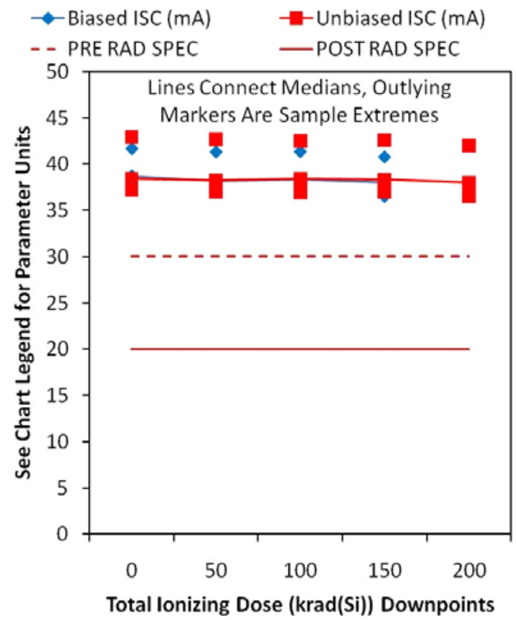



FIGURE 6. REFERENCE SHORT CIRCUIT CURRENT, $I_{SC}$

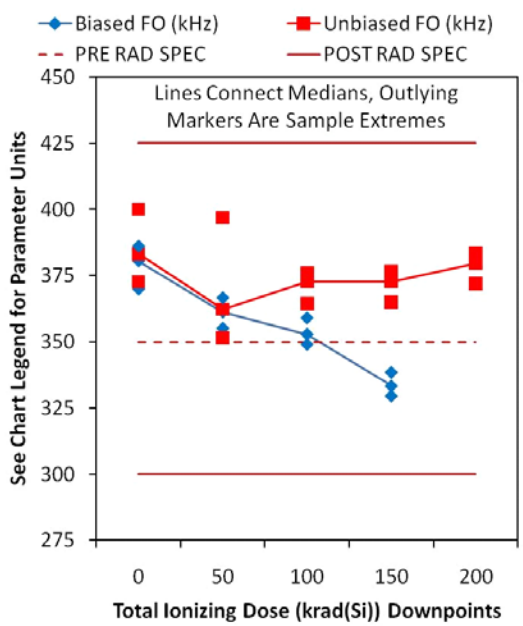



FIGURE 7. OSCILLATOR INITIAL FREQUENCY, $F_O$

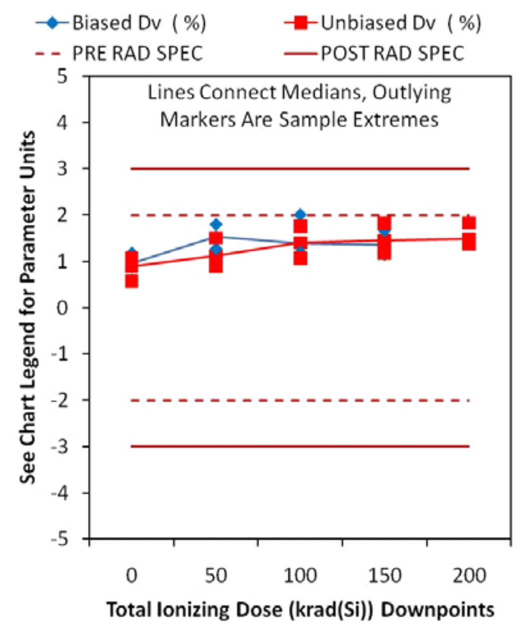



FIGURE 8. OSCILLATOR FREQUENCY VOLTAGE STABILITY, $dF_O/dV$

## Parameter Results (Continued)

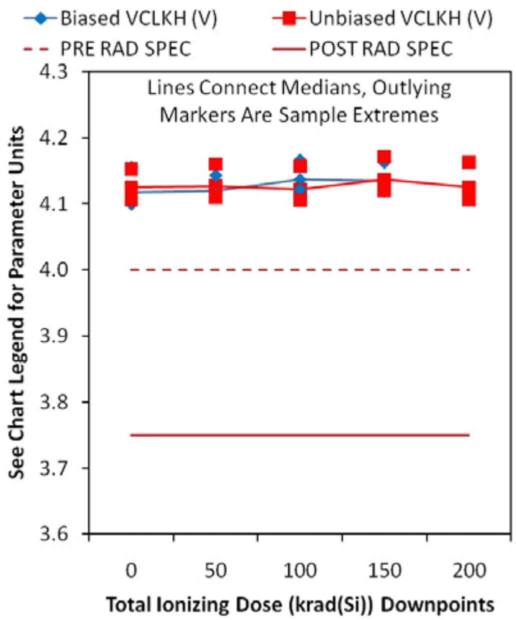



FIGURE 9. CLOCK OUTPUT HIGH VOLTAGE, $V_{CLKH}$

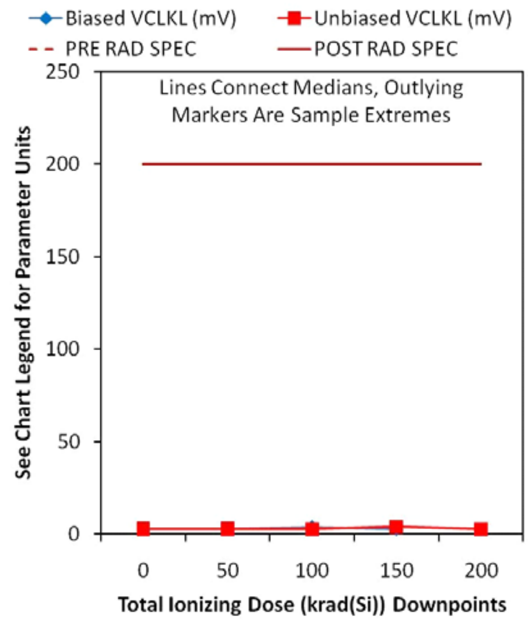



FIGURE 10. CLOCK LOW OUTPUT VOLTAGE, $V_{CLKL}$

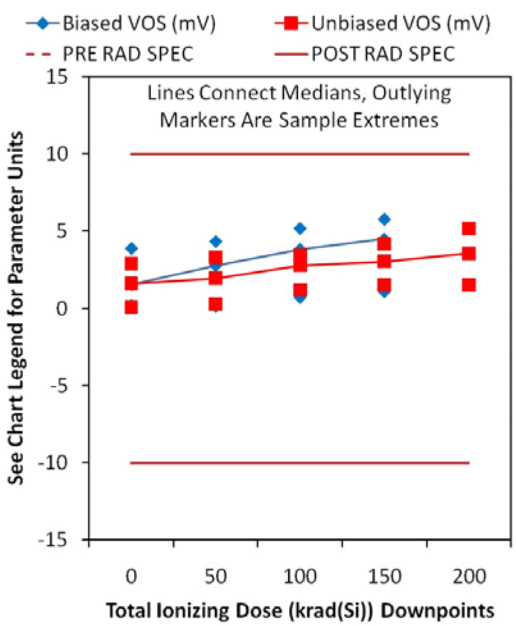



FIGURE 11. ERROR AMPLIFIER OFFSET VOLTAGE, $V_{OS}$

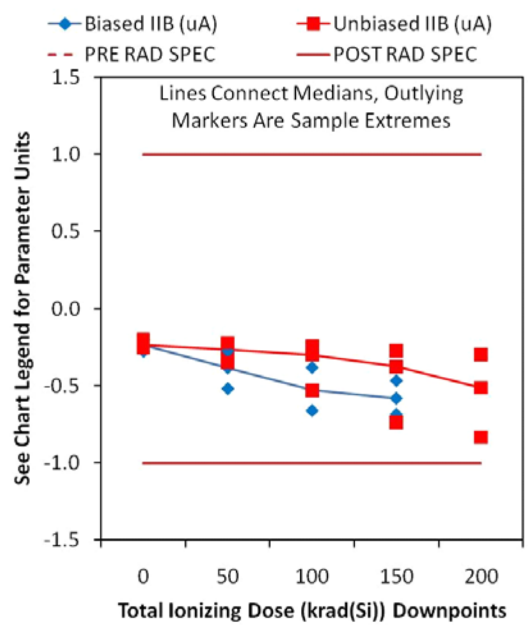



FIGURE 12. ERROR AMPLIFIER INPUT BIAS CURRENT, $I_{IB}$

## Parameter Results (Continued)

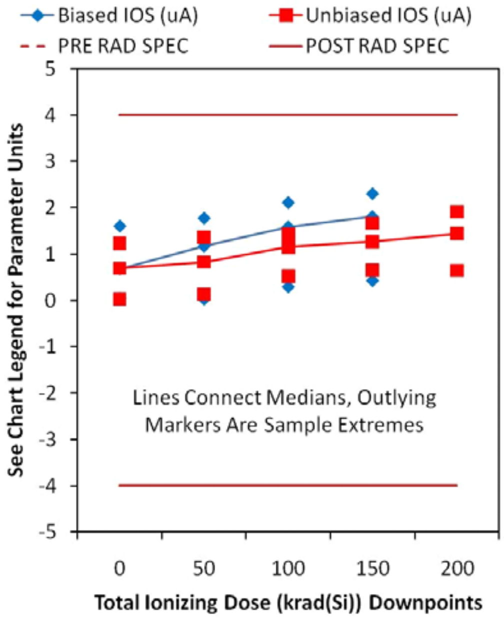



FIGURE 13. ERROR AMPLIFIER INPUT OFFSET CURRENT, $I_{OS}$

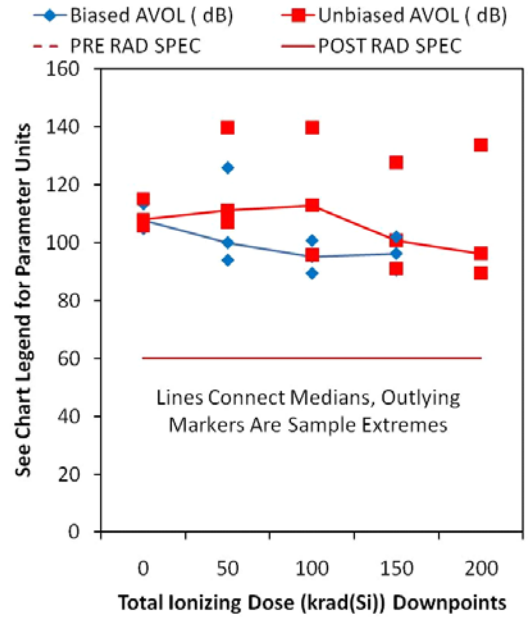



FIGURE 14. ERROR AMPLIFIER OPEN LOOP GAIN, $A_{VOL}$

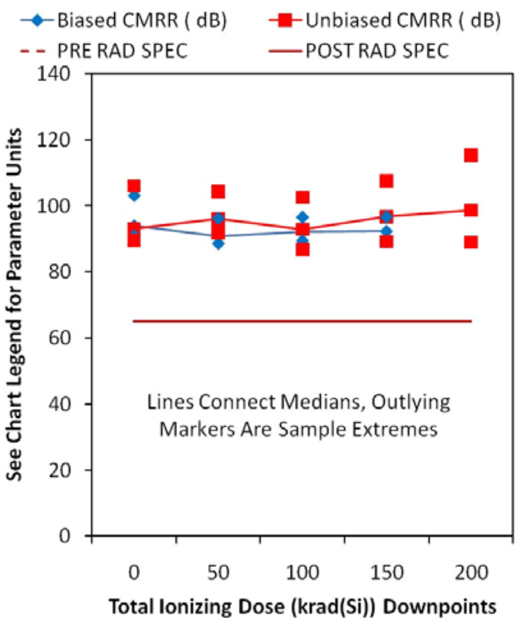



FIGURE 15. ERROR AMPLIFIER COMMON MODE REJECTION RATIO (CMRR)

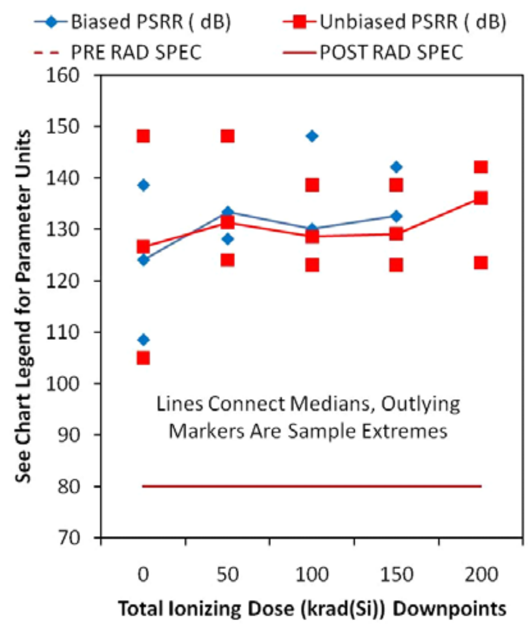



FIGURE 16. ERROR AMPLIFIER POWER SUPPLY REJECTION RATIO (PSRR)

## Parameter Results (Continued)

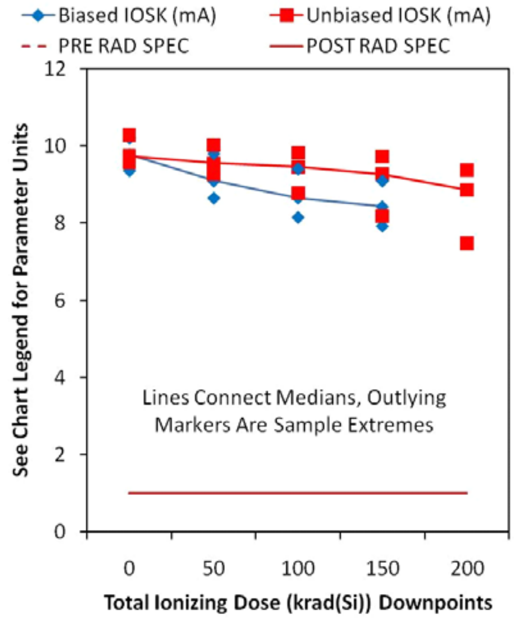



FIGURE 17. ERROR AMPLIFIER OUTPUT SINK CURRENT ($I_{OSK}$)

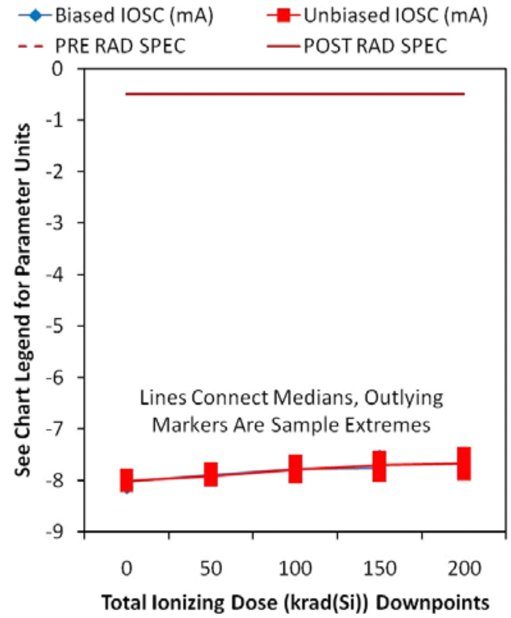



FIGURE 18. ERROR AMPLIFIER OUTPUT SOURCE CURRENT ($I_{OSC}$)

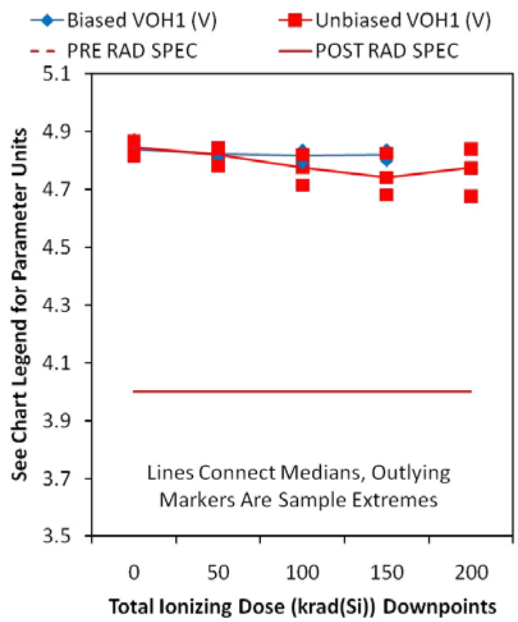



FIGURE 19. ERROR AMPLIFIER OUTPUT HIGH VOLTAGE ($V_{OH1}$)

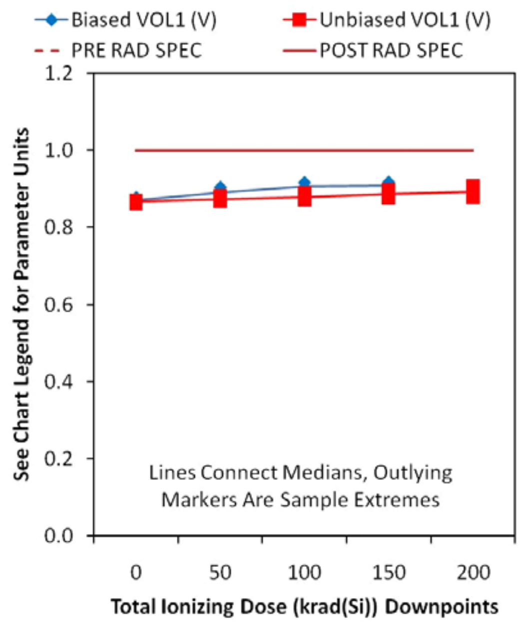



FIGURE 20. ERROR AMPLIFIER OUTPUT LOW VOLTAGE ($V_{OL1}$)

## Parameter Results (Continued)

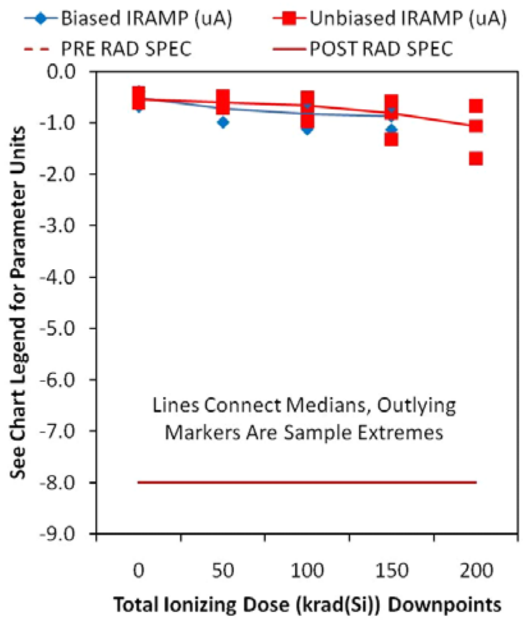



FIGURE 21. PWM RAMP BIAS CURRENT ($I_{RAMP}$)

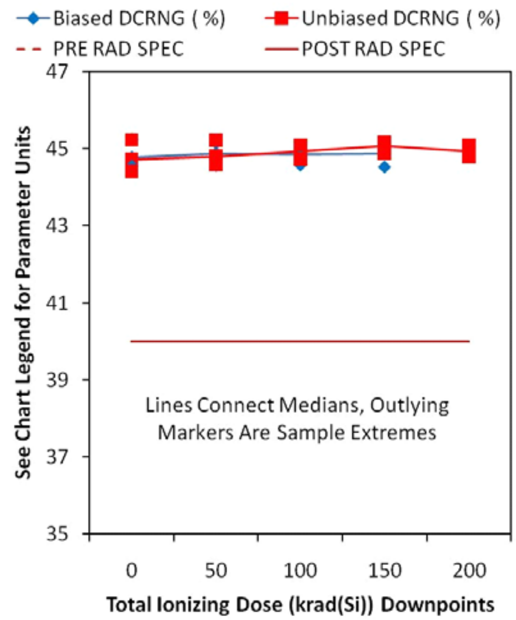



FIGURE 22. PWM DUTY CYCLE RANGE ($D_{CRNG}$) FOR OUTPUT A

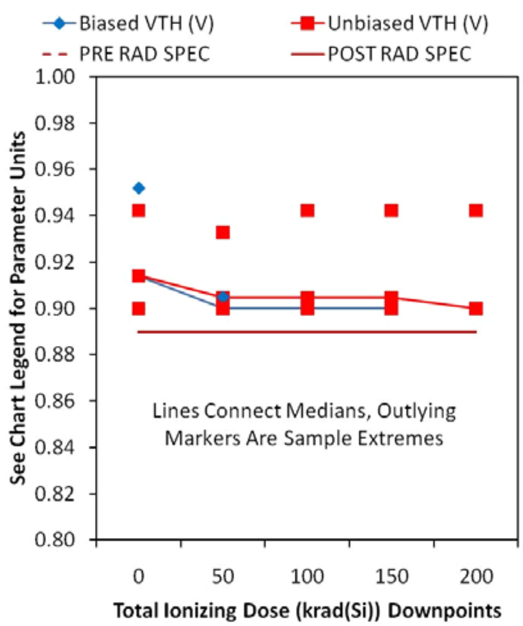



FIGURE 23. PWM ERROR AMPLIFIER OUTPUT ZERO THRESHOLD VOLTAGE ($V_{TH}$)

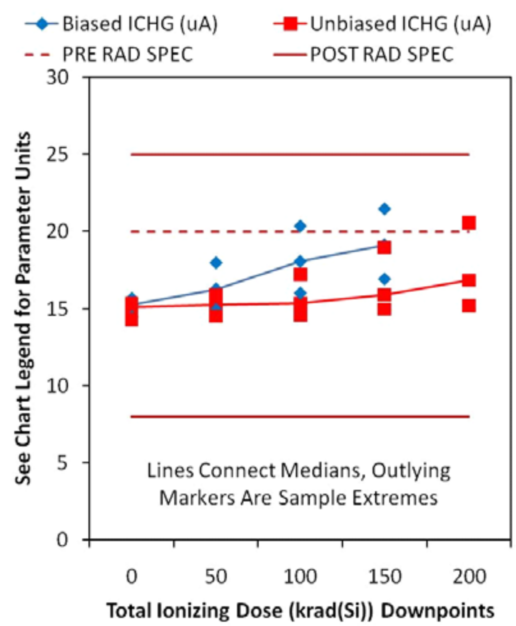



FIGURE 24. SOFT START CHARGING CURRENT ($I_{CHG}$)

## Parameter Results (Continued)

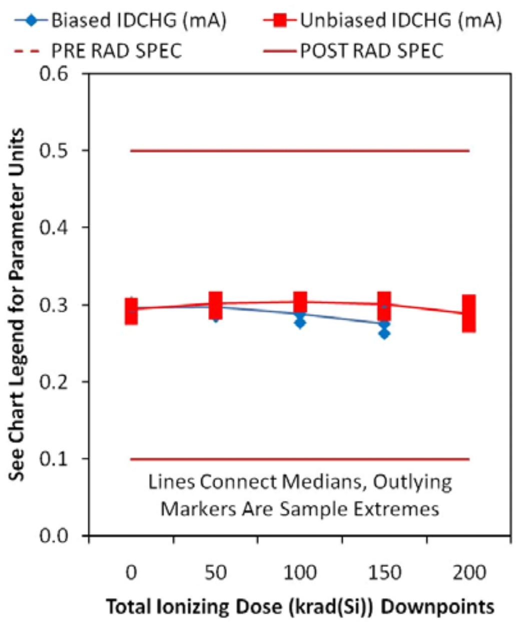



FIGURE 25. SOFT-START DISCHARGING CURRENT ($I_{DCHG}$)

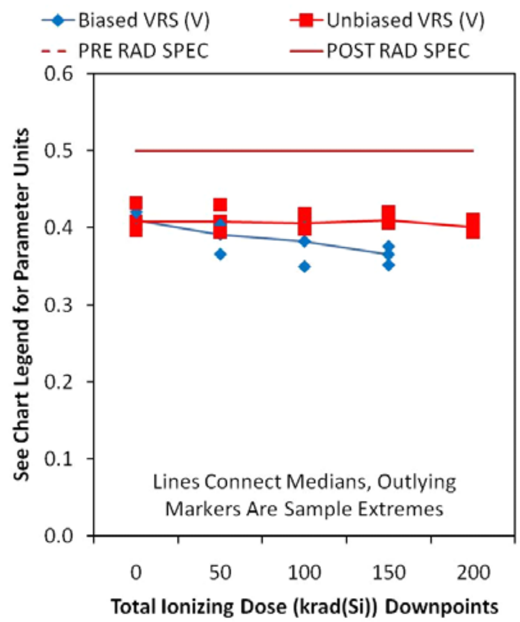



FIGURE 26. OVERCURRENT RESTART THRESHOLD VOLTAGE ($V_{RS}$)

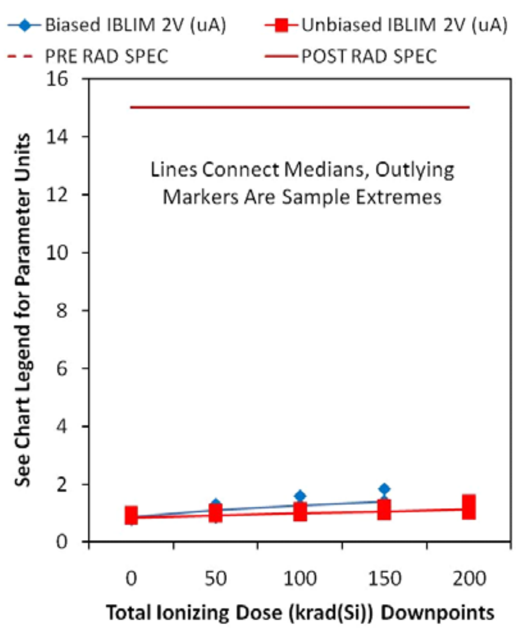



FIGURE 27. CURRENT LIMIT BIAS CURRENT AT 2V ($I_{BLIM}$)

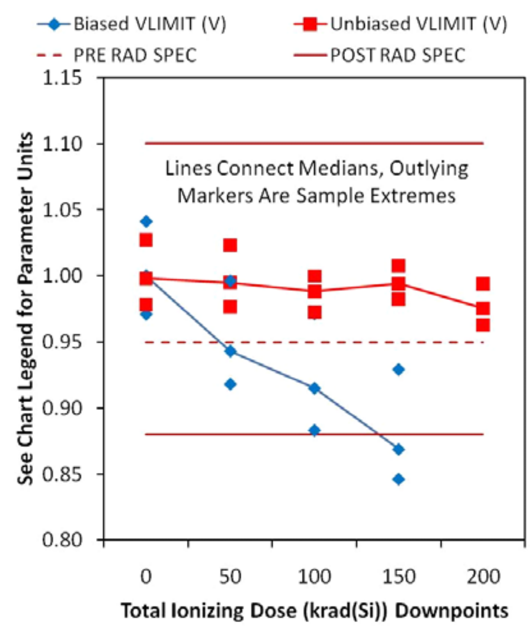



FIGURE 28. CURRENT LIMIT THRESHOLD VOLTAGE ($V_{LIMIT}$)

## Parameter Results (Continued)

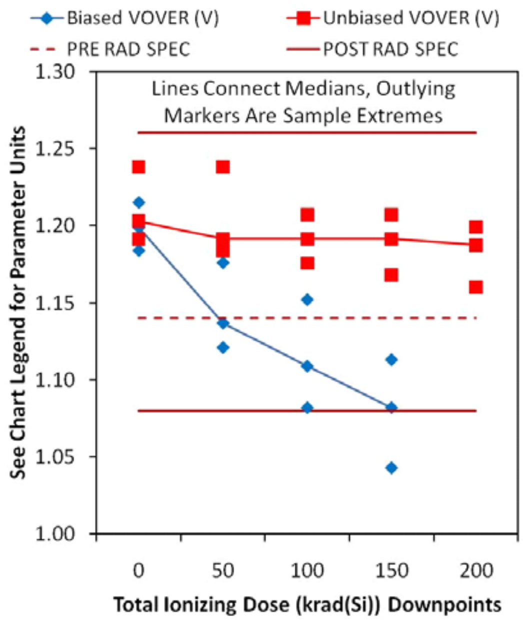



FIGURE 29. OVERCURRENT THRESHOLD VOLTAGE ($V_{OVER}$)

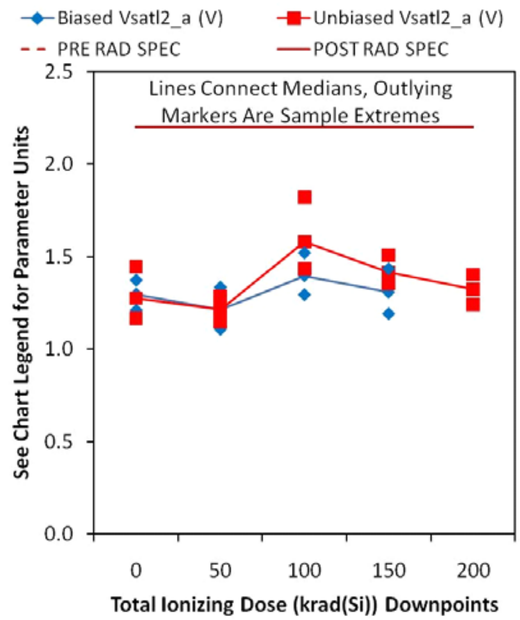



FIGURE 30. OUTPUT A LOW SATURATION VOLTAGE AT $I_{OUT}$ = 200mA ($V_{SATL2}$)

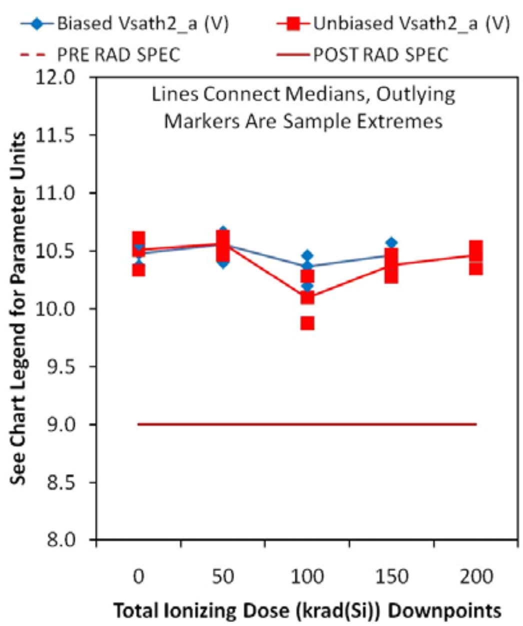



FIGURE 31. OUTPUT A HIGH SATURATION VOLTAGE AT $I_{OUT}$ = 200mA ($V_{SATH2}$)

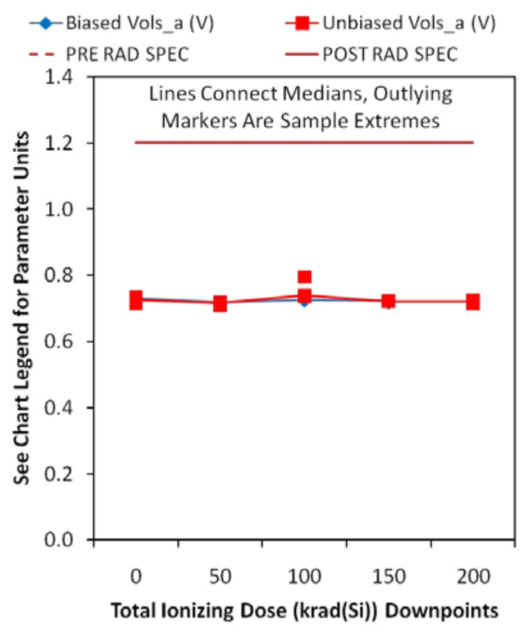



FIGURE 32. UNDERVOLTAGE LOCK-OUT (UVLO) OUTPUT SATURATION VOLTAGE ($V_{OLS}$)

# Parameter Results (Continued)

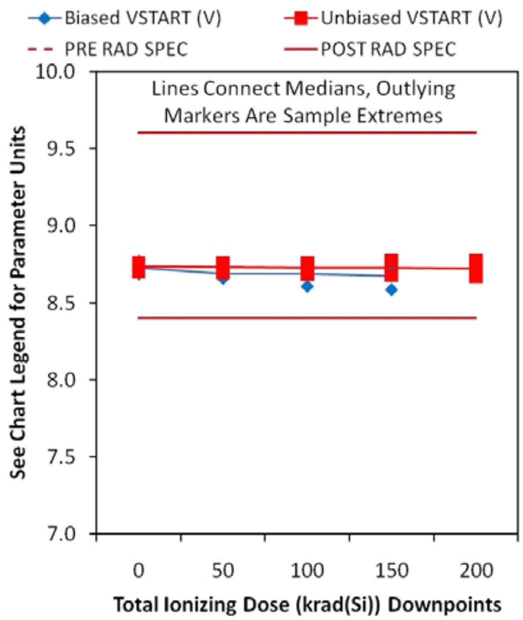



FIGURE 33. UNDERVOLTAGE LOCK-OUT START THRESHOLD ($V_{START}$)

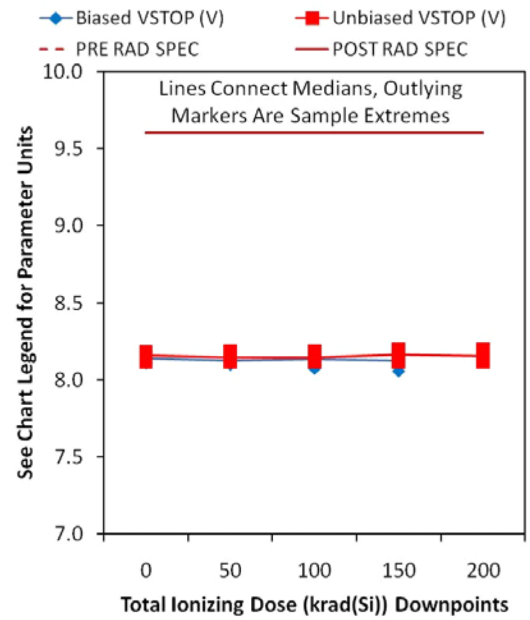



FIGURE 34. UNDERVOLTAGE LOCK-OUT STOP THRESHOLD ($V_{STOP}$)

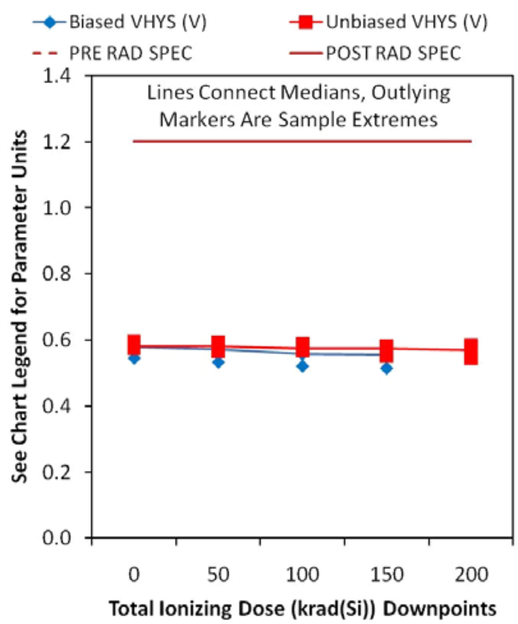



FIGURE 35. UNDERVOLTAGE LOCK-OUT HYSTERESIS VOLTAGE ($V_{HYS}$)

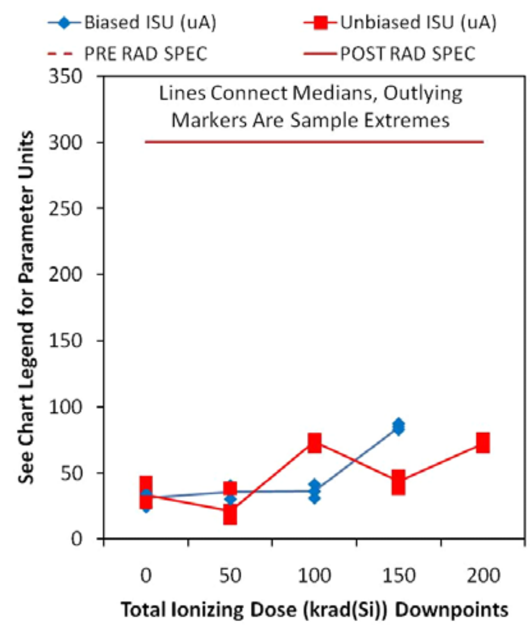



FIGURE 36. START-UP SUPPLY CURRENT ($I_{SU}$)

## Parameter Results (Continued)

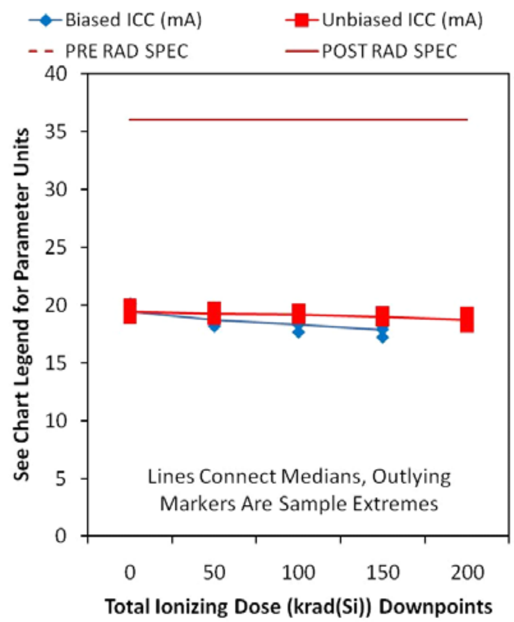



FIGURE 37. OPERATING SUPPLY CURRENT ($I_{CC}$)

## Discussion and Conclusion

The low dose rate downpoints of the HS-1825AEH were tested to the SMD post-irradiation limits. All parameters passed the post radiation limits at the 50krad(Si) low dose rate assurance level. The current limit ($V_{LIMIT}$) and overcurrent ($V_{OVER}$) threshold voltages (Figures 28 and 29), dropped just below the post radiation specifications at 150krad(Si) for the biased condition. The unbiased case for these parameters showed little movement through the 200krad(Si) dose point.

The data clearly indicates that the part is capable of maintaining specified operation up to the 50krad(Si) level of radiation assurance testing for the "EH" version of the part. Further, the data indicates considerable margin with performance being maintained up to 100krad(Si). At 150krad(Si), two parameters for the biased configuration, the current limit threshold ($V_{LIMIT}$) and the overcurrent threshold ($V_{OVER}$) begin to drop just below specification. These two parameters in the biased condition are shown to be the most sensitive to the LDR environment.

**SALES OFFICES** Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

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