Single Event Testing of the IS-2100ARH Half Bridge Driver

Introduction

The intense heavy ion environment encountered in space applications can cause a variety of transient and destructive effects in analog circuits, including single-event latchup (SEL), single-event upset (SEU) and single-event burnout (SEB). These effects can lead to system-level failures including disruption and permanent damage. For predictable, reliable space system operation these components have to be specifically designed and fabricated for SEE hardness, followed by SEE testing to validate the design. This report discusses the results of preliminary SEE testing of the Intersil IS-2100ASRH half bridge driver.

Product Description

The Intersil IS-2100ARH is a hardened equivalent to the industry standard IR2110 and HIP2500 high frequency half bridge drivers. It is a 150V N-channel power MOSFET driver IC. The low side and high side drivers are independently controlled and are matched. A novel level shifting architecture yields the low-power benefits of pulsed operation with the safety of DC operation. The Intersil IS-2100ARH is SEE hardened to an LET of 80MeV/mg/cm^2; this is achieved through use of redundancy/voting logic and/or large devices at the needed circuit nodes. The part is implemented in the Intersil radiation-hardened silicon gate (RSG) process.

SEE Test Objectives

The objectives of SEE testing of the IS-2100ARH were to evaluate the single-event latchup performance of the part and to determine its single-event upset vulnerability. In particular, we were interested in validating the elimination of SEE-caused low-to-high (LH) transitions, which can have a destructive effect on the power MOSFET devices driven by the IS-2100ARH in DC-DC converter applications.

SEE Test Procedure

Samples of the IS-2100ARH were tested for single-event effects at the Cyclotron Institute at Texas A&M University using Au ions (LET= 83.9MeV/mg/cm^2).

At the TAMU facility, all SEE testing is performed outside the chamber. The device under test was mounted in the beam line and irradiated with heavy ions of the appropriate species. The samples were assembled into dual in-line packages with the metal lids removed for beam exposure. The beam was directed on to the exposed die and the beam flux, beam fluence and device output errors were measured.

The tests were controlled remotely from the control room. All input power was supplied from portable supplies connected to the DUT via a cable. The supply currents were monitored along with the device outputs. All currents were measured with digital meters while all the output waveforms were displayed on a digital oscilloscope for ease of identifying different types of SEE effects displayed by the part. Events were captured by triggering on changes in the output pulses.

Single Event Latchup and Burnout Testing Results

The IS-2100ARH is built in the Intersil RSG process, and the dielectrically isolated material used for this process eliminates all latchup mechanisms. As expected, no burnout or latchup was observed using Au ions (LET = 90.9 MeV/mg/cm^2) at 60 degree incidence from the perpendicular, equivalent to an effective LET of 181.8 as compared to testing at normal incidence. Testing was performed at the Texas A&M University Cyclotron Institute on three parts at 25^{o}C and 125^{o}C at maximum supply voltage (Vdd=Vcc=20V, VS=150V and VB=170V). All test runs were run to a fluence of 1x10^7/cm^2. Parts were toggled at 1Khz, 50% duty cycle. Idd and Ivb were measured before and after exposure and the results are shown in Table 1. The post exposure Ivb values were taken 1 minute after the beam was shut off. Immediately post exposure the readings were 20-50ua higher at 25^{o}C only; about 10-20krad(Si) of total dose is accumulated, so these are probably total dose effects. This was not seen at 125^{o}C as the total dose damage is probably annealing much fasterat the higher temperature. As can be seen from the table, no destructive effects or latchup were encountered.

Table 1: Supply and bootstrap currents over irradiation, Au at 90.9MeV/mg/cm^2.

		Pre-Exposure		Post-Exposure	
SN	Temp	Idd(ma)	Ivb(ua)	Idd(ma)	Ivb(ua)
1	25^{o}C	2.04	262	2.03	263
2		2.035	262	2.029	276
4		2.042	259	2.028	280
1	125^{o}C	1.80	240	1.81	240
4		1.74	231	1.69	228
5		1.745	233	1.71	231

Single Event Transient and Upset Testing

Low to high (LH) glitches on the output of a half-bridge driver are the key upset issue in the targeted DC-DC converter applications of this part, as such glitches will cause both external power NMOS FETs to be ON simultaneously. The resultant high "shootthrough" current could destroy the devices. On the other hand, HL glitches will momentarily cause both FETs to be OFF, which will not lead to an overstress. Hence, during the design circuitry and die area were not added to prevent HL glitches other than in the Shutdown latches, which are normally controlled through the SD input.

The design objective of no upset or transient glitches from the low side output (LO) or high side output (HO) output logic "0" level was demonstrated using Au at 90.9MeV/mg/cm^2, the same ion species as used for the SEB/Latchup tests. Outputs were monitored with both counters and with a digital sampling oscilloscope set to trigger on low to high (LH) transitions. Test set-ups were verified by single pulsing LIN and HIN to check that the resultant output pulse was caught by both the counters and oscilloscope. Two units were tested at minimum and maximum supply voltage (12-20V) and at 25^{o}C and 125^{o}C. Each test was performed at an ion fluence of 1x10^6/cm^2. VS was offset 20V from ground (any higher voltage would exceed the maximum input voltage for the HO counter). The three units used in SEB/Latchup testing were also monitored for LH transients with the oscilloscope during the SEB/Latchup testing, with VS offset the maximum 150V; no LH transients were found. This monitoring was done by setting the oscilloscope's persistence to infinity so any transient is painted onto the display and stored indefinitely. Figure 1 and 2 show the scope displays after SEB test runs at 25^{o}C and 125^{o}C. Channel 1 is the LIN and HIN input, channel 2 is the LO output and channel 3 is the HO output (which is AC coupled as it is offset 150V above ground). Rail to rail high to low (HL) transients are clearly visible, but no LH transients are observed. The HL transient cross sections are given in Table 2.

An additional SEE issue is the upset of the LIN or HIN input latch; this will force the LO or HO output to go low until the next LH transition on the LIN or HIN input. This would cause the DC-DC converter to miss up to one cycle. The DC-DC converter designer would need to evaluate to what extent performance would be affected. For higher frequency converters, missing one pulse would likely be insignificant. Even so, the IS-2100ASRH latches were designed and proven to be upset free using Au ions at LET of 90 (effective LET of 180 at 60 degree incidence). Again referring to Figure 1 or 2, if a shutdown latch (SD) upset occurred a HL transition not recovering to the high state until the next rising input edge would be observed. Only HL transients are observed; there are no HL transitions latched by a SD latch upset. Additional testing at minimum supplies (SEB/SEL testing was done at maximum supplies) at 25^{o}C also detected no SD latch upsets.

Vdd, VB-VS	Fluence, /cm^2	Output	Transients	Transient cross section, LET=90MeV/mg/cm^2, cm^2
12	4x10^6	LO	568	1.42x10^{-4}
12	4x10^6	HO	920	2.3x10^{-4}
20	4x10^6	LO	1022	2.56x10^{-4}
20	4x10^6	HO	516	1.29x10^{-4}

Table 2: LO and HO SEE cross sections at LET=90MeV/mg/cm^2

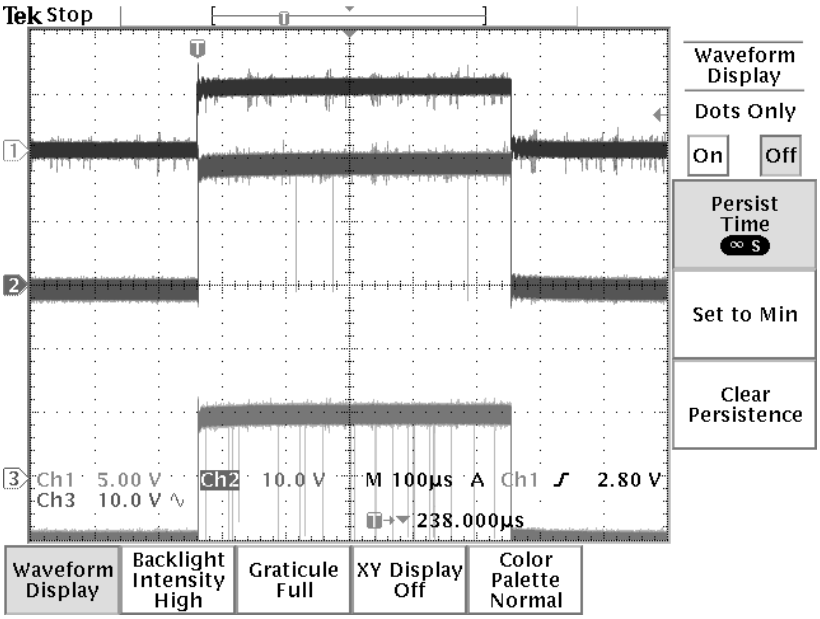

Figure 1: HL transients, Au ions at LET=90MeV/mg/cm^2, 25^{o}C ambient. Note absence of LH transients.

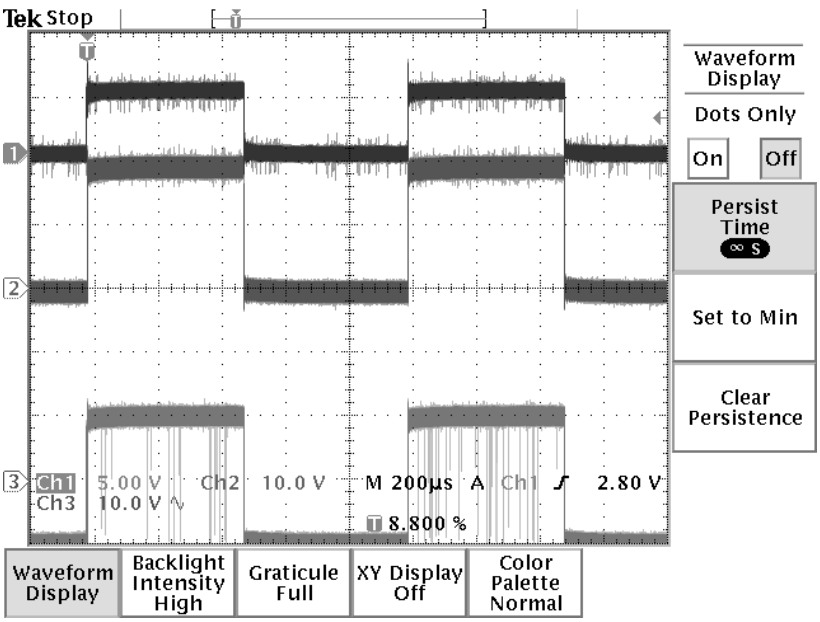

Figure 2: HL transients on HO, Au ions at 90MeV/mg/cm^2, 125^{o}C ambient. Note absence of LH transients.

Conclusion

As expected, the IS-2100ARH showed no latchup or destructive effects up to an LET of 90MeV/mg/cm^2. Additionally, no potentially destructive (at the system level) low to high (LH) transients were encountered at this high LET, validating the SEE hardness of this part.