

IS-1825ASRH, ISL71823xRH

Neutron Testing of the IS-1825ASRH High-Speed Dual Output PWM

Introduction

This report summarizes results of 1MeV equivalent neutron testing of the IS-1825ASRH, the high-speed dual output PWM. The test was conducted to determine the sensitivity of the part to displacement damage (DD) caused by neutron or proton environments. Neutron fluences ranged from $5 \times 10^{11} \text{ n/cm}^2$ to $1 \times 10^{13} \text{ n/cm}^2$.

Product Description

The radiation hardened IS-1825ASRH pulse width modulator is used in high frequency switched-mode power supplies and can be used in either current-mode or voltage-mode. It is well suited for single-ended boost converter applications.

Device features include a precision voltage reference, low power start-up circuit, high frequency oscillator, wide-band error amplifier, and fast current-limit comparator. The use of proprietary process capabilities and unique design techniques results in fast propagation delay times and high output current over a wide range of output voltages. Constructed using the Renesas Rad Hard Silicon Gate (RSG) Dielectric Isolation BiCMOS process, the IS-1825ASRH has been specifically designed to provide highly reliable performance when exposed to hard radiation environments.

The IS-1825ASRH is available in five versions that differ in their electrical testing, total dose lot acceptance testing, and output operation (1825 is dual alternating and 1823 is in-phase). The IS-1825BSEH is acceptance tested on a wafer-by-wafer basis to 300krad(Si) at high dose rate (50-300rad(Si)/s) and to 50krad(Si) at low dose rate (0.01rad(Si)/s). The IS-1825ASRH and IS-1825BSRH are acceptance tested on a wafer-by-wafer basis to 300krad(Si) at high dose rate (50-300rad(Si)/s) only. The ISL71823ASRH and ISL71823BSRH are acceptance tested on a wafer-by-wafer basis to 300krad(Si) at high dose rate (50-300rad(Si)/s) only.

The devices are offered in a 16 Ld CDIP or a 20 Ld CDFP and are fully specified to across the temperature range of -50°C to +125°C.

A functional block diagram for the IS-1825ASRH is shown in [Figure 1](#).

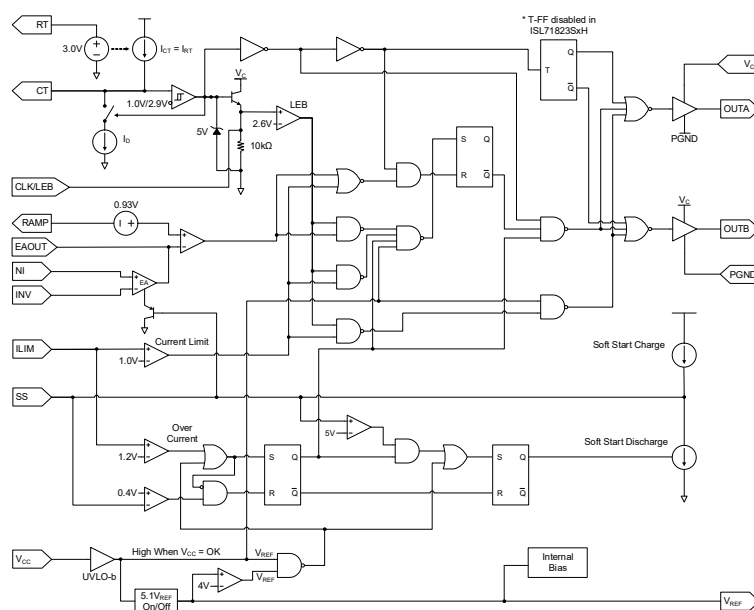


Figure 1. IS-1825ASRH Functional Block Diagram

Contents

1. Test Description 3

1.1 Irradiation Facility 3

1.2 Test Fixturing 3

1.3 Radiation Dosimetry 3

1.4 Characterization Equipment and Procedures 3

1.5 Experimental Matrix 3

2. Results 4

2.1 Attributes Data 4

2.2 Variables Data 4

3. Discussion and Conclusion 29

4. Revision History 29

A. Appendix 30

A.1 Related Information 31

1. Test Description

1.1 Irradiation Facility

Neutron fluence irradiations were performed on the test samples on March 29, 2023, at the University of Massachusetts, Lowell (UMASS Lowell) fast neutron irradiator per Mil-STD-883G, Method 1017.2, with each part unpowered during irradiation. The target irradiation levels were $5 \times 10^{11} \text{n/cm}^2$, $2 \times 10^{12} \text{n/cm}^2$, and $1 \times 10^{13} \text{n/cm}^2$. As neutron irradiation activates many of the heavier elements found in a packaged integrated circuit, the parts exposed at the higher neutron levels required (as expected) some cooldown time before being shipped back to Renesas (Palm Bay, FL) for electrical testing.

1.2 Test Fixturing

No formal irradiation test fixturing is involved, as these DD tests are bag tests in the sense that the parts are irradiated with all leads unbiased.

1.3 Radiation Dosimetry

Table 1 shows dosimetry from UMASS Lowell, indicating the total accumulated gamma dose and actual neutron fluence exposure levels for each set of samples.

Table 1. Neutron Fluence Dosimetry Data

Irradiation	Requested Fluence (n/cm ²)	Reactor Power (kW)	Time (s)	Fluence Rate (n/cm ² -s) ^{[1][2]}	Gamma Dose (rad(Si)) ^[3]	Measured Fluence (n/cm ²) ^[4]
CRF#77981-B	5.00E+11	50	131	3.83E+09	75	5.30E+11
CRF#77981-C	2.00E+12	80	327	6.12E+09	298	2.33E+12
CRF#77981-D	1.00E+13	1000	131	7.65E+10	1492	1.04E+13

1. Dosimetry method: ASTM E-265.
2. The neutron fluence rate is determined from *Initial Testing of the New Ex-Core Fast Neutron Irradiator at UMass Lowell (6/18/02)*. Validated on 6/07/2011 under the Trident II D5LE neutron facility study by Navy Crane.
3. Based on reactor power at 1000kW, the gamma dose is 41krad(Si)/hr $\pm$ 5.3% as mapped by TLD-based dosimetry.
4. Validated by S-32 flux monitors.

1.4 Characterization Equipment and Procedures

Electrical testing was performed before and after irradiation using the Renesas production automated test equipment (ATE). All electrical testing was performed at room temperature.

1.5 Experimental Matrix

Testing proceeded in general accordance with the guidelines of MIL-STD-883 TM 1017. The experimental matrix consisted of six samples irradiated at $5 \times 10^{11} \text{n/cm}^2$, six irradiated at $2 \times 10^{12} \text{n/cm}^2$, and six irradiated at $1 \times 10^{13} \text{n/cm}^2$. Table 2 shows the actual levels achieved, which were $5.30 \times 10^{11} \text{n/cm}^2$, $2.33 \times 10^{12} \text{n/cm}^2$, and $1.04 \times 10^{13} \text{n/cm}^2$. Two control units were used.

The 20 IS-1825ASRH samples were drawn from Lot G5J3W. Samples were packaged in the 20-lead hermetically sealed Ceramic Dual Flat-Pack (CDFP) production package. Samples were processed through burn-in before irradiation and screened to the SMD limits at room, low, and high temperatures before the neutron testing.

2. Results

Neutron testing of the IS-1825ASRH is complete, and the results are reported in the balance of this report. It should be understood when interpreting the data that each neutron irradiation was performed on a different set of samples; this is not total dose testing, where the damage is cumulative.

2.1 Attributes Data

Table 2. Attributes Data

1MeV Fluence, (n/cm ²)		Sample Size	Pass ^[1]	Fail	Notes
Planned	Actual				
5×10 ¹¹	5.30×10 ¹¹	6	6	0	All passed
2×10 ¹²	2.33×10 ¹²	6	6	0	All passed
1×10 ¹³	1.04×10 ¹³	6	6	0	All passed

1. A pass indicates a sample that passes all SMD limits.

2.2 Variables Data

The plots in Figure 2 through Figure 50 show data plots for key parameters before and after irradiation to each level. The plots show the mean of each parameter as a function of neutron irradiation. The plots also include error bars at each down-point, representing the minimum and maximum measured values of the samples. However, in some plots, the error bars might not be visible because of their values compared to the scale of the graph. While the applicable electrical limits taken from the SMD are also shown, it should be noted that these limits are provided for guidance only as the IS-1825ASRH is not specified for the neutron environment.

All samples passed the post-TID irradiation SMD limits after all three exposures up to and including 1.04×10¹³n/cm².

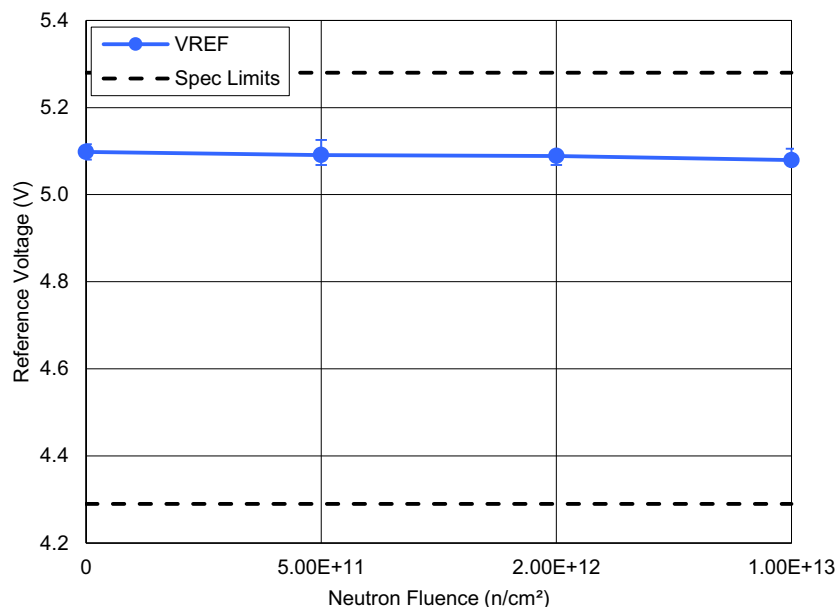


Figure 2. IS-1825ASRH reference output voltage (V_{REF}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 4.29V and a maximum of 5.28V.

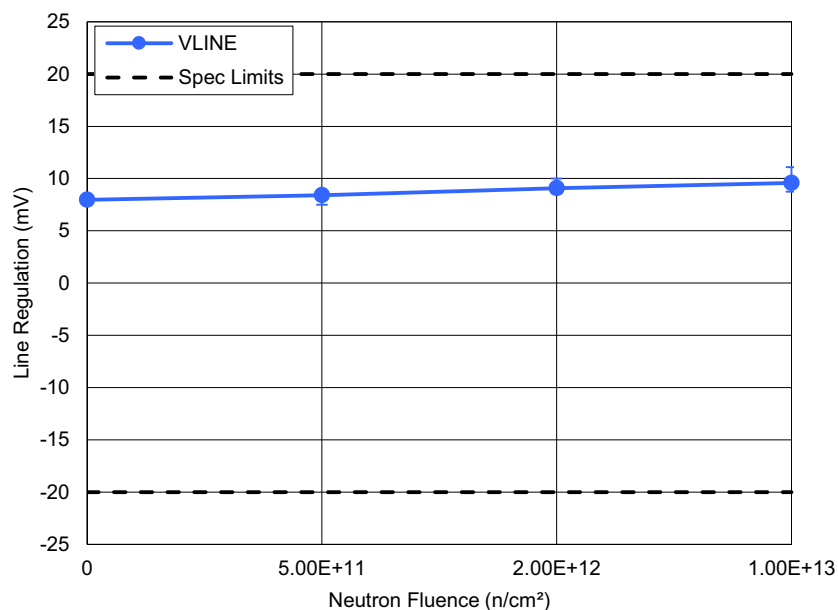


Figure 3. IS-1825ASRH line regulation (V_{LINE}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of -20mV and a maximum of 20mV.

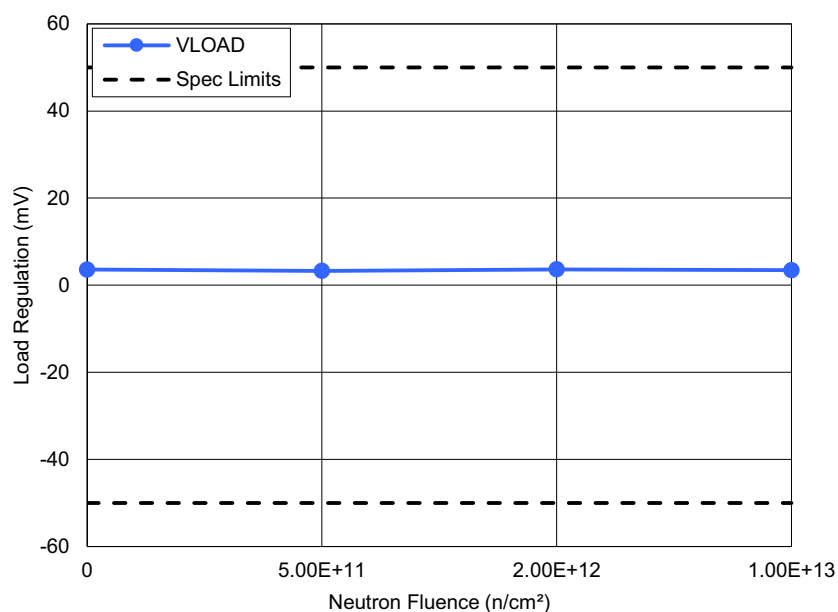


Figure 4. IS-1825ASRH load regulation (V_{LOAD}), 1mA to 10mA load step, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of -50mV and a maximum of 50mV.

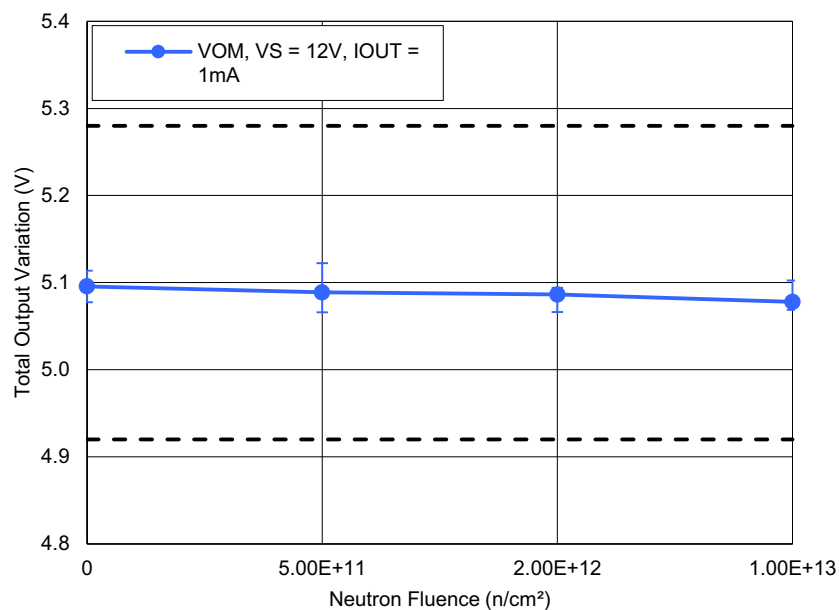


Figure 5. IS-1825ASRH total reference voltage output variation (V_{OM}), 12V supply, 1mA output current, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 4.92V and a maximum of 5.28V.

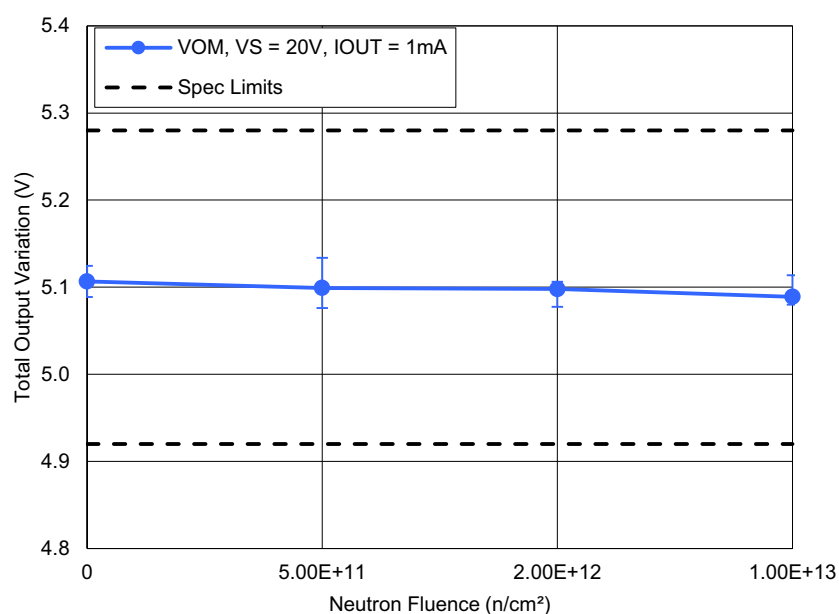


Figure 6. IS-1825ASRH total reference voltage output variation (V_{OM}), 20V supply, 1mA output current, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 4.92V and a maximum of 5.28V.

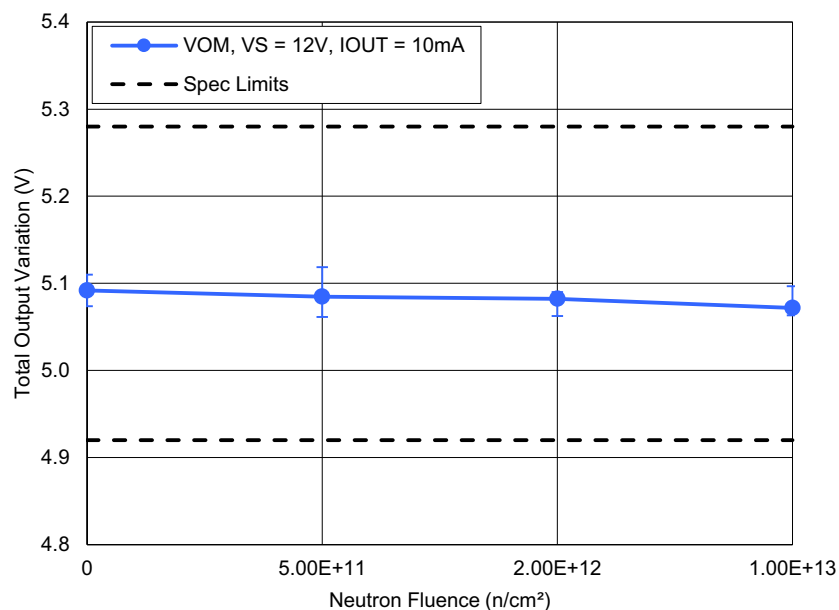


Figure 7. IS-1825ASRH total reference voltage output variation (V_{OM}), 12V supply, 10mA output current, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 4.92V and a maximum of 5.28V.

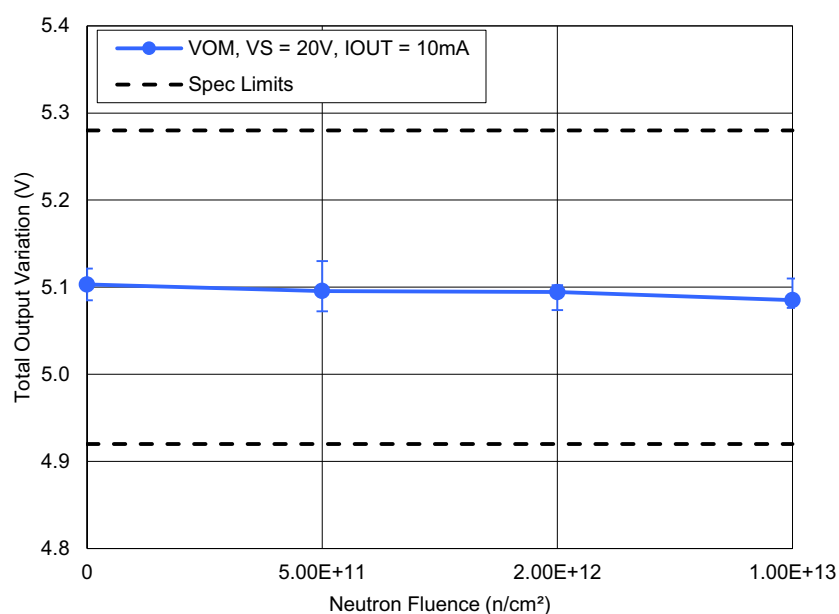


Figure 8. IS-1825ASRH total reference voltage output variation (V_{OM}), 20V supply, 10mA output current, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 4.92V and a maximum of 5.28V.

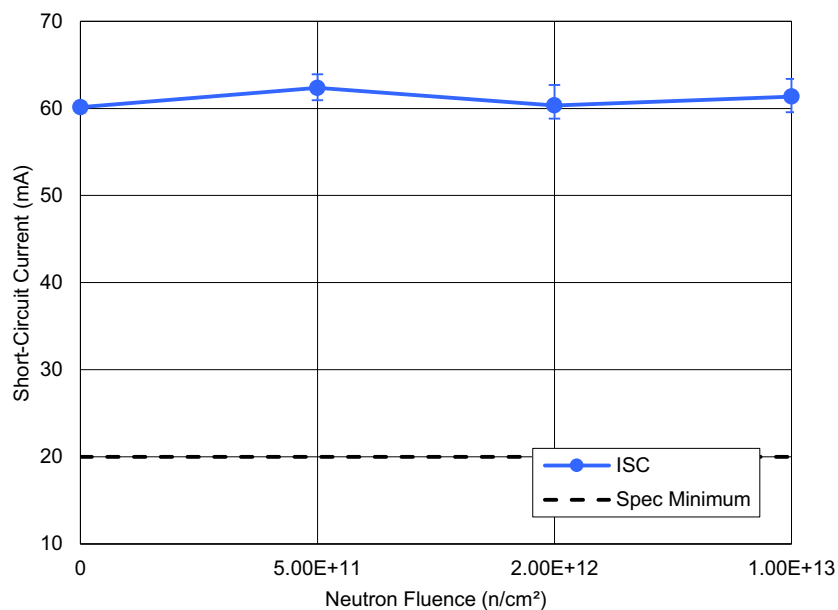


Figure 9. IS-1825ASRH reference short-circuit current (I_{SC}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 20mA.

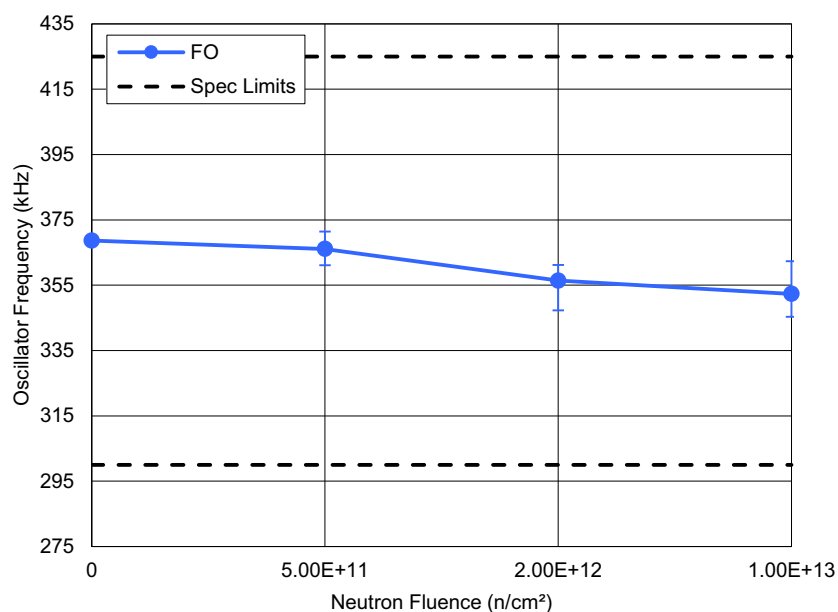


Figure 10. IS-1825ASRH oscillator frequency (F_O) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 300kHz and a maximum of 425kHz.

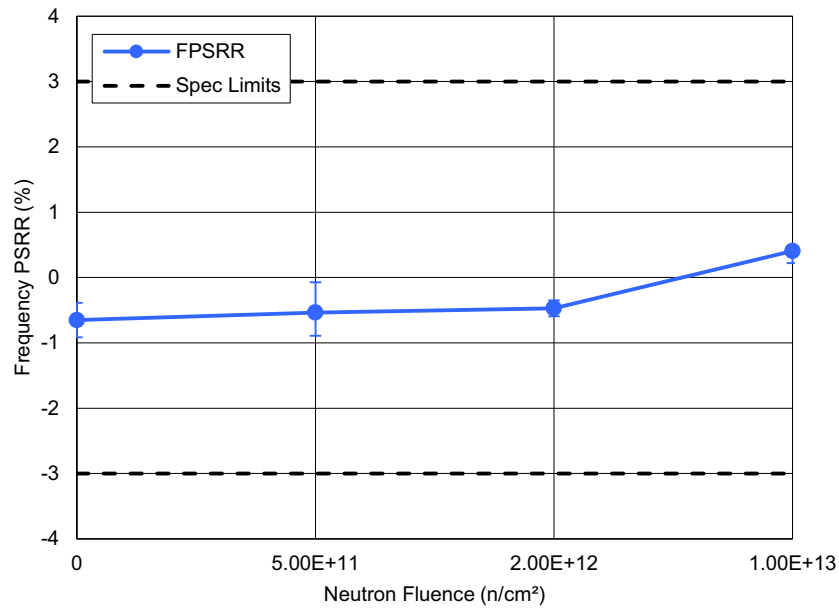


Figure 11. IS-1825ASRH oscillator frequency power supply rejection ratio (F_{PSRR}), 12V to 20V supply, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of -3% and a maximum of 3%.

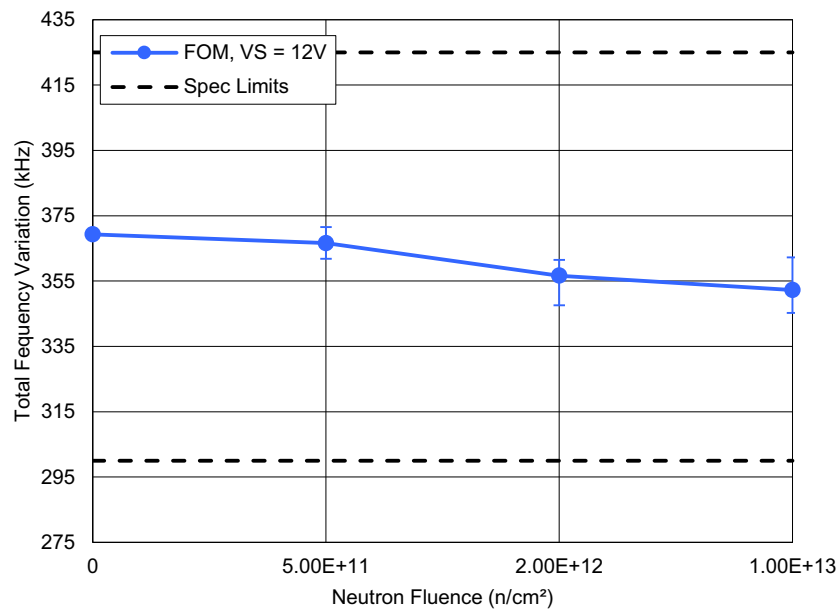


Figure 12. IS-1825ASRH oscillator total frequency variation (F_{OM}), 12V supply, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 300kHz and a maximum of 425kHz.

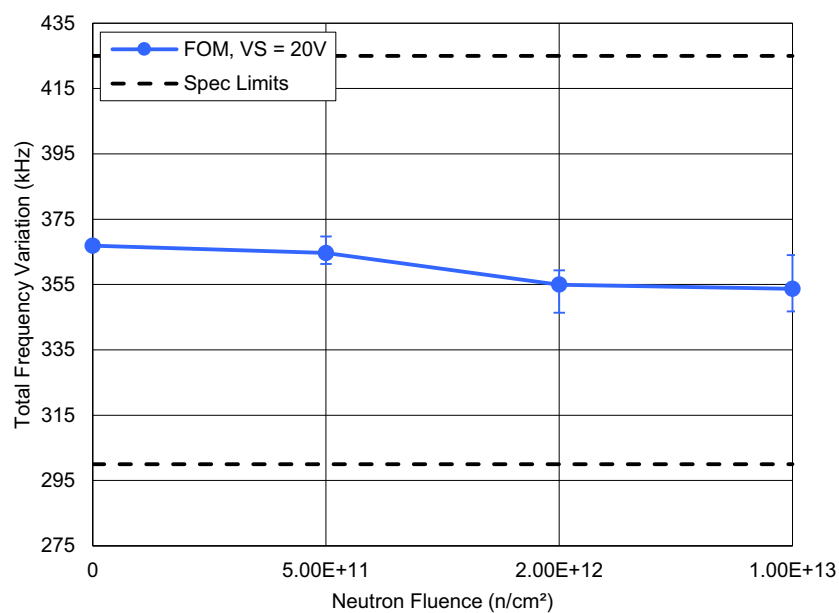


Figure 13. IS-1825ASRH oscillator total frequency variation (F_{OM}), 20V supply, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 300kHz and a maximum of 425kHz.

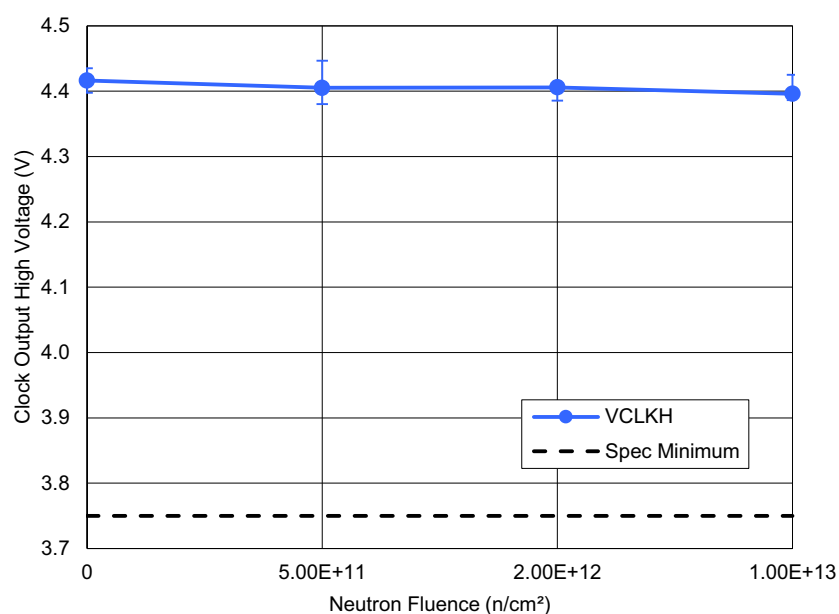


Figure 14. IS-1825ASRH clock output high voltage (V_{CLKH}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 3.75V.

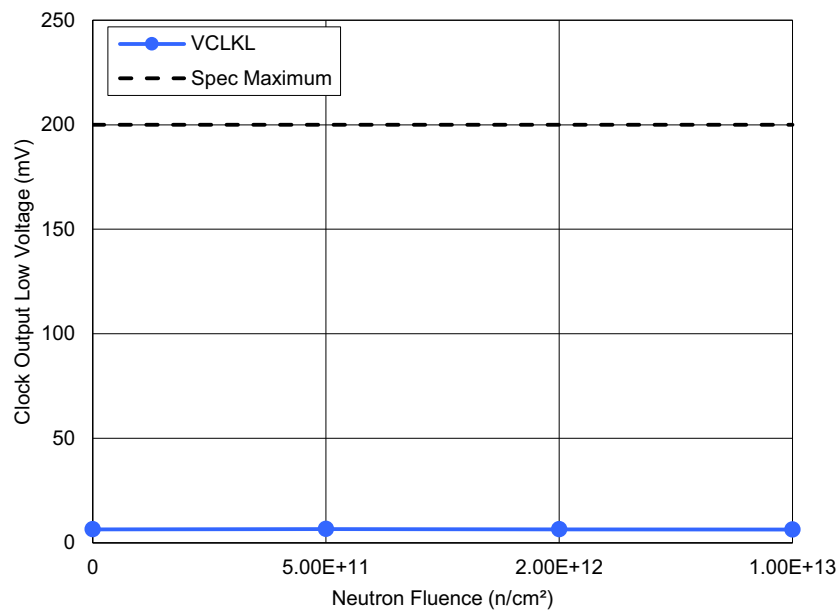


Figure 15. IS-1825ASRH clock output low voltage (V_{CLKL}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 200mV.

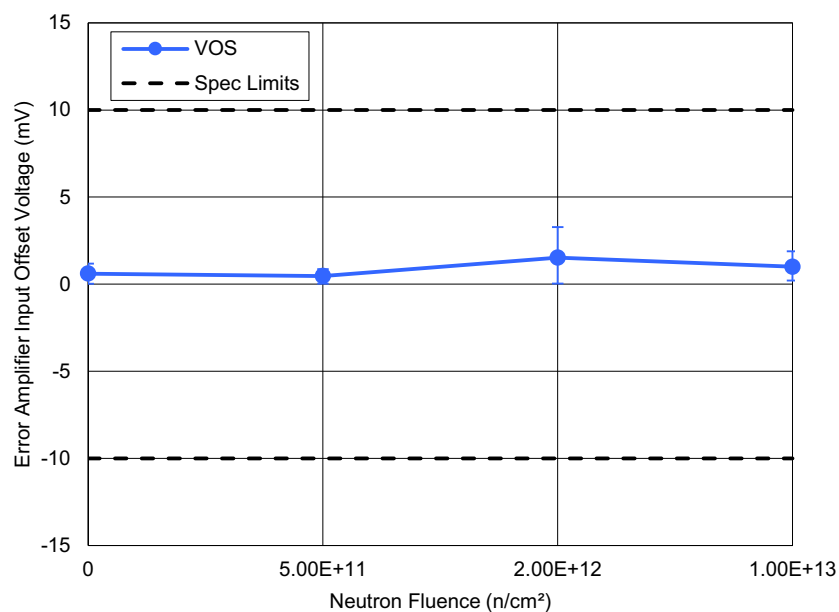


Figure 16. IS-1825ASRH error amplifier input offset voltage (V_{OS}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of -10mV and a maximum of 10mV.

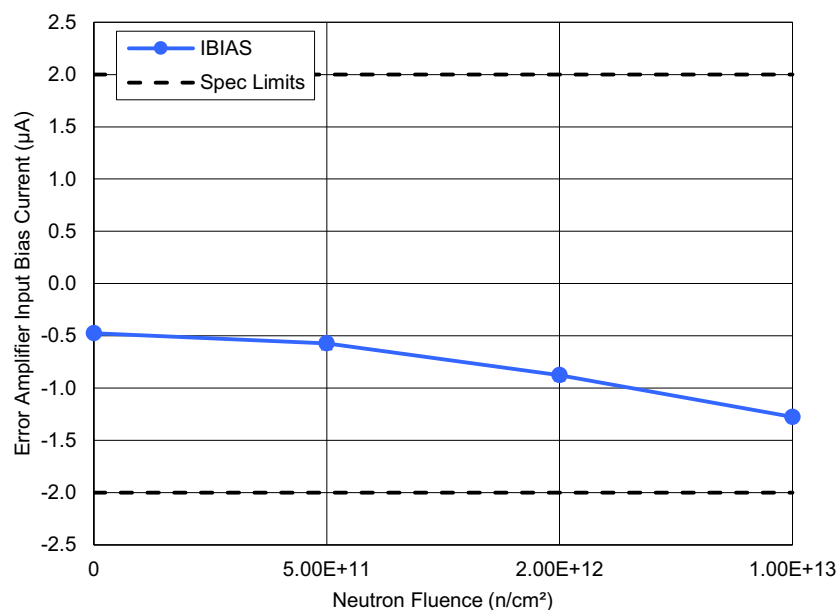


Figure 17. IS-1825ASRH error amplifier input bias current (I_{BIAS}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of $-2\mu A$ and a maximum of $2\mu A$.

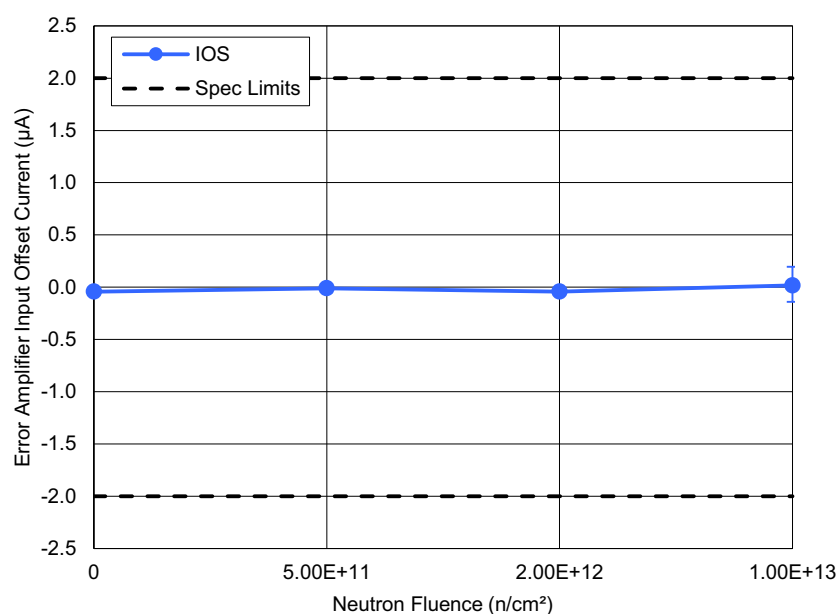


Figure 18. IS-1825ASRH error amplifier input offset current (I_{OS}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of $-2\mu A$ and a maximum of $2\mu A$.

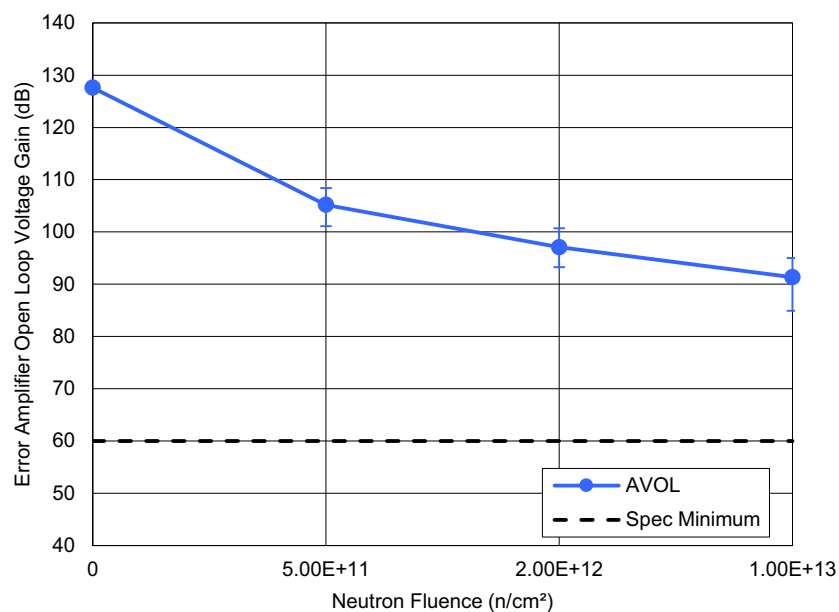


Figure 19. IS-1825ASRH error amplifier open-loop voltage gain (A_{VOL}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 60dB.

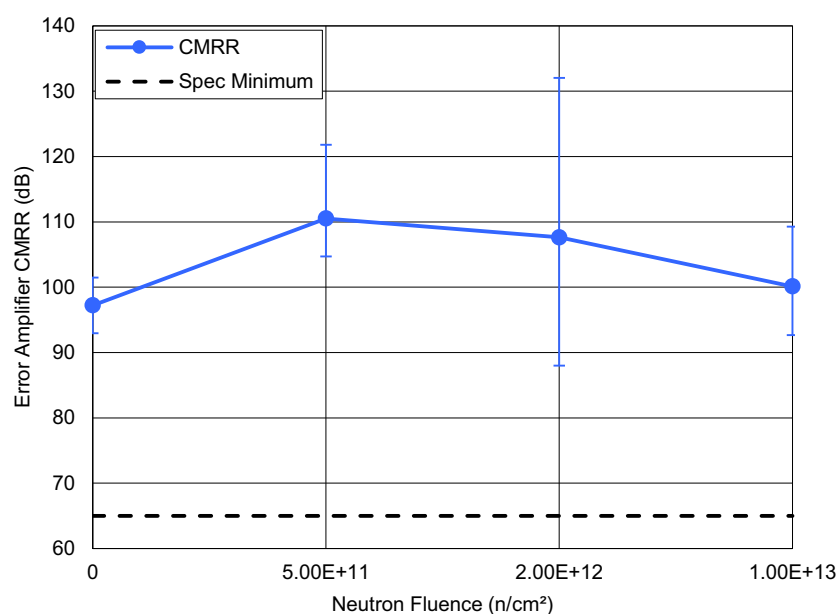


Figure 20. IS-1825ASRH error amplifier common-mode rejection ratio (CMRR) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 65dB.

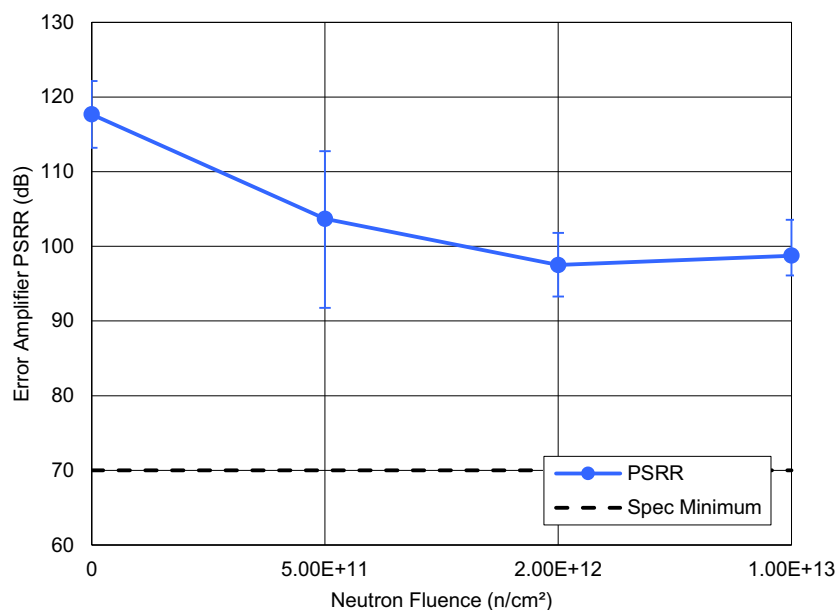


Figure 21. IS-1825ASRH error amplifier power supply rejection ratio (PSRR) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 70dB.

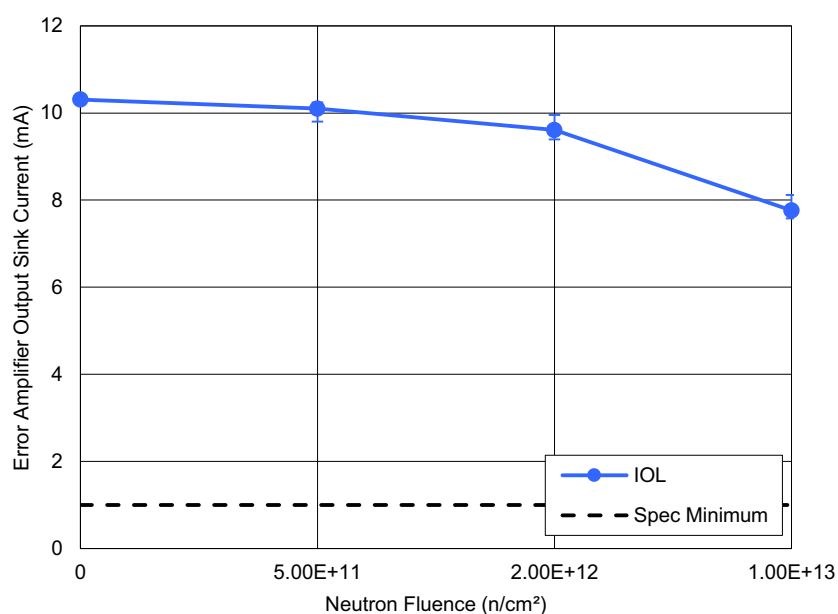


Figure 22. IS-1825ASRH error amplifier output sink current (I_{OL}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 1mA.

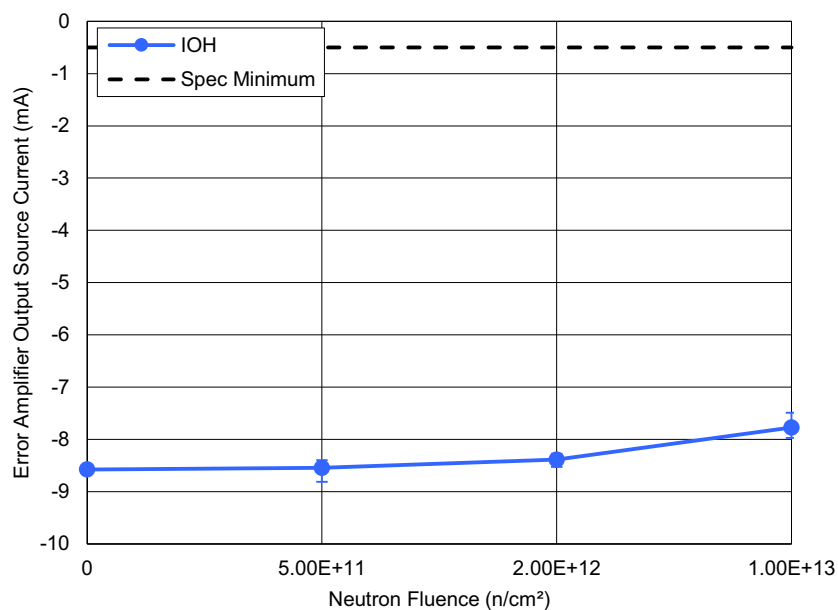


Figure 23. IS-1825ASRH error amplifier output source current (I_{OH}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of -0.5mA.

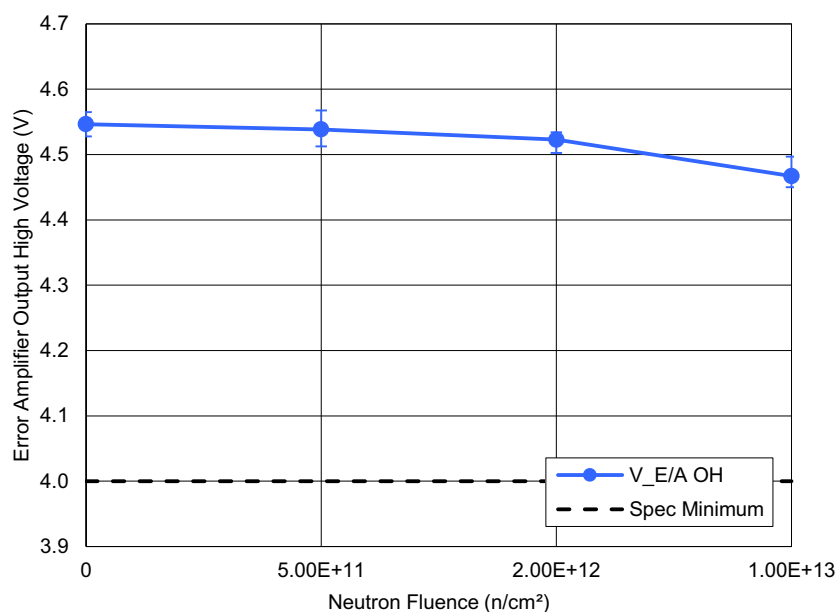


Figure 24. IS-1825ASRH error amplifier output high voltage ($V_{E/A OH}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 4V.

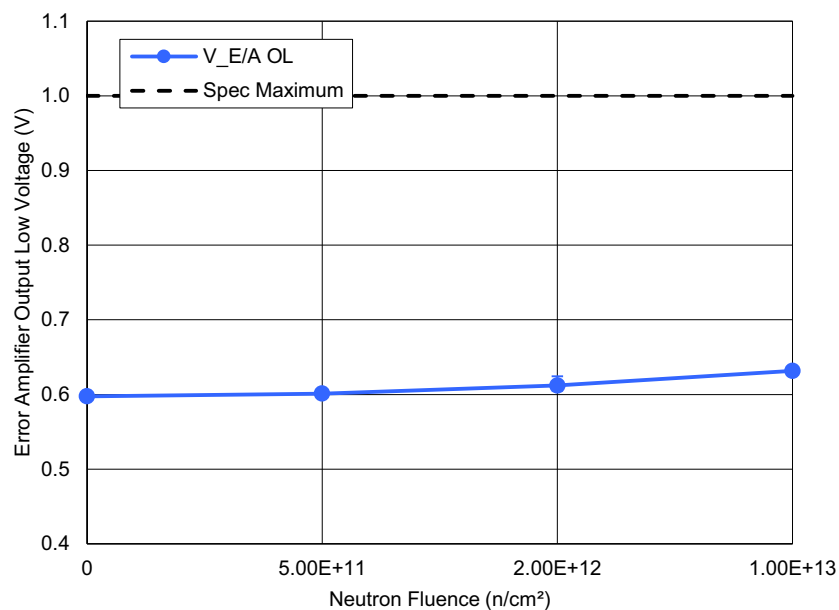


Figure 25. IS-1825ASRH error amplifier output low voltage ($V_{E/A OL}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 1V.

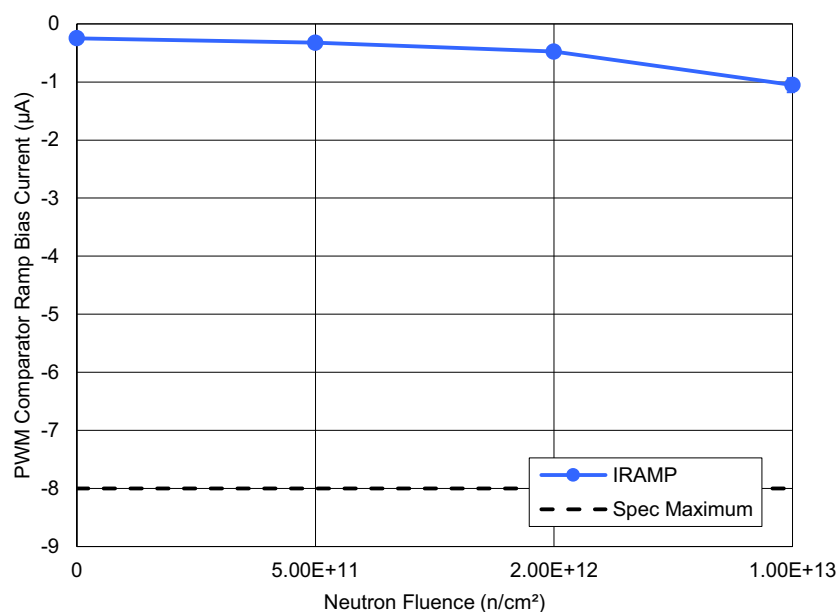


Figure 26. IS-1825ASRH PWM comparator ramp bias current (I_{RAMP}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of -8µA.

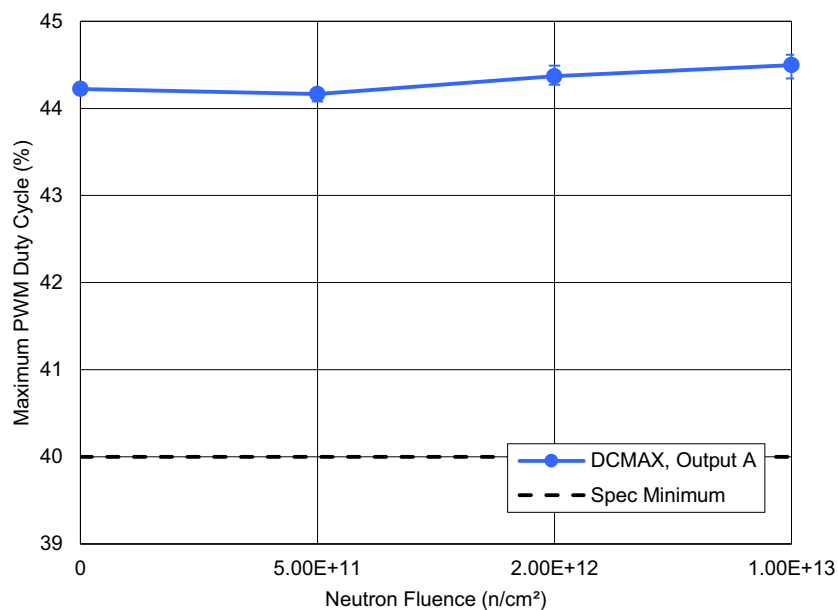


Figure 27. IS-1825ASRH maximum PWM duty cycle (DC_{MAX}), output A, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 40%.

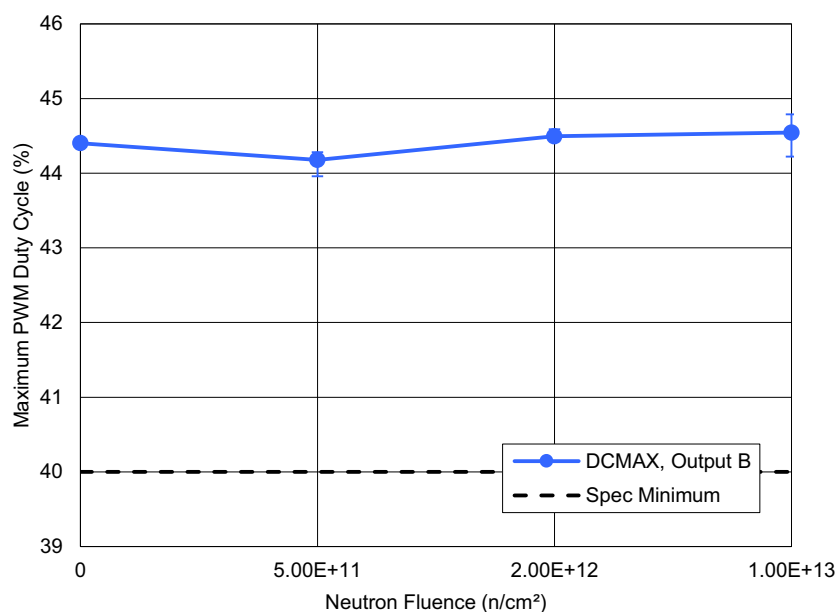


Figure 28. IS-1825ASRH maximum PWM duty cycle (DC_{MAX}), output B, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 40%.

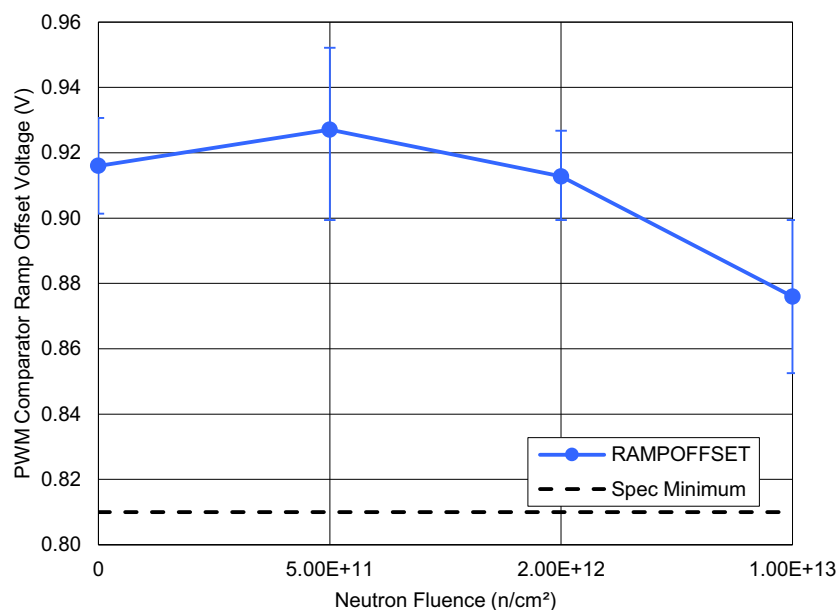


Figure 29. IS-1825ASRH PWM comparator ramp offset voltage ($RAMP_{OFFSET}$) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 0.81V.

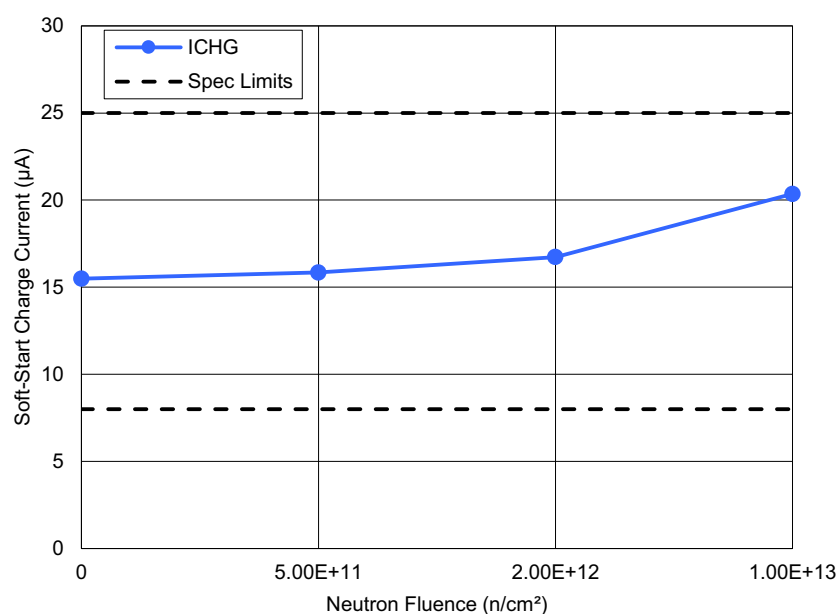


Figure 30. IS-1825ASRH soft-start charge current (I_{CHG}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 8µA and a maximum of 25µA.

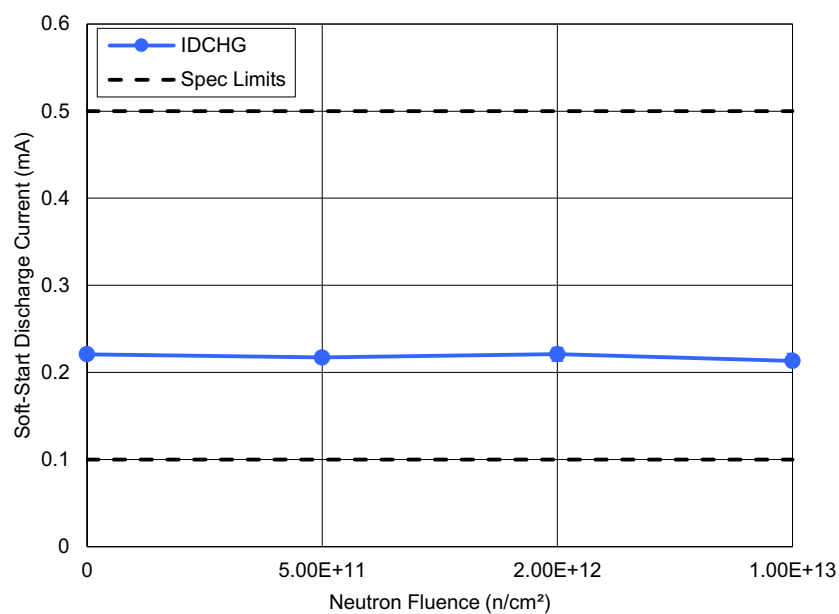


Figure 31. IS-1825ASRH soft-start discharge current (I_{DCHG}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 0.1mA and a maximum of 0.5mA.

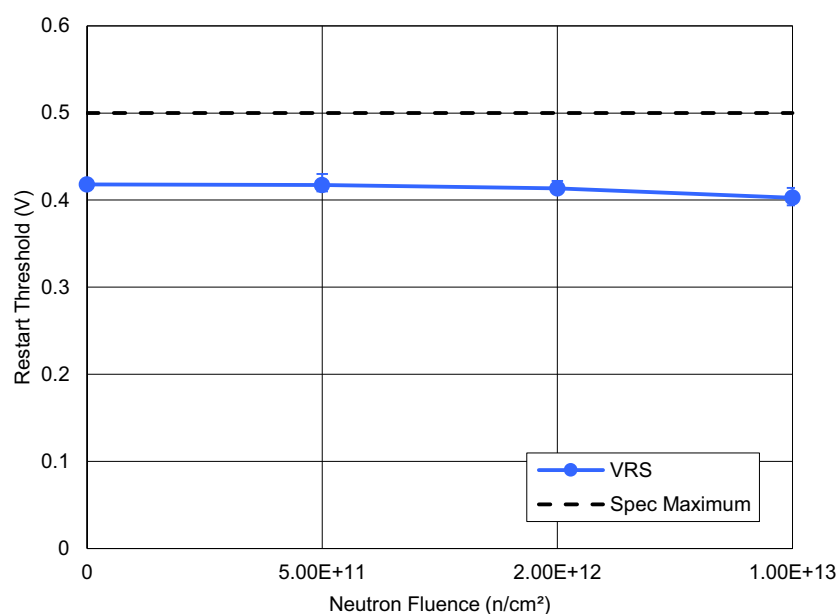


Figure 32. IS-1825ASRH restart threshold (V_{RS}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 0.5V.

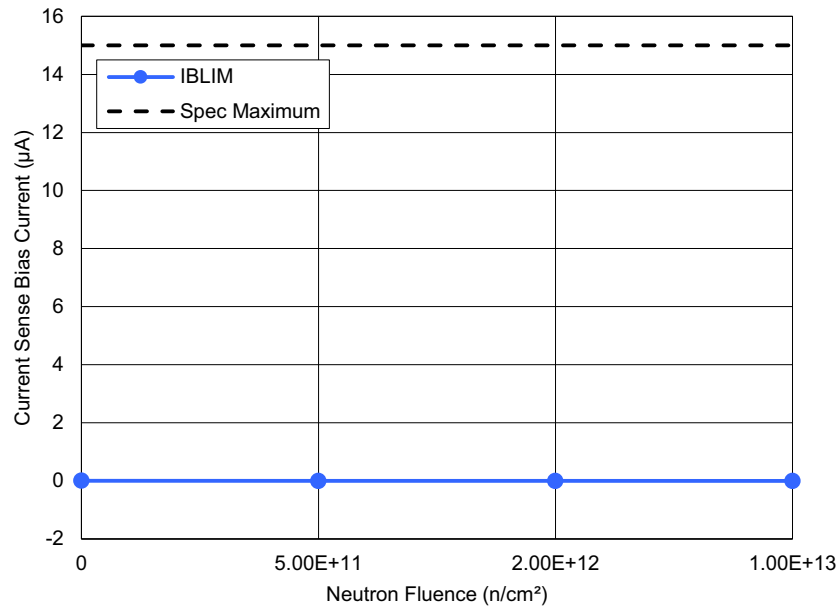


Figure 33. IS-1825ASRH current sense bias current (I_{BLIM}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 15µA.

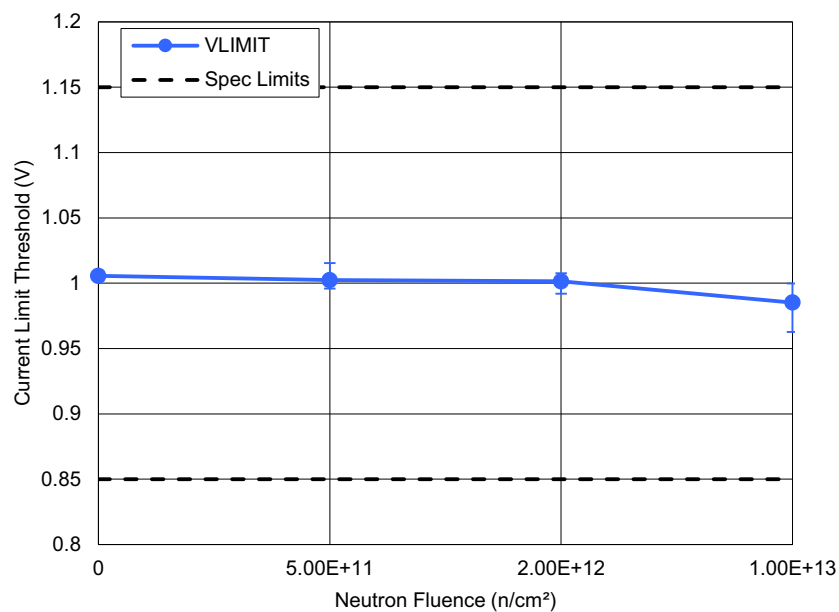


Figure 34. IS-1825ASRH current limit threshold (V_{LIMIT}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 0.85V and a maximum of 1.15V.

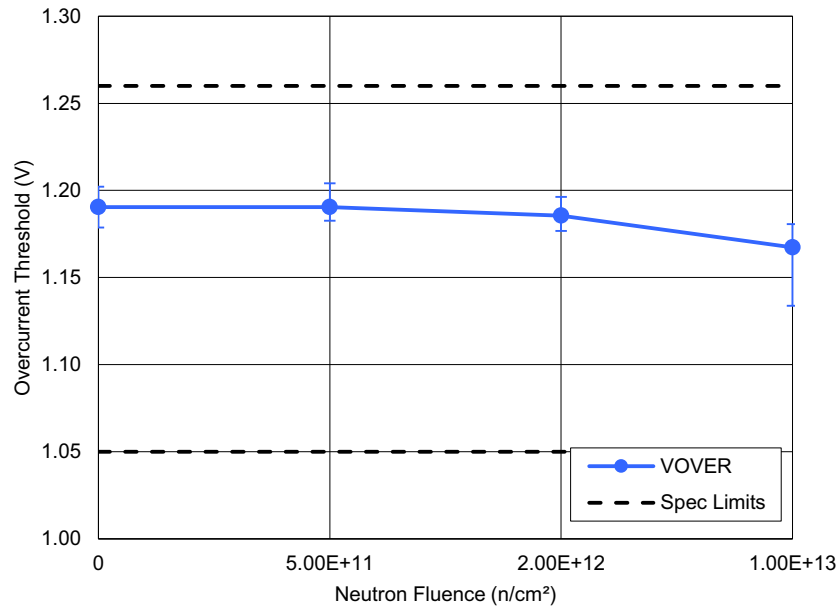


Figure 35. IS-1825ASRH overcurrent threshold (V_{OVER}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 1.05V and a maximum of 1.26V.

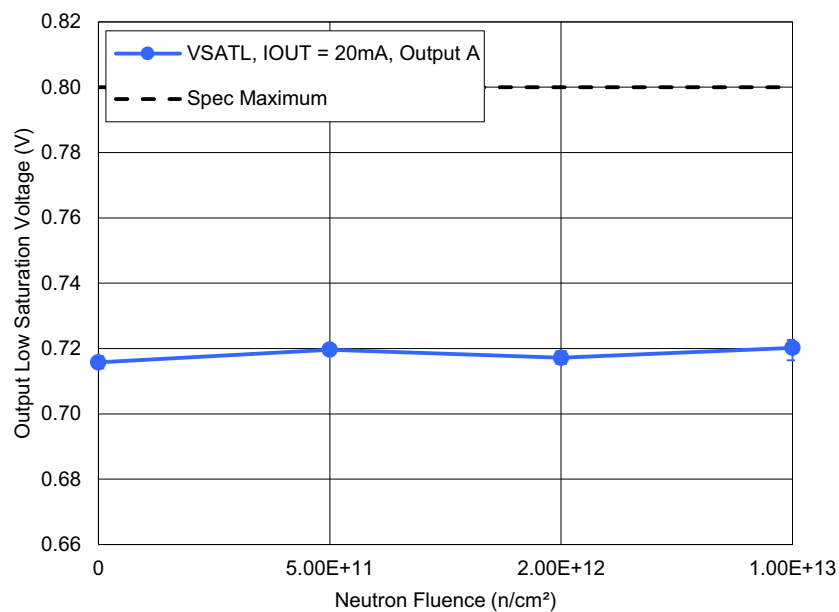


Figure 36. IS-1825ASRH output low saturation voltage (V_{SATL}), A output at 20mA, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 0.8V.

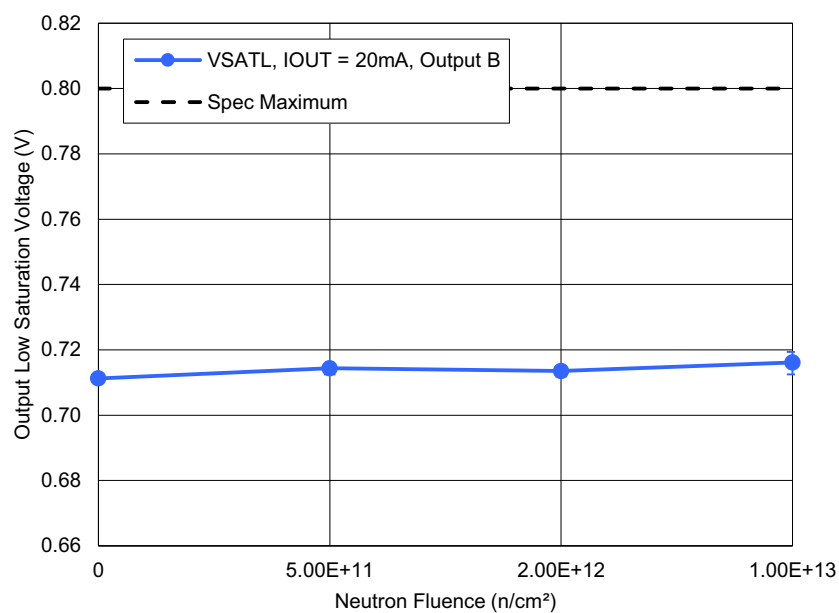


Figure 37. IS-1825ASRH output low saturation voltage (V_{SATL}), B output at 20mA, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 0.8V.

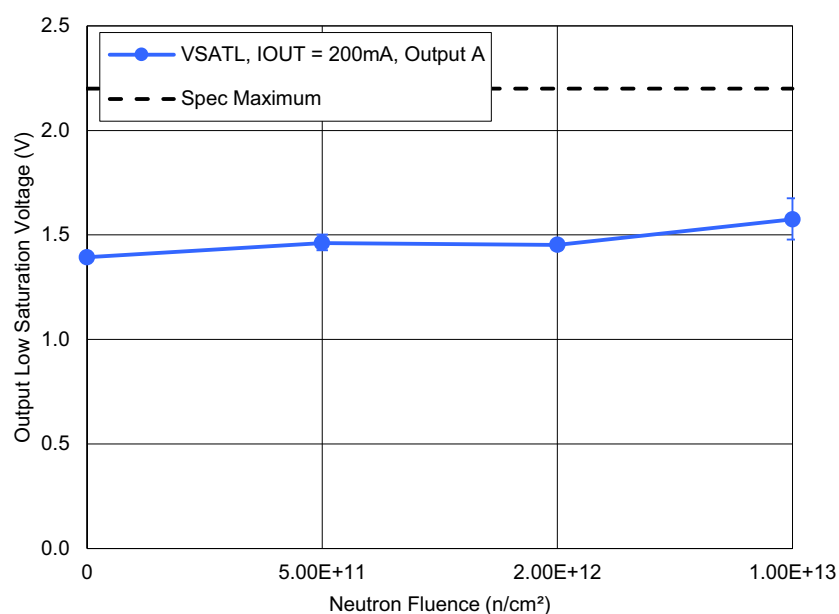


Figure 38. IS-1825ASRH output low saturation voltage (V_{SATL}), A output at 200mA, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 2.2V.

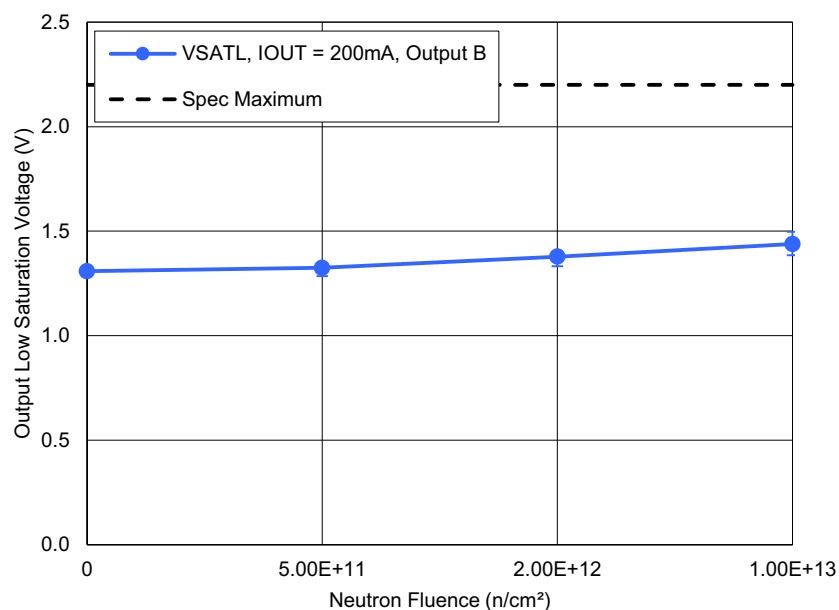


Figure 39. IS-1825ASRH output low saturation voltage (V_{SATL}), B output at 200mA, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 2.2V.

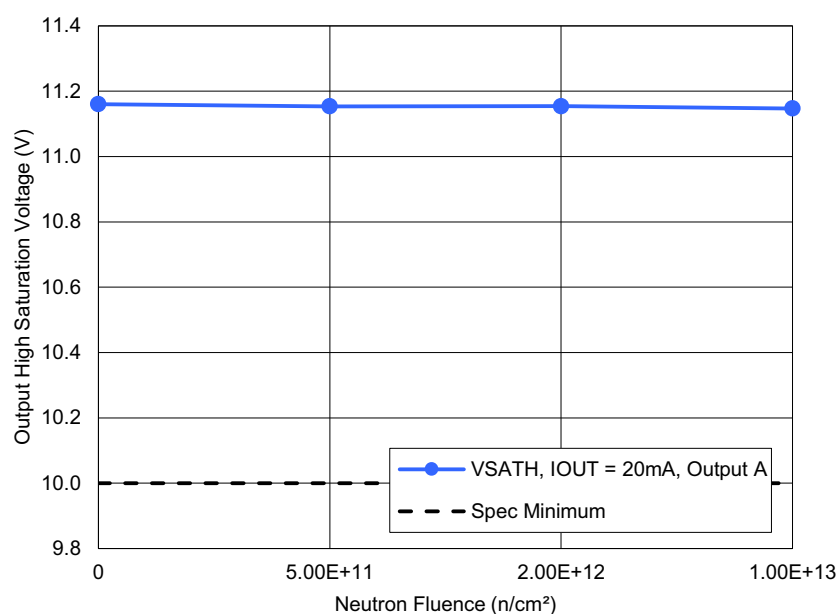


Figure 40. IS-1825ASRH output high saturation voltage (V_{SATH}), A output at 20mA, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 10V.

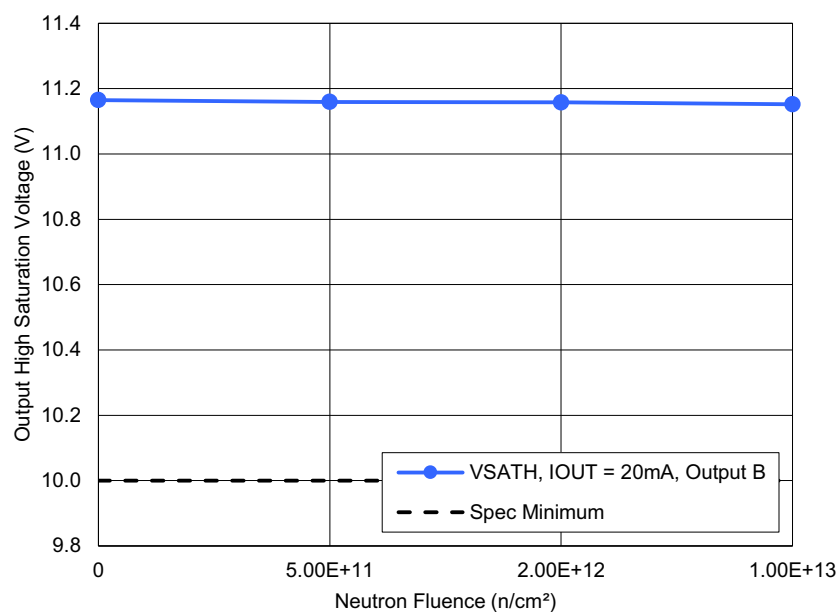


Figure 41. IS-1825ASRH output high saturation voltage (V_{SATH}), B output at 20mA, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 10V.

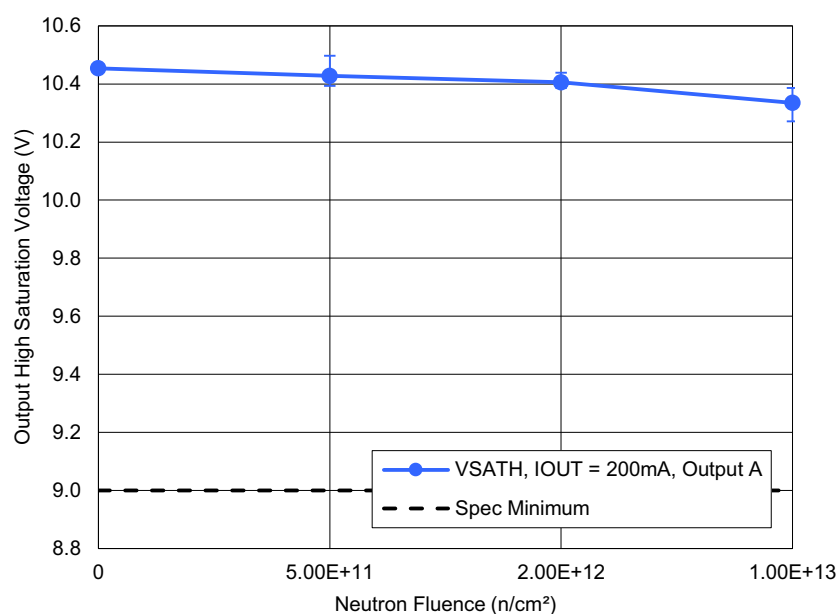


Figure 42. IS-1825ASRH output high saturation voltage (V_{SATH}), A output at 200mA, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 9V.

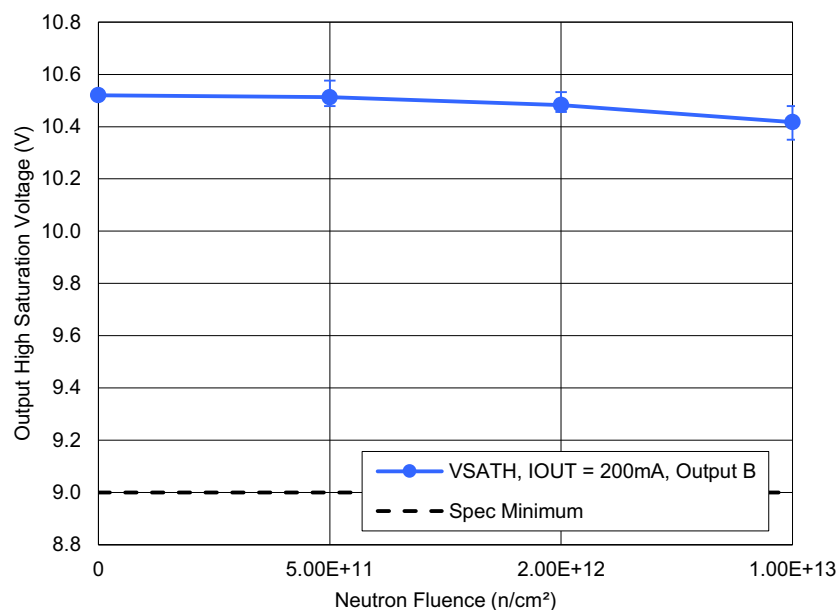


Figure 43. IS-1825ASRH output high saturation voltage (V_{SATH}), B output at 200mA, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a minimum of 9V.

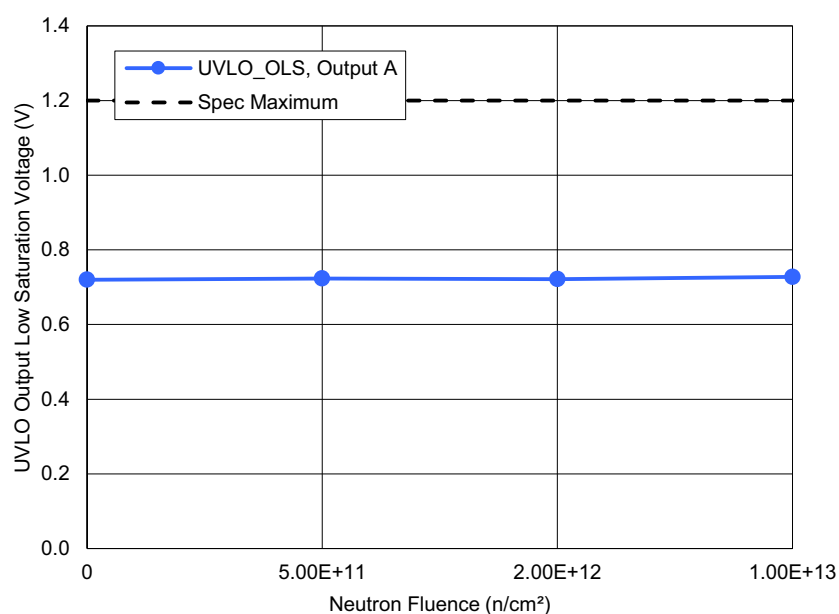


Figure 44. IS-1825ASRH undervoltage lockout (UVLO) output low saturation voltage ($UVLO_{OLS}$), A output, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 1.2V.

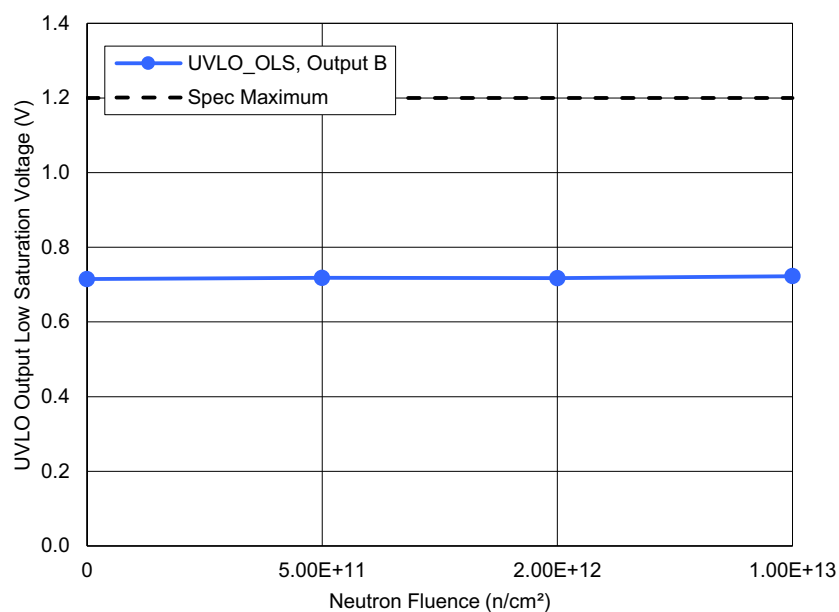


Figure 45. IS-1825ASRH undervoltage lockout (UVLO) output low saturation voltage ($UVLO_{OLS}$), B output, following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 1.2V.

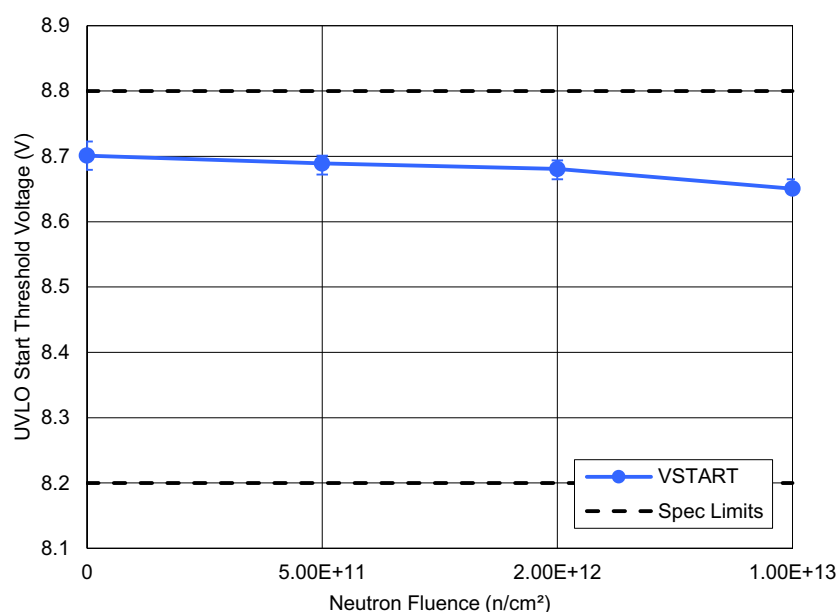


Figure 46. IS-1825ASRH undervoltage lockout (UVLO) start threshold voltage (V_{START}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 8.2V and a maximum of 8.8V.

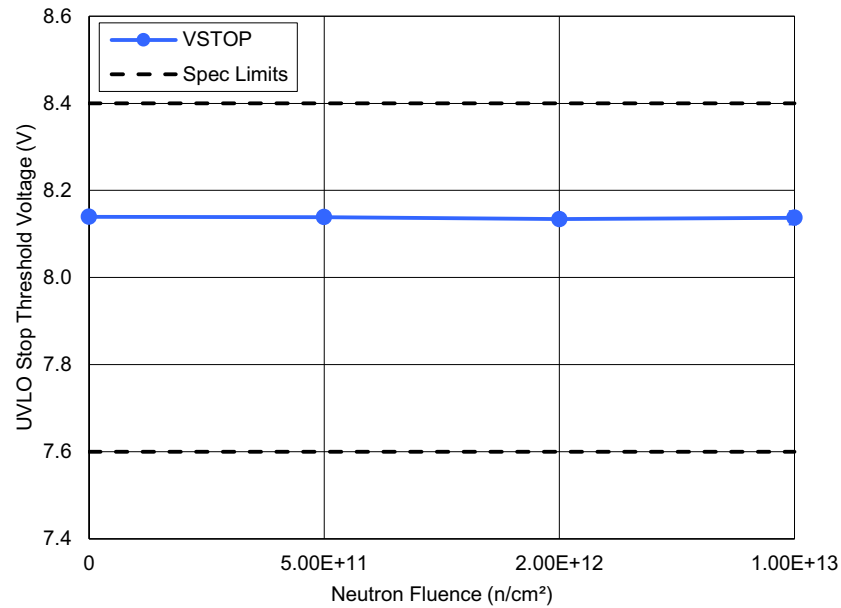


Figure 47. IS-1825ASRH undervoltage lockout (UVLO) stop threshold voltage (V_{STOP}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 7.6V and a maximum of 8.4V.

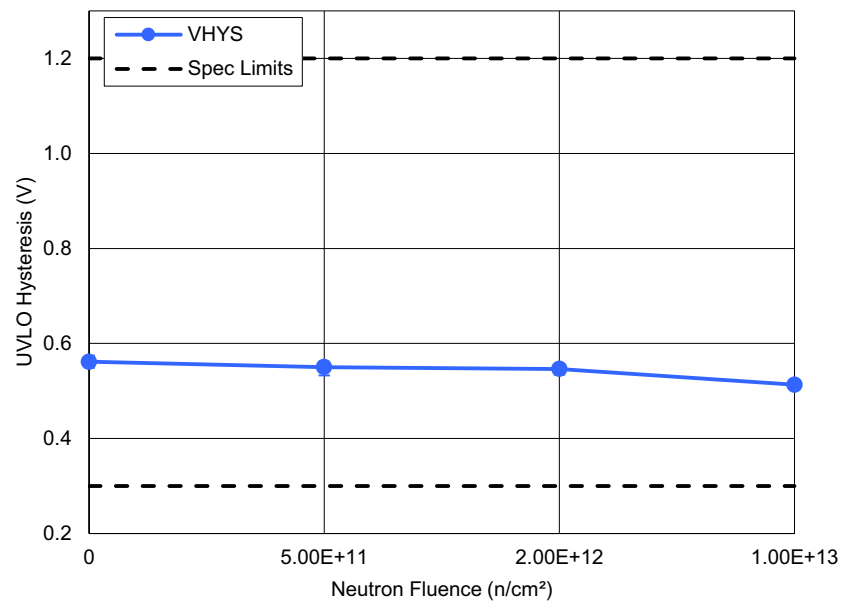


Figure 48. IS-1825ASRH undervoltage lockout (UVLO) hysteresis (V_{HYS}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limits are a minimum of 0.3V and a maximum of 1.2V.

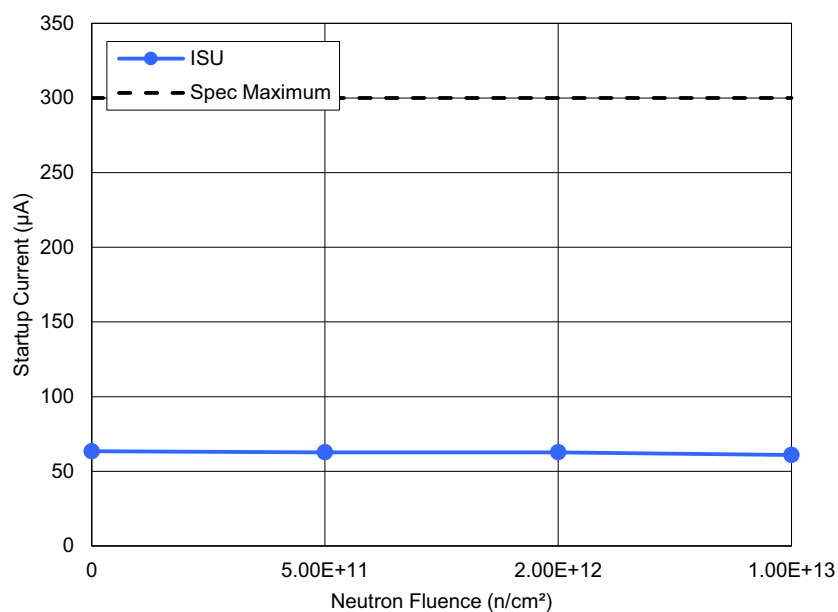


Figure 49. IS-1825ASRH startup current (I_{SU}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 300µA.

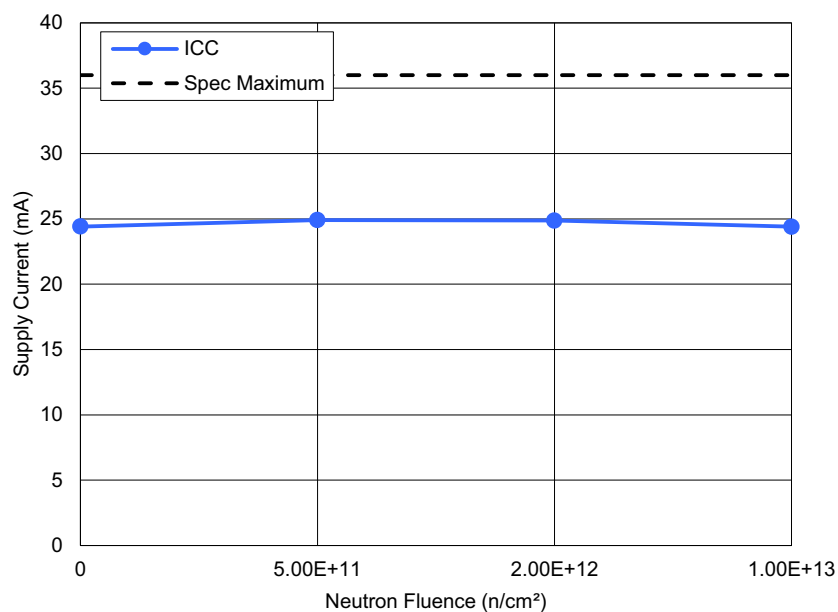


Figure 50. IS-1825ASRH startup current (I_{CC}) following irradiation to each level. The error bars (if visible) represent the minimum and maximum measured values. The post-TID irradiation SMD limit is a maximum of 36mA.

3. Discussion and Conclusion

This document reports the 1MeV equivalent neutron testing results of the IS-1825ASRH, the high-speed dual output PWM. Parts were tested at actual fluences of $5.30 \times 10^{11} \text{n/cm}^2$, $2.33 \times 10^{12} \text{n/cm}^2$, and $1.04 \times 10^{13} \text{n/cm}^2$. The results of key parameters before and after irradiation to each level are plotted in [Figure 2](#) through Figure 50. The plots show the mean of each parameter as a function of neutron irradiation, with error bars representing the minimum and maximum measured values. The figures also show the applicable electrical limits taken from the SMD. However, these limits are provided for guidance only as the IS-1825ASRH is not specified for the neutron environment.

All samples passed the post-TID irradiation SMD limits after all three exposures up to and including $1.04 \times 10^{13} \text{n/cm}^2$.

4. Revision History

Revision	Date	Description
1.00	Jul 3, 2023	Initial release.

A. Appendix

Table 3. Reported Parameters

Figure	Parameter	Symbol	Conditions	Low Limit	High Limit	Unit
2	Reference Output Voltage	V_{REF}		4.92	5.28	V
3	Line Regulation	V_{LINE}	$12.0V < V_S < 20V$	-20	20	mV
4	Load Regulation	V_{LOAD}	$1mA < I_{OUT} < 10mA$	-50	50	mV
5	Total Output Variation	V_{OM}	$V_S = 12V, I_{OUT} = 1mA$	4.92	5.28	V
6			$V_S = 20V, I_{OUT} = 1mA$	4.92	5.28	V
7			$V_S = 12V, I_{OUT} = 10mA$	4.92	5.28	V
8			$V_S = 20V, I_{OUT} = 10mA$	4.92	5.28	V
9	Reference Short Circuit Current	I_{SC}	$V_{REF} = 0V$	20	-	mA
10	Oscillator Frequency	F_O		300	425	kHz
11	Oscillator Frequency PSRR	F_{PSRR}	$12.0V < V_S < 20V$	-3	3	%
12	Oscillator Total Frequency Variation	F_{OM}	$V_S = 12V$	300	425	kHz
13			$V_S = 20V$	300	425	kHz
14	Clock Output High Voltage	V_{CLKH}		3.75	-	V
15	Clock Output Low Voltage	V_{CLKL}		-	0.2	V
16	Error Amplifier Input Offset Voltage	V_{OS}	$V_{CM} = 3V, V_O = 3V$	-10	10	mV
17	Error Amplifier Input Bias Current	I_{BIAS}	$V_{CM} = 3V, V_O = 3V$	-2	2	μA
18	Error Amplifier Input Offset Current	I_{OS}	$V_{CM} = 3V, V_O = 3V$	-2	2	μA
19	Error Amplifier Open Loop Gain	A_{VOL}	$1V < V_O < 4V$	60	-	dB
20	Error Amplifier Common Mode Rejection Ratio	CMRR	$1.5V < V_{CM} < 4V$	65	-	dB
21	Error Amplifier Power Supply Rejection Ratio	PSRR	$12V < V_S < 20V$	70	-	dB
22	Error Amplifier Output Sink Current	I_{OL}	$V_{E/A OUT} = 1V$	1	-	mA
23	Error Amplifier Output Source Current	I_{OH}	$V_{E/A OUT} = 4V$	-0.5	-	mA
24	Error Amplifier Output High Voltage	$V_{E/A OH}$	$I_{E/A OUT} = -0.5mA$	4	-	V
25	Error Amplifier Output Low Voltage	$V_{E/A OL}$	$I_{E/A OUT} = 1mA$	-	1	V
26	Comparator Ramp Bias Current	I_{RAMP}	$V_{RAMP} = 0V$	-8	-	μA
27	Duty Cycle Range	DC_{MAX}	Output A	40	-	%
28			Output B	40	-	%

Table 3. Reported Parameters (Cont.)

Figure	Parameter	Symbol	Conditions	Low Limit	High Limit	Unit
29	Ramp Offset	$RAMP_{OFFSET}$	$V_{RAMP} = 0V$	0.81	-	V
30	Soft-Start Charge Current	I_{CHG}	$V_{SS} = 2.5V$	8	25	μA
31	Soft-Start Discharge Current	I_{DCHG}	$V_{SS} = 2.5V$	0.1	0.5	mA
32	Restart Threshold	V_{RS}	-	-	0.5	V
33	Current-Sense Bias Current	I_{BLIM}	$0V < V_{ILIM} < 2V$	-	15	μA
34	Current Limit Threshold	V_{LIMIT}	-	0.85	1.15	V
35	Overcurrent Threshold	V_{OVER}	-	1.05	1.26	V
36	Output Low Saturation Voltage	V_{SATL}	Output A, $I_{OUT} = 20mA$	-	0.8	V
37			Output B, $I_{OUT} = 20mA$	-	0.8	V
38			Output A, $I_{OUT} = 200mA$	-	2.2	V
39			Output B, $I_{OUT} = 200mA$	-	2.2	V
40	Output High Saturation Voltage	V_{SATH}	Output A, $I_{OUT} = 20mA$	10	-	V
41			Output B, $I_{OUT} = 20mA$	10	-	V
42			Output A, $I_{OUT} = 200mA$	9	-	V
43			Output B, $I_{OUT} = 200mA$	9	-	V
44	UVLO Output Low Saturation Voltage	$UVLO_{OLS}$	Output A	-	1.2	V
45			Output B	-	1.2	V
46	Start Threshold Voltage	V_{START}	-	8.2	8.8	V
47	Stop Threshold Voltage	V_{STOP}	-	7.6	8.4	V
48	UVLO Hysteresis	V_{HYS}	-	0.3	1.2	V
49	Startup Current	I_{SU}	$V_S = 8V$	-	300	μA
50	Supply Current	I_{CC}	$V_{INV} = V_{RAMP} = V_{ILIM/SD} = 0V$ $V_{NON-INV} = 1V$	-	36	mA

A.1 Related Information

For a full list of related documents, visit our website:

- [IS-1825ASRH](#) device page
- MIL-STD-883 test method 1017

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.