Single Event Testing of the IS-139ASRH Quad Comparator

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Introduction

The intense heavy ion environment encountered in space applications can cause a variety of transient and destructive effects in analog circuits, including single-event latchup (SEL), single-event upset (SEU) and single-event burnout (SEB). These effects can lead to system-level failures including disruption and permanent damage. For predictable, reliable space system operation these components have to be specifically designed and fabricated for SEE hardness, followed by SEE testing to validate the design. This report discusses the results of preliminary SEE testing of the Intersil IS-139ASRH quad comparator.

Product Description

The Intersil IS-139ASRH is a functional equivalent to the industry standard LM139 quad voltage comparator. The base LM139 has been widely used in space systems and has been the subject of frequent radiation testing in both the total dose and energetic heavy ion environments. It has shown vulnerability to low dose rate effects (ELDRS) and will propagate single-event pulse (SEP) phenomena into the circuitry it is driving, necessitating redundancy, filtering or error correction techniques to avoid system upset. The Intersil IS-139ASRH is hardened to a linear energy transfer (LET) of 80 MeV.cm^2/mg. This is achieved through redundant comparator architecture, on-chip filtering and appropriate device sizing. Additional circuitry provides full testability for each of the redundant comparators.

The IS-139ASRH is available in two versions that differ in their total dose lot acceptance testing. The IS-139ASEH is acceptance tested on a wafer by wafer basis to 300 krad(Si) at high dose rate (50 – 300 rad(Si)/s) and to 50 krad(Si) at low dose rate (0.01 rad(Si)/s). The IS-1395ASRH is acceptance tested on a wafer by wafer basis to 300 krad(Si) at high dose rate (50 – 300 rad(Si)/s) only. Both versions use the same die.

SEE Test Objectives

The objectives of SEE testing of the IS-139ASRH were to evaluate the single-event latchup performance of the part and to determine its single-event transient vulnerability.

SEE Test Procedure

Samples of the IS-139ASRH were tested for single-event effects at the Cyclotron Institute at Texas A&M University using Au ions (LET= 83.9 MeV.cm^2/mg), Kr ions (LET= 38.0 MeV.cm^2/mg) and Ar ions (LET= 8.0 MeV.cm^2/mg).

At the TAMU facility, all SEE testing is performed outside the chamber. The device under test was mounted in the beam line and irradiated with heavy ions of the appropriate species. All SEU/SET testing was done with the beam perpendicular to the chip surface. The samples were assembled into dual in-line packages with the metal lids removed for beam exposure. The beam was directed on to the exposed die and the beam flux, beam fluence and device output errors were measured.

The tests were controlled remotely from the control room. All input power was supplied from portable supplies connected to the DUT via a cable. The supply currents were monitored along with the device outputs. All currents were measured with digital meters and all output waveforms were displayed on a digital oscilloscope for ease of identifying different types of SEE effects displayed by the part. Events were captured by triggering on changes in the output pulses.

Single Event Latchup and Burnout Testing Results

The IS-139ASRH is built in the Intersil radiation-hardened Silicon Gate (RSG) process, and the dielectrically isolated material used for this process eliminates all latchup mechanisms. As expected, no burnout or latchup was observed using Au ions (LET = 83.9 MeV.cm^2/mg) at 60 degree incidence from perpendicular, equivalent to an effective LET of 181.8, as compared to testing at normal incidence. Testing was performed on three parts at 25^{o}C and two parts at 125^{o}C, with all parts at maximum supply voltage (Vcc=30V). All tests were run at a fluence of 10^7 ions/cm^2. All four comparator minus inputs were tied to 1V and the plus inputs were toggled from zero to 2V at 1kHz, 50% duty cycle. During ion exposure, outputs were monitored on a four channel digital phosphor oscilloscope and supply current was monitored on a current meter. Idd was recorded pre and post exposure, under continues power, and results are shown in Table 1. As can be seen from the table, no latchup or other destructive effects were observed.

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Table 1: IS-139ASRH Icc Pre and Post SEB/SEL Testing

		Pre-Exposure	Post-Exposure
SN	Temp	Icc (mA)	Icc (mA)
4	25^{o}C	2.348	2.351
6		2.320	2.321
9		2.334	2.335
4	125^{o}C	2.378	2.381
6		2.345	2.349

Single Event Upset Testing Results

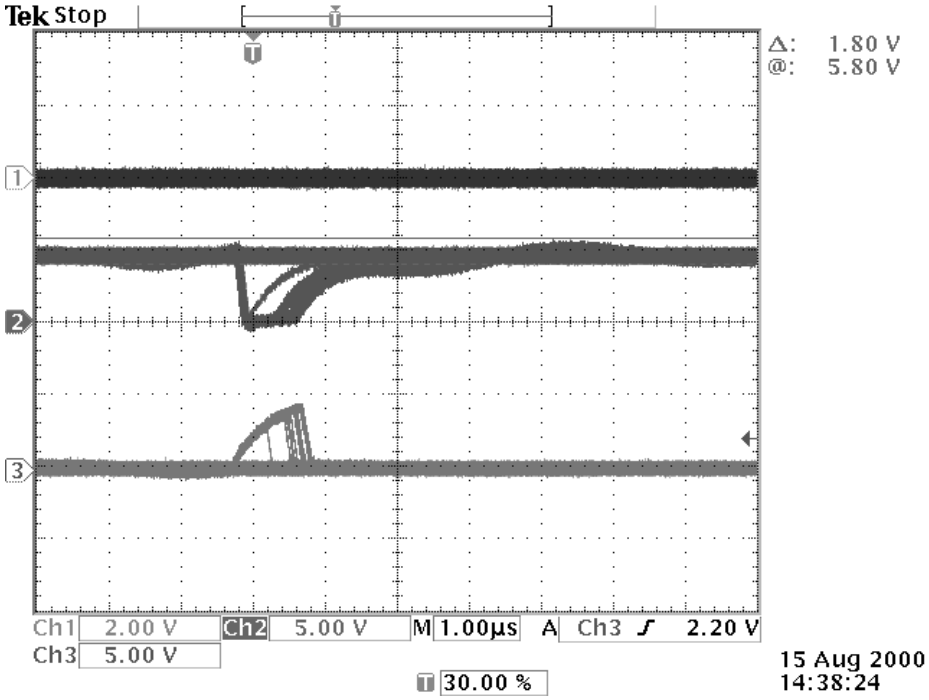
The SEU hardened IS -139ASRH achieves SEU/SET immunity by incorporating redundant architecture, on-chip filtering and appropriate device sizing. (See Figure 1 for a schematic representation.) If a given transistor has an SEU/SET event, the output will remain in the correct state.

During the SEL/SEB testing the comparator outputs were monitored with a digital phosphor oscilloscope with the persistence set at infinity. Any output transient would then be "painted" onto the screen. No upsets or transients were observed. The SEL/SEB testing was done with 1V overdrive on the inputs. Since the input offset voltage spec is to the order of 2 - 5mV, there is nearly a volt of noise immunity on the inputs. If the input overdrive is reduced to values near the offset voltage, a particle strike on input or output devices can generate noise in the fixture's parasitic R/L/C. If this noise causes the input offset to decrease below specification, the output will accordingly change state.

Figure 1 shows external components and parasitics of the SEU/SET test setup. A 10 ft. shielded cable connects the device under test to the test electronics. This cable's inner conductor has an inductance of 3.3uH (Lcable in figure) and distributed from it to the shield (tied to ground at each end) is a stray capacitance of 300pF (Ccable in figure). The test fixture had additional sockets wired in adjacent to the comparators under test to permit various values of resistors (RS) and capacitors (CIN) to be plugged in. This enabled characterization of the minimum input offset voltage required to be free of output transients for a range of source impedance and input capacitance applications. Taking the case of an ion passing through an input electrostatic discharge protection diode (shown as ESD in Fig. 1), we see that this will either dump charge into or pull current out of the input depending on whether the clamp diode to Vcc or ground is hit. The resultant input voltage transient would be minimized for high CIN, low RS and low Lcable.

The comparator was characterized for the minimum differential input voltage ('overdrive') required to eliminate output transients for a range of input resistances and capacitances. Results are given in Tables 2-4. Two comparators were used for this characterization, one with its inputs held at a positive differential and the other at an equal but negative differential. One output would then be in the "1" logic state, the other in the logic "0" state. The minimum overdrive needed to avoid transients in Tables 2-4 is the worst case of the two.

Each reading was verified good using a minimum fluence of $5x10^5$ ions/cm^2. For input levels below these minimum overdrive values, sufficient noise is generated on the inputs to overcome the input differential applied. The outputs would then switch, but recover within 2us. Scope traces shown on the next page show HL glitches on channel two and LH glitches on another comparator on channel three. This is data from S/N3, testing with Kr, at Vcc=9V, input offset = 5mV, VL=5V, RL=1K, CIN=0 and RIN=0.



Scope photo: HL glitches on channel two and LH glitches on another comparator on channel three. This is data from sample S/N 3, testing with Kr, at Vcc=9V, Input offset = 5mV, VL=5V, RL=1K, CIN=0 and RIN=0.

Note from the data in Table 2 that when the input overdrive was raised to 5.8mV, these upsets ceased. No output HL transients occur once sufficient noise margin is applied to the inputs, even with a direct strike on the output driver device or output ESD clamp diodes. This is because the maximum calculated SEU charge for an ion with a LET of 90, at 60 degrees incidence from vertical, is only 32 pC with this oxide isolated process. With the output load capacitance of 300pf, only a 0.1V perturbation would occur.

Table 2: Minimum Input Overdrive (mV) for No Output transients vs. RIN; CIN = 0pf

CIN	RIN (ohms)	Vcc (V)	Minimum Input Overdrive (mV)				
			Au (LET=87)		Kr (LET=35)		Ar (LET=8)
			SN 7	SN 13	SN 3	SN 13	SN 13
0pF	0	9	5	4.8	5.8	5	5
		15	6.8	6.5	6.7	5	5
		30	7.5	6.6	6.7	5	5
	300	9	7.5		10		
		15	9.3		10		
		30	9.3		14		
	1K	9	18	18	10	6	
		15	18	18	10	8	
		30	18	18	13	10	
	3.2K	9	34		12		5
		15	34		15		5
		30	36		26		5
	10K	9	87	86	25	25	5.4
		15	89	86	38	36	
		30	89	88	50	50	15
	32K	9	188		45		6.3
		15	192		84		24
		30	192		90		27
	100K	9	270	272	150	58	12.5
		15	270	276	150	125	27
		30	270	279	150	131	51

Table 3: Minimum Input Overdrive (mV) for No Output transients vs. RIN; CIN = 100pf

CIN	RIN (ohms)	Vcc (V)	Minimum Input Overdrive (mV)				
			Au (LET=87)		Kr (LET=35)		Ar (LET=8)
			SN7	SN13	SN3	SN13	SN13
100 pF	0	9					
		15					
		30					
	300	9					
		15					
		30					
	1K	9	18		6	5	
		15	19		6	6	
		30	19		7.5	6.8	
	3.2K	9					
		15					
		30					
	10K	9	61		10		
		15	61		26		
		30	61		35		
	32K	9					
		15					
		30					
	100K	9	97		40	40	8.2
		15	97		46	46	10
		30	98		53	52	20

Table 4: Minimum Input Overdrive (mV) for No Output transients vs. RIN; CIN = 300pf

CIN	RIN (ohms)	Vcc (V)	Minimum Input Offset Voltage (mV)				
			Au (LET=87)		Kr (LET=35)		Ar (LET=8)
			SN7	SN13	SN3	SN13	SN13
300 pf	0	9					
		15					
		30					
	300	9					
		15					
		30					
	1K	9					
		15					
		30					
	3.2K	9					
		15					
		30					
	10K	9	31				
		15	31				
		30	32				
	32K	9					
		15					
		30					
	100K	9	44				
		15	44				
		30	45				

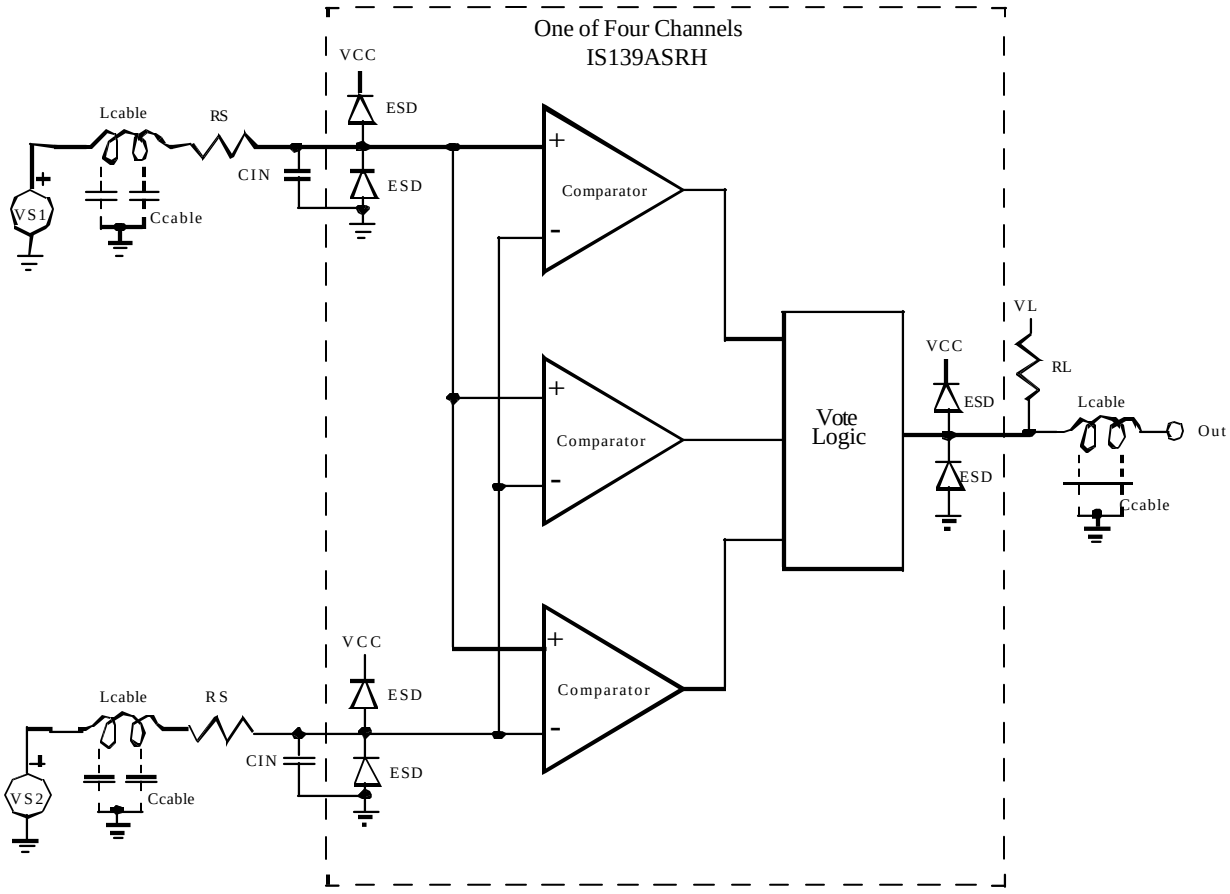


Figure 1. Functional Schematic, one of four IS139ASRH Channels, input source drivers/parasitics and output load.

Conclusion

As expected, the IS-139ASRH quad comparator showed no destructive effects or latchup up to an effective LET of 181.8 MeV.cm^2/mg. Upset testing was performed at several LET values; upset at the comparator outputs were observed only at very low values of input overdrive. Under these conditions, the device is vulnerable to noise induced into the input stage and external wiring. When overdrive values are above these critical levels, the comparator will not display any output transients.