Calculation of Semiconductor Failure Rates

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One of the fundamentals of understanding a product's reliability requires an understanding of the calculation of the failure rate. The traditional method of determining a product's failure rate is through the use of accelerated high temperature operating life tests performed on a sample of devices randomly selected from its parent population. The failure rate obtained on the life test sample is then extrapolated to end-use conditions by means of predetermined statistical models to give an estimate of the failure rate in the field application. Although there are many other stress methods employed by semiconductor manufacturers to fully characterize a product's reliability, the data generated from operating life test sampling is the principal method used by the industry for estimating the failure rate of a semiconductor device in field service. This article focuses on describing the methods used in calculating the failure rate and ends with showing the failure rates determined for some of Intersil's newer integrated circuit process technologies.

Table 1 gives definitions of some of the terms used to describe the failure rate of semiconductor devices.

Table 1: FAILURE RATE PRIMER.

TERMS	DEFINITIONS/DESCRIPTIONS
Failure Rate (λ)	Measure of failure per unit of time. The useful life failure rate is based on the exponential life distribution. The failure rate typically decreases slightly over early life, then stabilizes until wear-out which shows an increasing failure rate. This should occur beyond useful life.
Failure In Time (FIT)	Measure of failure rate in 10^9 device hours; e. g. 1 FIT = 1 failure in 10^9 device hours.
Total Device Hours (TDH)	The summation of the number of units in operation multiplied by the time of operation.
Mean Time To Failure (MTTF)	Mean of the life distribution for the population of devices under operation or expected lifetime of an individual, MTTF =1/λ, which is the time where 63.2% of the population has failed. Example: For λ = 10 FITs, MTTF = 1/λ = 100 million hours.
Confidence Level or Limit (CL)	Probability level at which population failure rate estimates are derived from sample life test. The upper confidence level interval is used.
Acceleration Factor (AF)	A constant derived from experimental data which relates the times to failure at two different stresses. The AF allows extrapolation of failure rates from accelerated test conditions to use conditions.

A simple failure rate calculation based on a single life test would follow equation 1.

$$\lambda \propto \frac{1}{TDH \times AF} \qquad \text{(Eq. 1)}$$

where,

λ = failure rate.

TDH = Total Device Hours = Number of units x hours under stress.

AF = Acceleration factor, see Equation 3.

Since reliability data can be accumulated from a number of different life tests with several different failure mechanisms, a comprehensive failure rate is desired. The failure rate calculation can be complicated if there are more than one failure mechanisms in a life test, since the failure mechanisms are thermally activated at different rates. Equation 1 accounts for these conditions and includes a statistical factor to obtain the confidence level for the resulting failure rate.

$$\lambda = \sum_{i=1}^{\beta} \left(\frac{x_i}{\left(\sum_{j=1}^{k} TDH_j \times AF_{ij} \right)} \right) \times \frac{M \times 10^9}{\sum_{i=1}^{\beta} x_i} \qquad \text{(Eq. 2)}$$

where,

λ = failure rate in FITs (Number fails in 10^9 device hours)

β = Number of distinct possible failure mechanisms

k = Number of life tests being combined

x_i = Number of failures for a given failure mechanism i = 1, 2,... β

TDH_j = Total device hours of test time for life test j, j = 1, 2,... k

AF_{ij} = Acceleration factor for appropriate failure mechanism, i = 1, 2,... k

$M = X^2_{(\alpha,\, 2r+2)} / 2$

where,

X^2 = chi square factor for 2r + 2 degrees of freedom

r = total number of failures (Σx_i)

α = risk associated with CL between 0 and 1.

In the failure rate calculation, acceleration factors (AF_{ij}) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. The acceleration factor is determined from the Arrhenius equation. This equation is used to describe physio-chemical reaction rates and has been found to be an appropriate model for expressing the thermal acceleration of semiconductor device failure mechanisms.

$$AF = exp\left(\frac{E_a}{k} \left(\frac{1}{T_{use}} - \frac{1}{T_{stress}} \right) \right) \qquad \text{(Eq. 3)}$$

where,

AF = Acceleration Factor

E_a = Thermal Activation Energy (Table 2)

k = Boltzmann's Constant (8.63 x 10^{-5} eV/K)

T_{use} = Use Temperature (°C + 273)

T_{stress} = Life test stress temperature (°C + 273)

Both T_{use} and T_{stress} (in degrees Kelvin) need to include the internal temperature rise of the device to represent the junction temperature of the chip under bias.

Failure rates for commercial, industrial and military applications are generally published at 55°C with a 60% CL within the semiconductor industry. Critical system applications sometimes specify a 90% or 95% CL at 55°C or 125°C. Derating to other temperatures and CLs are available from Intersil upon request.

The thermal activation energy (E_a) of a failure mechanism is determined by performing tests at a minimum of two different temperature stress levels. The stresses will provide the time to failure (t_f) for the two (or more) populations, thus allowing the simultaneous solution for the activation energy as follows:

$$ln(t_{f1}) = C + \frac{E_a}{kT_1} \quad \text{(Eq. 4)}$$

$$ln(t_{f2}) = C + \frac{E_a}{kT_2} \quad \text{(Eq. 5)}$$

By subtracting the two equations, and solving for the activation energy, the following equation is obtained.

$$E_a = \left(k \times \frac{ln(t_{f1}) - ln(t_{f2})}{(\frac{1}{T_1} - \frac{1}{T_2})} \right) \quad \text{(Eq. 6)}$$

Table 2 below lists several different failure mechanisms, their cause, and the activation energy associated with each. If no failure is recorded for the sample on life test the default activation energy is 1.0 eV, for an unknown failure mechanism an activation energy of 0.7 eV is assumed. Also listed is a possible screen to find the failure mechanism and how to control the problem if it occurs.

Table 2: FAILURE MECHANISM

Failure Mechanism	Activation Energy	Screening and Testing Methodology	Control Methodology
Oxide Defects	0.3 - 0.5eV	High Temperature operating life (HTOL) and voltage stress.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3 - 0.5eV	HTOL and voltage stress screens.	Vendor statistical Quality Control programs, and Statistical Process Control on thermal processes.

Table 2: FAILURE MECHANISM

Failure Mechanism	Activation Energy	Screening and Testing Methodology	Control Methodology
Corrosion	0.45ev	Highly Accelerated Stress Testing (HAST).	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5 - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor statistical Quality Control programs, Statistical Process Control of assembly processes, and proper handling.
Electromigration - Al line - Contact/Via	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design process groundrules to match measured data, statistical control of metals, photoresist and passivation.
Mask Defects/ Photoresist Defects	0.7eV	Mask Fab comparisons, print checks, defect density monitor in Fab, voltage stress test and HTOL.	Clean room control, clean mask, pellicles, Statistical Process Control of photoresist/ etch processes.
Contamination	1.0eV	C-V stress of oxides, wafer fab device stress test and HTOL.	Statistical Process Control of C-V data, oxide/interconnect cleans, high integrity glassivation and clean assembly process.
Charge Injection	1.3eV	HTOL and oxide characterization.	Design groundrules based on test results, wafer level Statistical Process Control of gate length and control of gate oxide thickness.

Example

Here is a simple example of how the above equations can be used to calculate the failure rate from life test data. Assume that 600 parts where stressed at 150°C ambient for 3000 hours with one failure at 2000 hours for a photoresist flaw (0.7eV) and one failure at 3000 hours for an oxide defect (0.3eV); the internal temperature rise (T_j) of the part is 20°C and the product was tested at 1000, 2000 and 3000 hours. We want to find the FIT rate for the process with a 95% CL at 55°C. Using the Arrhenius relationship (Eq. 3), the acceleration factors are computed as follows:

$$AF_1 = exp\left[\frac{0.7}{8.63\times10^{-5}}\left(\frac{1}{348}-\frac{1}{443}\right)\right] = 148.2 \qquad \text{Photoresist flaw} \qquad \text{(Eq. 7)}$$

$$AF_2 = exp\left[\frac{0.3}{8.63\times10^{-5}}\left(\frac{1}{348}-\frac{1}{443}\right)\right] = 8.52 \qquad \text{Oxide defect} \qquad \text{(Eq. 8)}$$

X^2 = 12.6, which is dependent on the degrees of freedom (2r + 2) = 6 for r = 2 failures and $\alpha = 95 / 100 = 0.95$ for CL = 95%. M is then simply $X^2/2$ = 6.3.

The total device hours (TDH) is derived from the summation of the devices on stress multiplied by their test duration.

$$TDH = 600 \times 1000 + 599 \times 1000 + 598 \times 1000 = 1.797 \times 10^6 hours$$

From Eq. 2 , λ in FITs is computed as follows:

$$\lambda = \left(\frac{1}{1.797 \times 10^6 \times 148.2} + \frac{1}{1.797 \times 10^6 \times 8.52}\right) \times \left(\frac{6.3 \times 10^9}{2}\right) = 218 \text{ FITs} \quad \text{(Eq. 9)}$$

Note that for a 60% CL, the X^2 = 6.2, which yields 107 FITs.

The MTTF can be calculated from the reciprocal of the failure rate multiplied by 10^9.

$$MTTF = \left(\frac{1}{FITs}\right) \times 10^9 = 4.59 \times 10^6 \text{ hours @ 95\%CL} \quad \text{(Eq. 10)}$$

$$MTTF = \left(\frac{1}{FITs}\right) \times 10^9 = 9.35 \times 10^6 \text{ hours @ 60\%CL} \quad \text{(Eq. 11)}$$

Intersil Process FIT rates

Table 3 below gives the FIT rate and MTTF for several Intersil processes.

Table 3: FIT rate of Intersil Processes.

Process	Derating Temperature / CL	FIT rate	MTTF (hours)
AVLSI1R (26CT31-32)	55°C 60% CL 55°C 95% CL	7.0 FITs 24.0 FITs	1.34E+8 hours 4.09E+7 hours
AVLSI1RA (in qualification)	55°C 60% CL 55°C 95% CL	3.20 FITs 10.4 FITs	3.13E+8 hours 9.57E+7 hours
TSOS4 (64K X 1 SRAM) (in qualification)	55°C 60% CL 55°C 95% CL	6.11 FITs 20.0 FITs	1.64E+8 hours 5.00E+7 hours
VHFP (hermetic)	55°C 60% CL 55°C 95% CL	16.95 FITs 31.48 FITs	5.90E+7 hours 3.18E+7 hours