

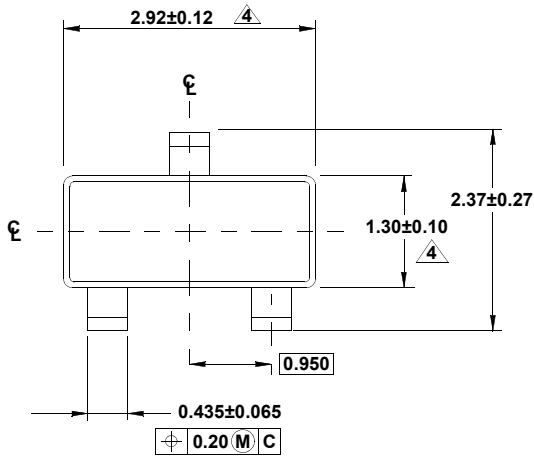
Plastic Packages for Integrated Circuits

Package Outline Drawing

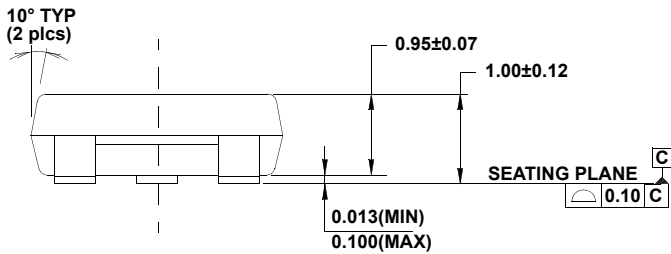
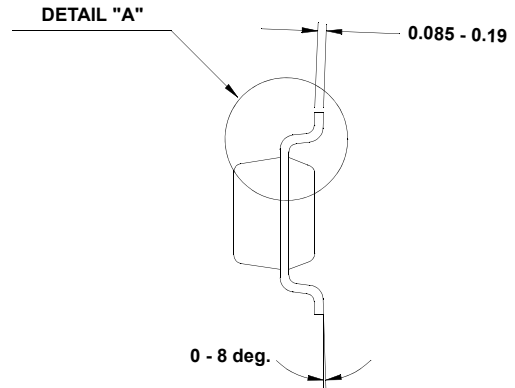
P3.064

3 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE (SOT23-3)

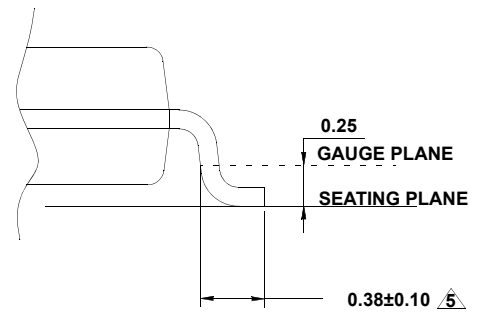
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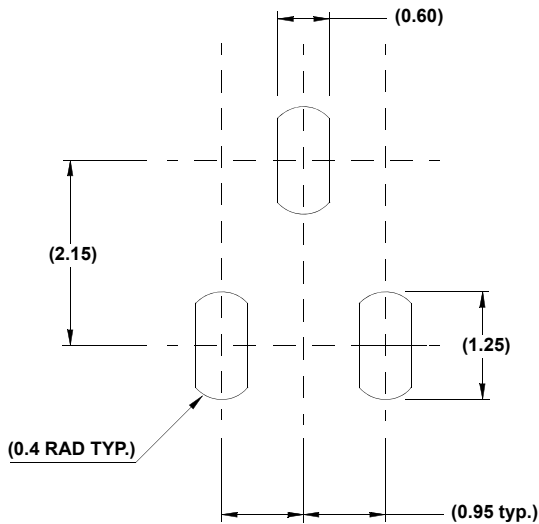
TOP VIEW



SIDE VIEW



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters. Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Reference JEDEC TO-236.
4. Dimension does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. Footlength is measured at reference to gauge plane.